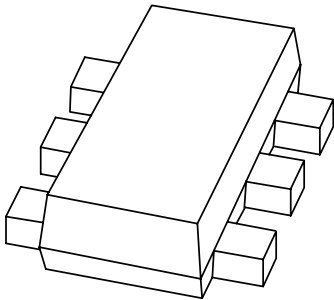


DATA SHEET



PEMH11

NPN resistor-equipped transistors;
 $R1 = 10\text{ k}\Omega$, $R2 = 10\text{ k}\Omega$

Preliminary specification

2001 Oct 22

NPN resistor-equipped transistors; R1 = 10 kΩ, R2 = 10 kΩ

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FEATURES

- 300 mW total power dissipation
- Very small 1.6 × 1.2 mm ultra thin package
- Self alignment during soldering due to straight leads
- Replaces two SC-75/SC-89 packaged transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

NPN resistor-equipped transistors in a SOT666 plastic package.

MARKING

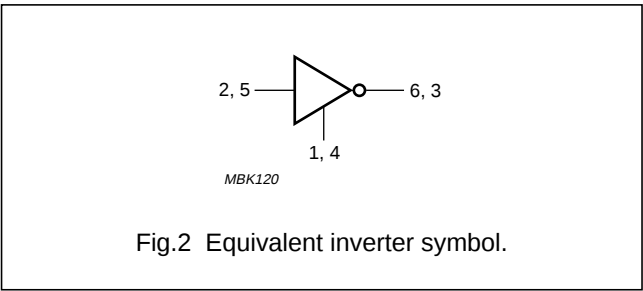
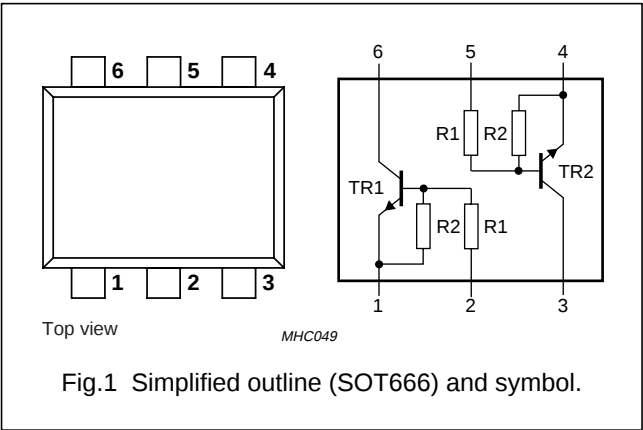
TYPE NUMBER	MARKING CODE
PEMH11	H1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	50	V
I _{CM}	peak collector current	100	mA
TR1	NPN	–	–
TR2	NPN	–	–
R1	bias resistor	10	kΩ
R2	bias resistor	10	kΩ

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



NPN resistor-equipped transistors; R1 = 10 kΩ, R2 = 10 kΩ

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _i	input voltage				
	positive		–	+40	V
	negative		–	–10	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	300	mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

NPN resistor-equipped transistors; R1 = 10 k Ω , R2 = 10 k Ω

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CHARACTERISTICS

T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor						
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0	–	–	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 50 V; I _B = 0	–	–	1	μ A
		V _{CE} = 30 V; I _B = 0; T _j = 150 °C	–	–	50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0	–	–	400	μ A
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA	30	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA	–	–	150	mV
V _{i(off)}	input off voltage	V _{CE} = 5 V; I _C = 100 μ A	–	–	0.5	V
V _{i(on)}	input on voltage	V _{CE} = 0.3 V; I _C = 10 mA	2.5	–	–	V
R1	input resistor		7	10	13	k Ω
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C _c	collector capacitance	I _E = I _e = 0; V _{CB} = 10 V; f = 1 MHz	–	–	2.5	pF

NPN resistor-equipped transistors; R1 = 10 k Ω , R2 = 10 k Ω

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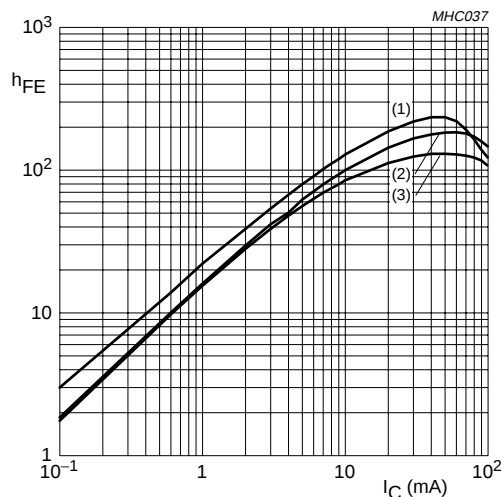
 $V_{CE} = 5\text{ V}$.(1) $T_{amb} = 150^\circ\text{C}$.(2) $T_{amb} = 25^\circ\text{C}$.(3) $T_{amb} = -40^\circ\text{C}$.

Fig.3 DC current gain as a function of collector current; typical values.

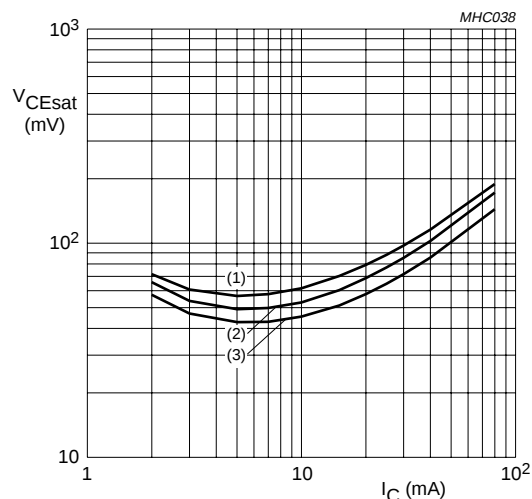
 $I_C/I_B = 20$.(1) $T_{amb} = 100^\circ\text{C}$.(2) $T_{amb} = 25^\circ\text{C}$.(3) $T_{amb} = -40^\circ\text{C}$.

Fig.4 Collector-emitter saturation voltage as a function of collector current; typical values.

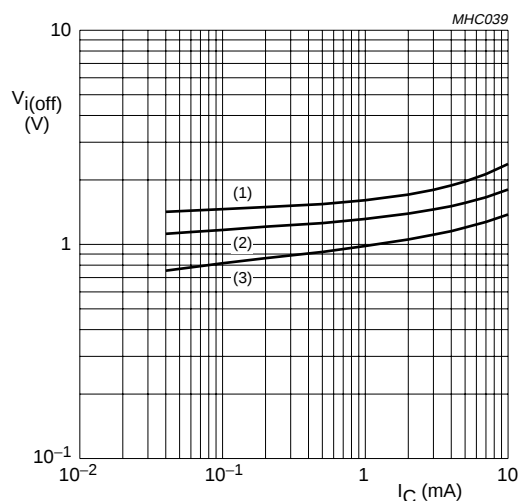
 $V_{CE} = 5\text{ V}$.(1) $T_{amb} = -40^\circ\text{C}$.(2) $T_{amb} = 25^\circ\text{C}$.(3) $T_{amb} = 100^\circ\text{C}$.

Fig.5 Input-off voltage as a function of collector current; typical values.

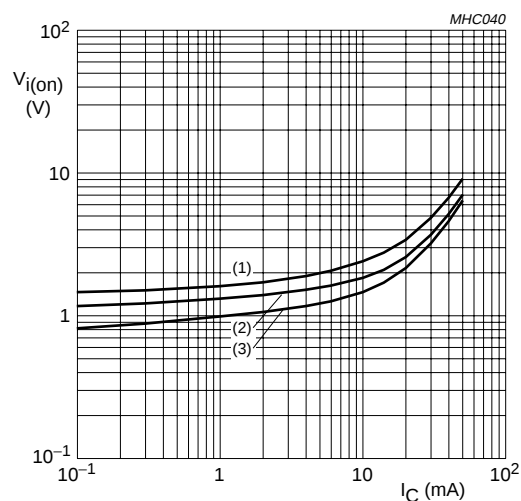
 $V_{CE} = 0.3\text{ V}$.(1) $T_{amb} = -40^\circ\text{C}$.(2) $T_{amb} = 25^\circ\text{C}$.(3) $T_{amb} = 100^\circ\text{C}$.

Fig.6 Input-on voltage as a function of collector current; typical values.

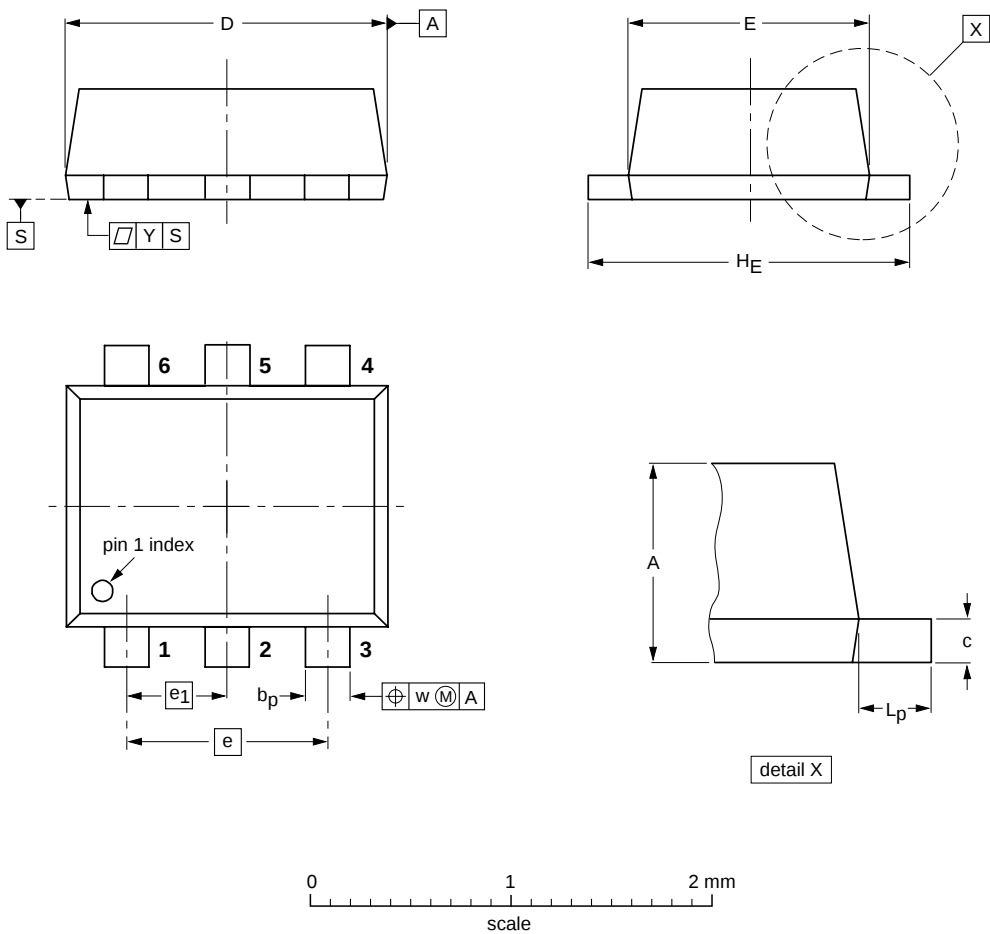
NPN resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

NPN resistor-equipped transistors; R1 = 10 k Ω , R2 = 10 k Ω

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Contact information

For additional information please visit **<http://www.semiconductors.philips.com>**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

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