

PHP/PHB/PHD98N03LT

TrenchMos™ logic level FET

Rev. 04 — 21 October 2002

Product data

1. Description

N-channel logic level field-effect power transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHP98N03LT in SOT78 (TO-220AB)

PHB98N03LT in SOT404 (D²-PAK)

PHD98N03LT in SOT428 (D-PAK).

2. Features

- Low on-state resistance
- Fast switching.

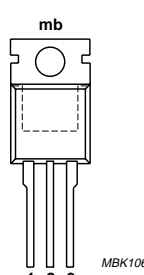
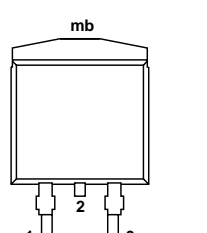
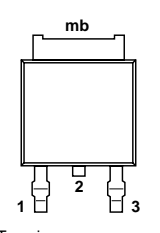
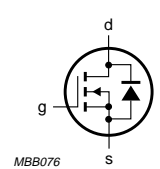
3. Applications

- Computer motherboard high frequency DC to DC converters.

4. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT428 simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)		

			
SOT78 (TO-220AB)	SOT404 (D²-PAK)	SOT428 (D-PAK)	

[1] It is not possible to make connection to pin 2 of the SOT404 and SOT428 packages.

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	111	W
T_j	junction temperature		-	175	°C
$R_{DS(on)}$	drain-source on-state resistance	$T_j = 25\text{ °C}; V_{GS} = 10\text{ V}; I_D = 25\text{ A}$	5.2	5.9	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 5\text{ V}; I_D = 25\text{ A}$	6.2	7.3	mΩ

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

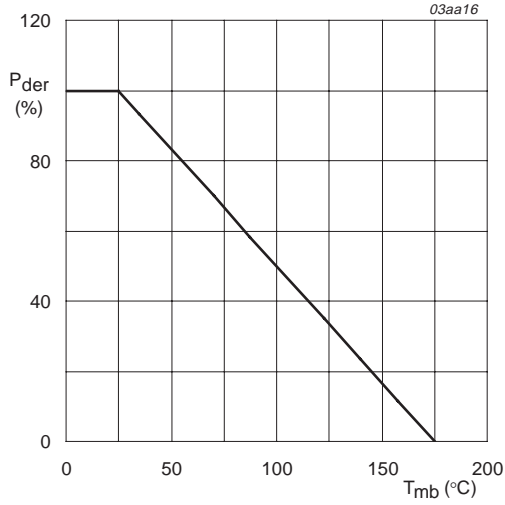
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	25	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2 and 3	-	75	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2	-	66	A
V_{GS}	gate-source voltage		-	±20	V
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	111	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C

Source-drain diode

I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	75	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	240	A

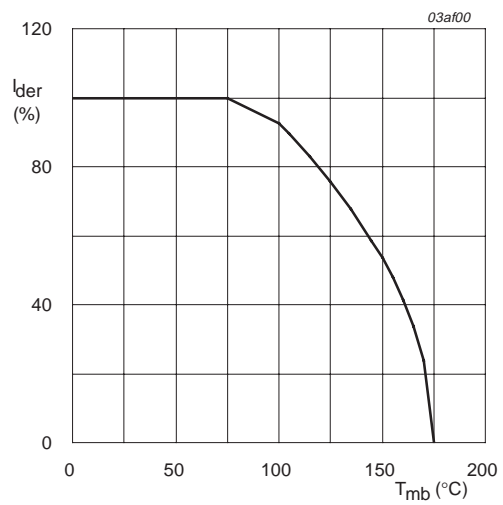
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 43\text{ A}; t_p = 0.27\text{ ms}; V_{DD} = 15\text{ V};$ $R_{GS} = 50\text{ }\Omega; V_{GS} = 5\text{ V};$ starting $T_j = 25\text{ °C};$	-	183	mJ
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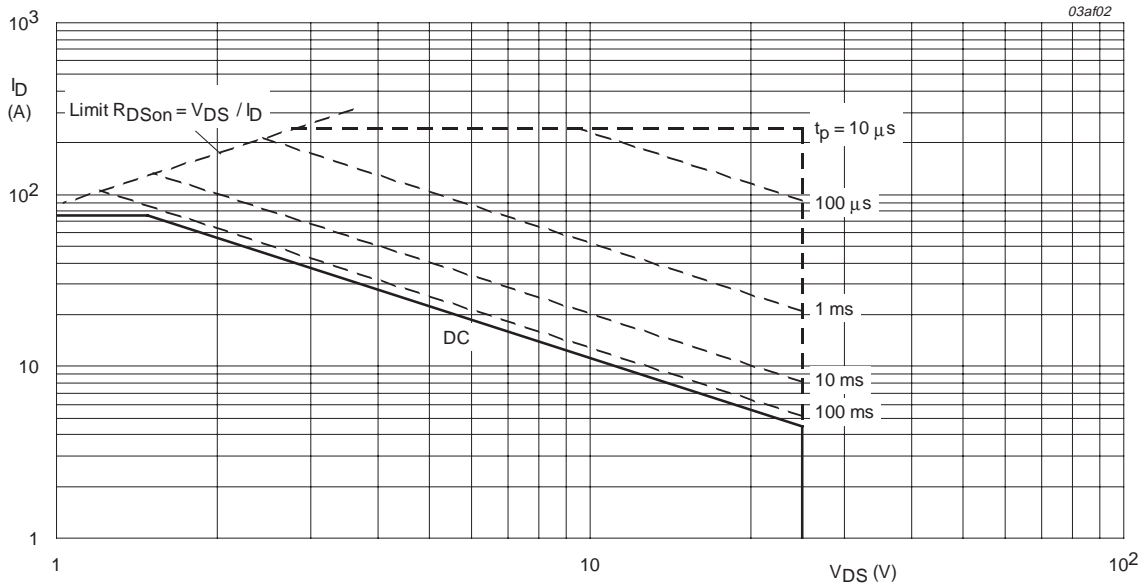
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.35	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78 package	vertical in still air	-	60	-	K/W
	SOT428 package	SOT428 minimum footprint; mounted on a PCB	-	75	-	K/W
	SOT404 and SOT428 packages	SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

7.1 Transient thermal impedance

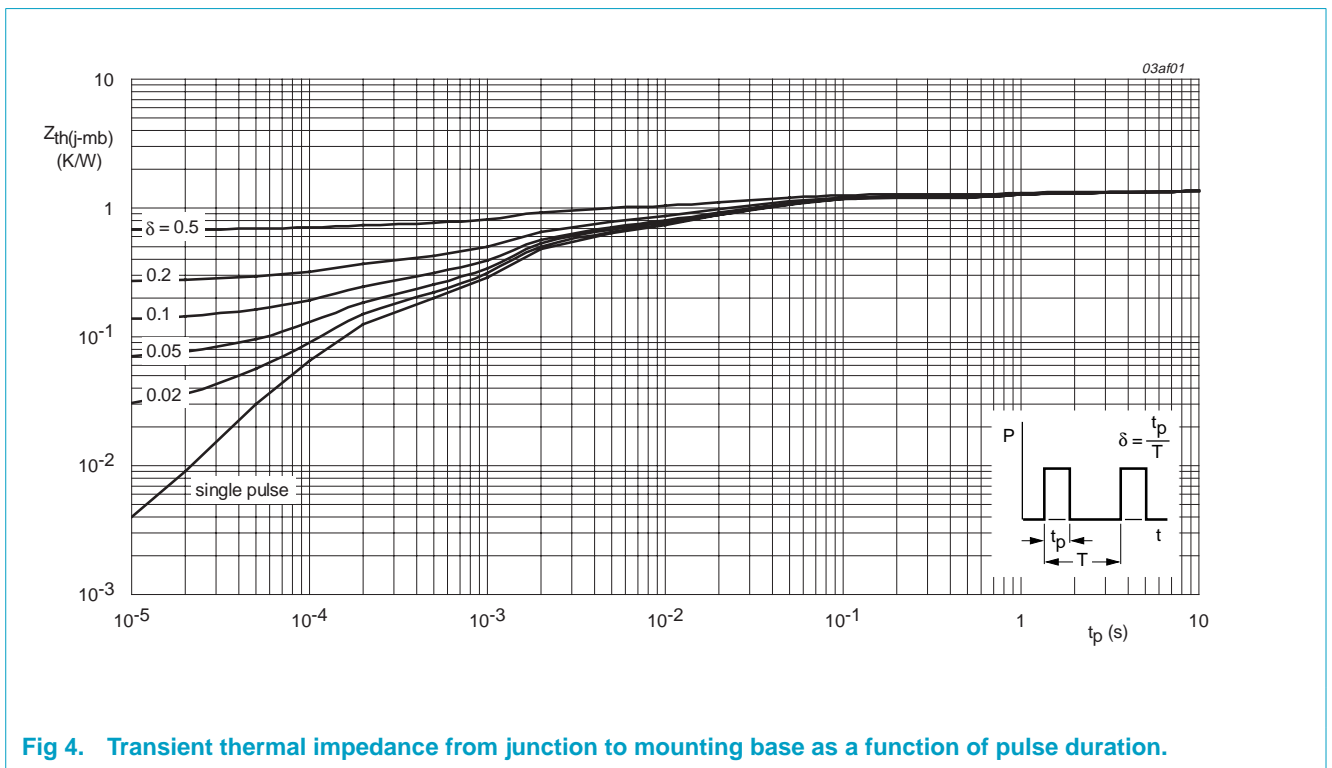
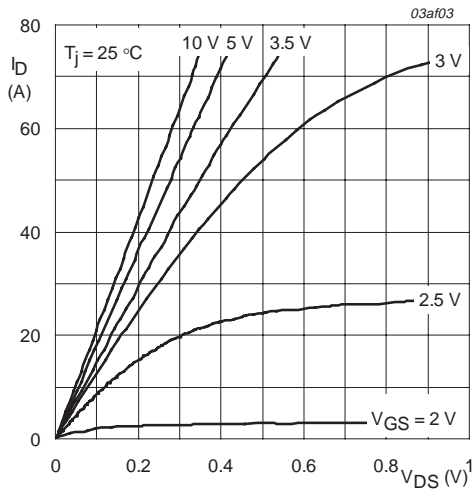


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

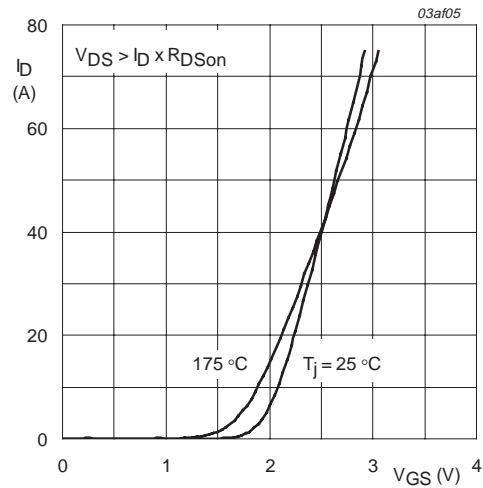
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V T _j = 25 °C	25	-	-	V
		T _j = -55 °C	22	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 T _j = 25 °C	1	1.5	2	V
		T _j = 175 °C	0.5	-	-	V
		T _j = -55 °C	-	-	2.3	V
I _{DSS}	drain-source leakage current	V _{DS} = 25 V; V _{GS} = 0 V T _j = 25 °C	-	0.05	1	μA
		T _j = 175 °C	-	-	500	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±15 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; Figure 7 and 8 T _j = 25 °C	-	6.2	7.3	mΩ
		T _j = 175 °C	-	10.5	12.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; Figure 7 and 8	-	5.2	5.9	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 50 A; V _{DD} = 15 V; V _{GS} = 5 V; Figure 13	-	40	-	nC
Q _{gs}	gate-source charge		-	16	-	nC
Q _{gd}	gate-drain (Miller) charge		-	15	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 20 V; f = 1 MHz; Figure 11	-	3000	-	pF
C _{oss}	output capacitance		-	710	-	pF
C _{rss}	reverse transfer capacitance		-	510	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 15 V; I _D = 12.5 A; V _{GS} = 5 V; R _G = 5.6 Ω	-	18	-	ns
t _r	rise time		-	80	-	ns
t _{d(off)}	turn-off delay time		-	104	-	ns
t _f	fall time		-	104	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 12	-	0.9	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V	-	37	-	ns
Q _r	recovered charge		-	20	-	nC



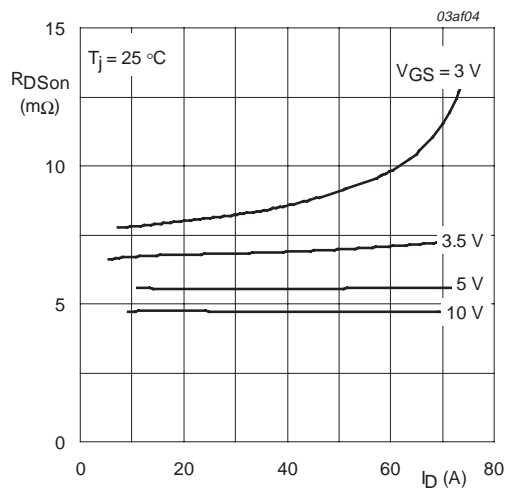
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



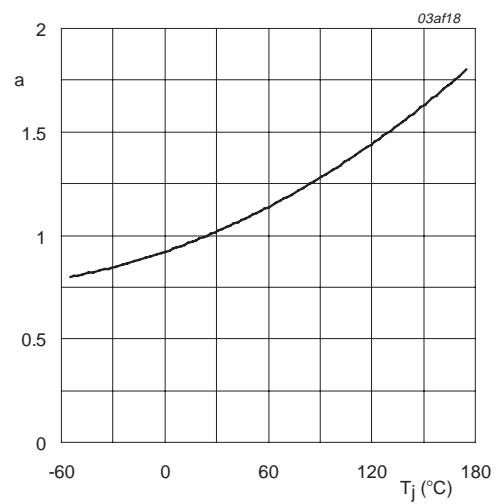
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



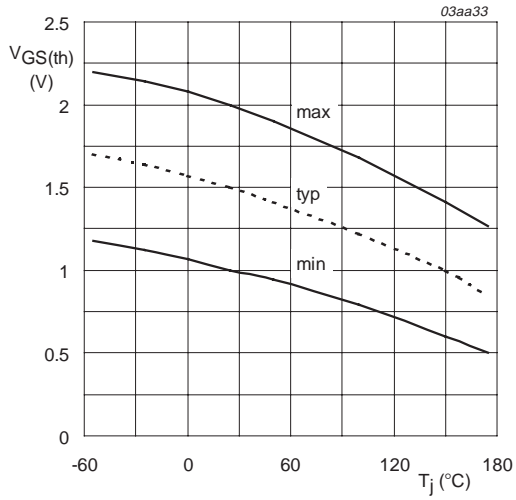
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



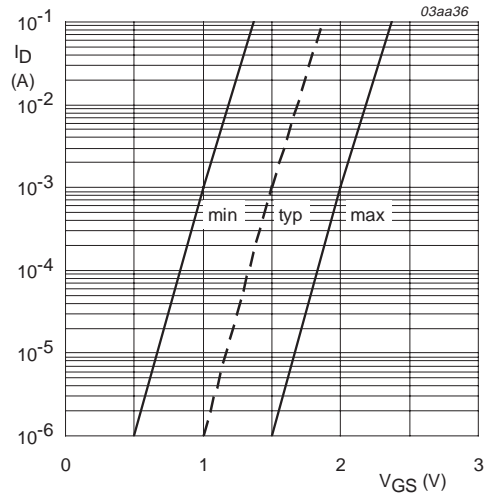
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



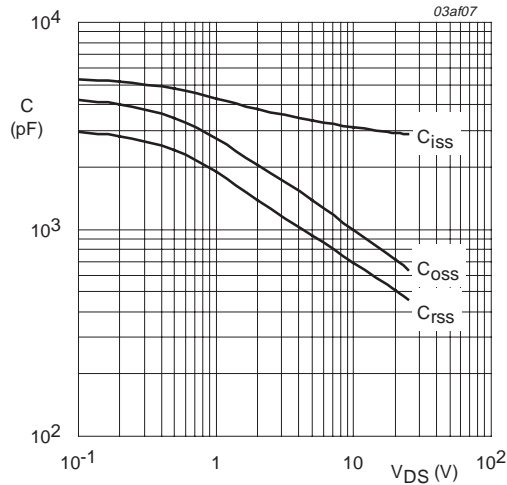
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



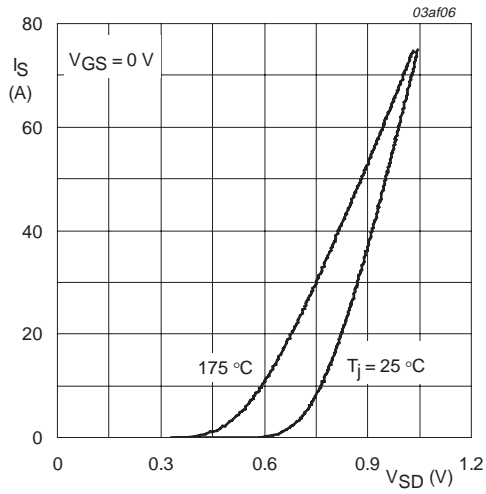
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



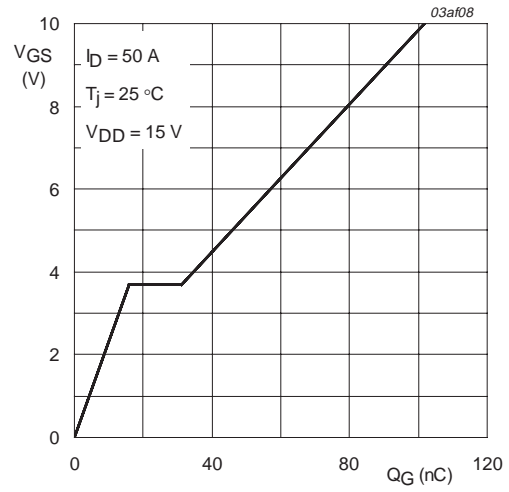
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 175°C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



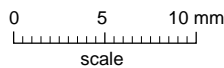
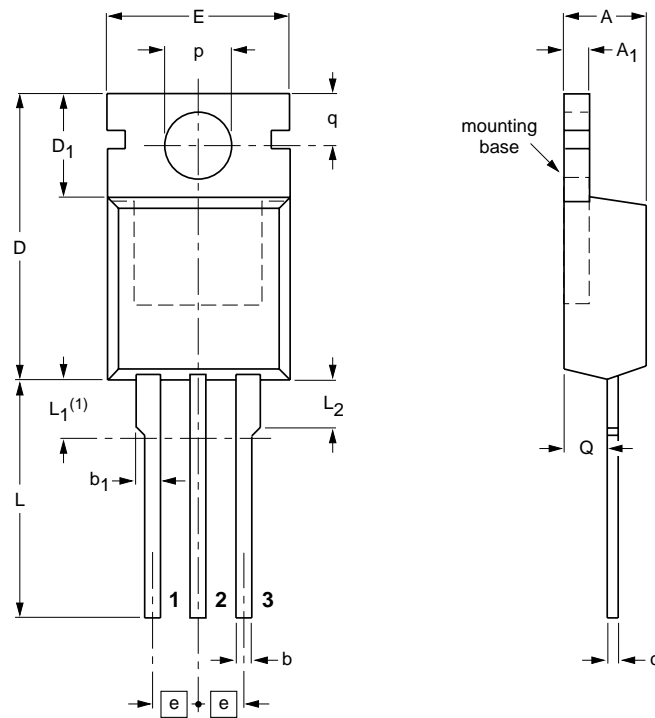
$I_D = 50\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

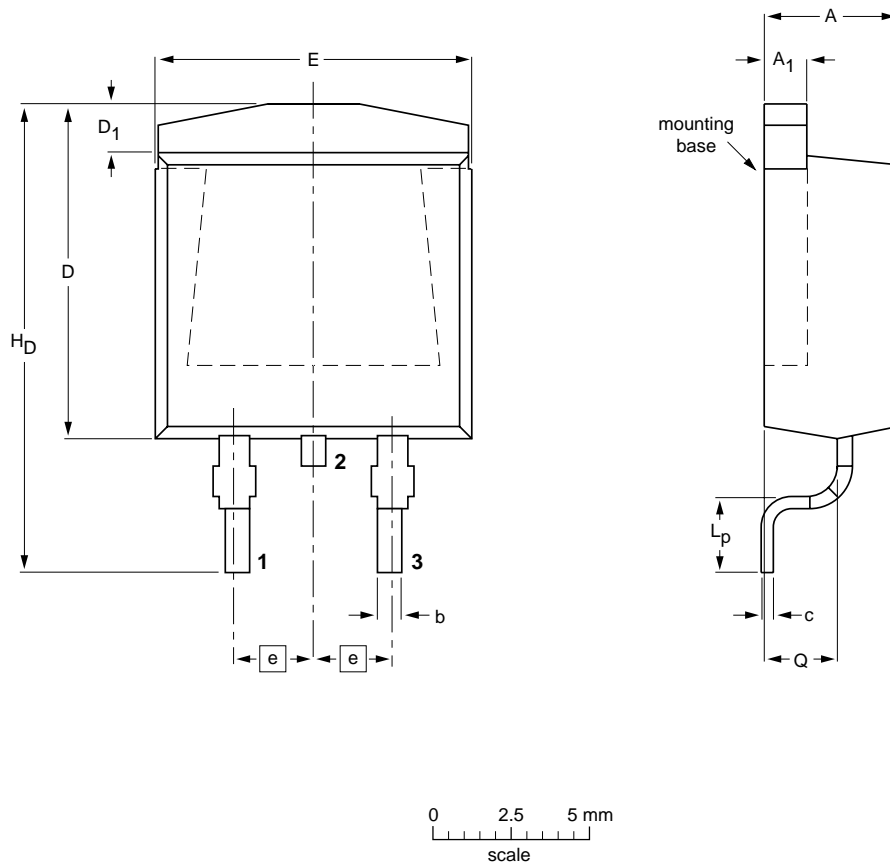
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT78		3-lead TO-220AB	SC-46		00-09-07 01-02-16

Fig 14. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D max.	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT404					99-06-25 01-02-12

Fig 15. SOT404 (D²-PAK)

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

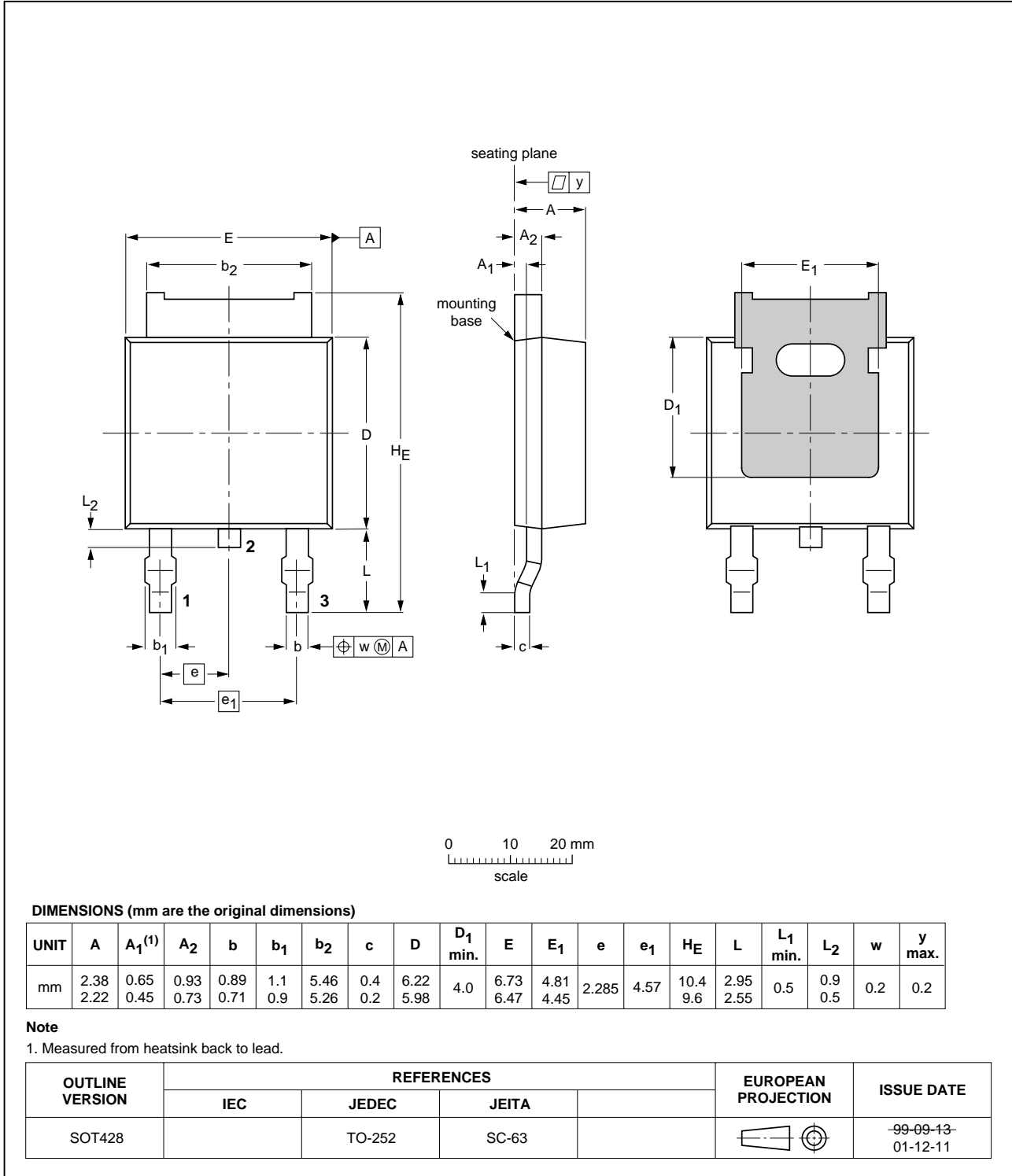


Fig 16. SOT428 (D-PAK)

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
04	20021021	-	Product data; fourth version. Supersedes third version of 20 February 2002 (9397 750 09287). Section 6 "Limiting values" Addition of avalanche ruggedness Graphs updated to latest standard.
03	20020220	-	Product data; third version. Supersedes second version of 18 October 2001. Section 6 "Limiting values" Standardized V_{GS} rating. Section 7 "Thermal characteristics" Clarification of thermal resistances table.
02	20011018	-	Product data; second version. Supersedes data PHP98N03LT-01 of 16 July 2001 (9397 750 08338). Modifications: <ul style="list-style-type: none">• Table 5 "Characteristics" on page 5: added Q_f and t_{rr}.
01	20010716	-	Product data; initial version.

11. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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