

PowerMOS transistor

Logic level FET

PHD3055L**GENERAL DESCRIPTION**

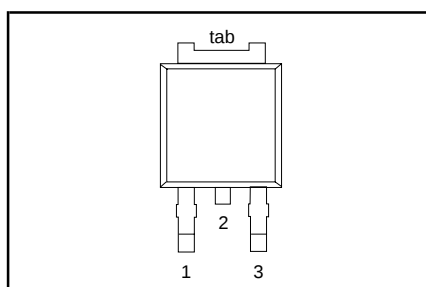
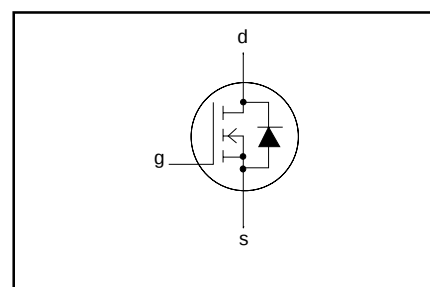
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	12	A
P_{tot}	Total power dissipation	50	W
$R_{DS(ON)}$	Drain-source on-state resistance	0.18	Ω

PINNING - SOT428

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION**SYMBOL****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}; V_{GS} = 10\text{ V}$ $T_{mb} = 100^\circ\text{C}; V_{GS} = 10\text{ V}$	-	12	A
I_{DM}	Pulsed drain current	$T_{mb} = 25^\circ\text{C}$	-	9	A
P_D	Total dissipation	$T_{mb} = 25^\circ\text{C}$	-	48	W
$\Delta P_D / \Delta T_{mb}$	Linear derating factor	$T_{mb} = 25^\circ\text{C}$ $T_{mb} > 25^\circ\text{C}$	-	50	W
V_{GS}	Gate-source voltage		-	0.33	W/K
V_{GSM}	Non-repetitive gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$	-	± 15	V
E_{AS}	Single pulse avalanche energy	$V_{DD} \leq 50\text{ V};$ starting $T_j = 25^\circ\text{C}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 5\text{ V}$	-	± 20	V
I_{AS}	Peak avalanche current	$V_{DD} \leq 50\text{ V};$ starting $T_j = 25^\circ\text{C}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 5\text{ V}$	-	25	mJ
T_j, T_{stg}	Operating junction and storage temperature range		-	6	A
			- 55	175	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	3	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

PowerMOS transistor

Logic level FET

PHD3055L

ELECTRICAL CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	60	-	-	V
$\Delta V_{(BR)DSS} / \Delta T_j$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	-	0.08	-	V/K
$R_{DS(ON)}$	Drain-source on resistance	$V_{GS} = 5\text{ V}; I_D = 6\text{ A}$	-	0.13	0.18	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$	1.0	1.5	2.0	V
g_{fs}	Forward transconductance	$V_{DS} = 50\text{ V}; I_D = 6\text{ A}$	3.5	5.5	-	S
I_{DSS}	Drain-source leakage current	$V_{DS} = 60\text{ V}; V_{GS} = 0\text{ V}$	-	0.1	25	μA
		$V_{DS} = 48\text{ V}; V_{GS} = 0\text{ V}; T_j = 150^\circ\text{C}$	-	1	250	μA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 10\text{ A}; V_{DD} = 48\text{ V}; V_{GS} = 5\text{ V}$	-	7.5	10	nC
Q_{gs}	Gate-source charge		-	1.9	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.5	7	nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 10\text{ A};$ $R_G = 24\text{ }\Omega; R_D = 2.7\text{ }\Omega$	-	12	-	ns
t_r	Turn-on rise time		-	105	-	ns
$t_{d(off)}$	Turn-off delay time		-	26	-	ns
t_f	Turn-off fall time		-	35	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	290	-	pF
C_{oss}	Output capacitance		-	103	-	pF
C_{rss}	Feedback capacitance		-	40	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	$T_{mb} = 25^\circ\text{C}$	-	-	12	A
I_{SM}	Pulsed source current (body diode)	$T_{mb} = 25^\circ\text{C}$	-	-	48	A
V_{SD}	Diode forward voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}$	-	-	1.5	V
t_{rr}	Reverse recovery time	$I_S = 10\text{ A}; V_{GS} = 0\text{ V};$ $di/dt = 100\text{ A}/\mu\text{s}$	-	40	-	ns
Q_{rr}	Reverse recovery charge		-	0.1	-	μC

PowerMOS transistor

Logic level FET

PHD3055L

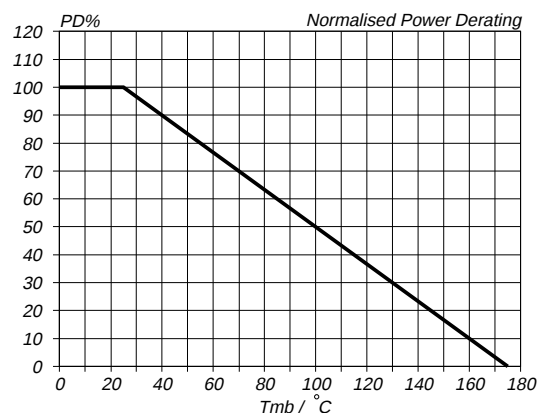


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25\ ^\circ C} = f(T_{mb})$

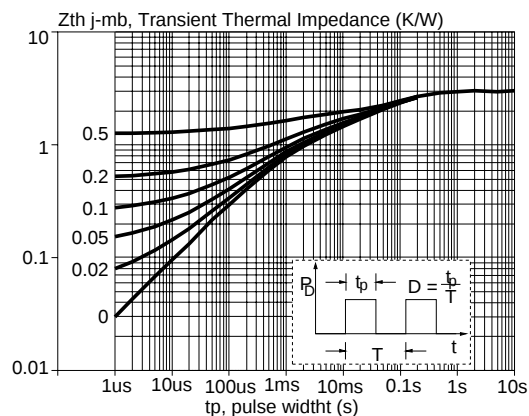


Fig.4. Transient thermal impedance.
 $Z_{th\ j-mb} = f(t)$; parameter $D = t_p / T$

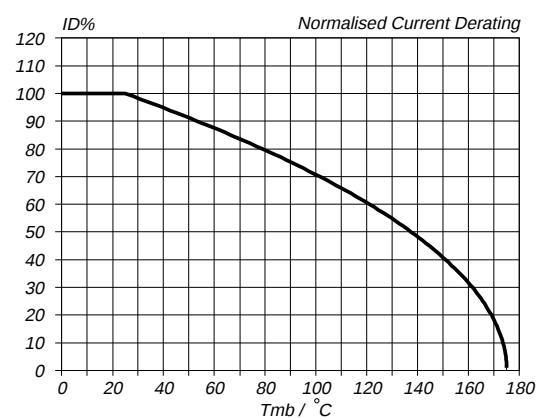


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25\ ^\circ C} = f(T_{mb})$; conditions: $V_{GS} \geq 10\ V$

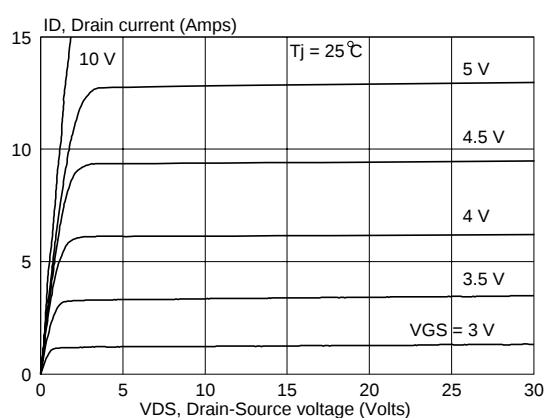


Fig.5. Typical output characteristics.
 $I_D = f(V_{DS})$; parameter V_{GS}

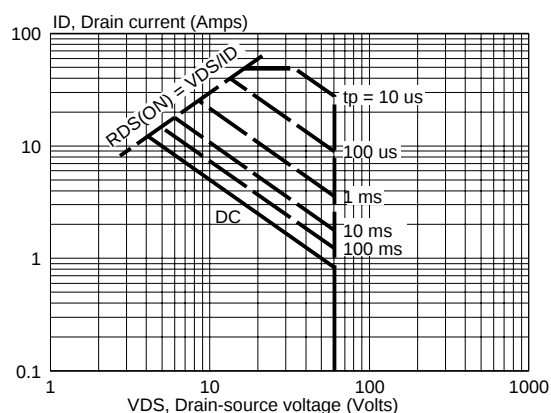


Fig.3. Safe operating area. $T_{mb} = 25\ ^\circ C$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

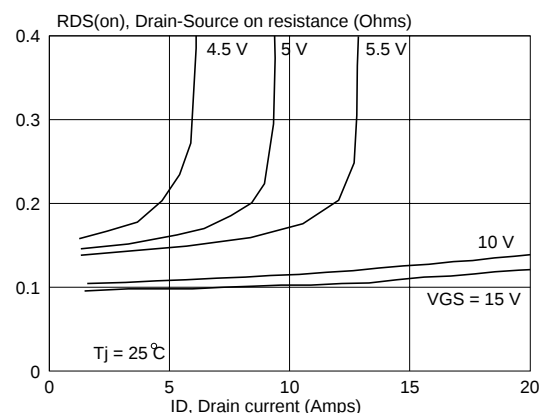
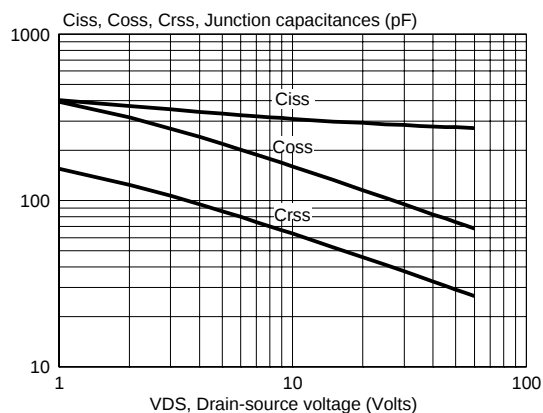
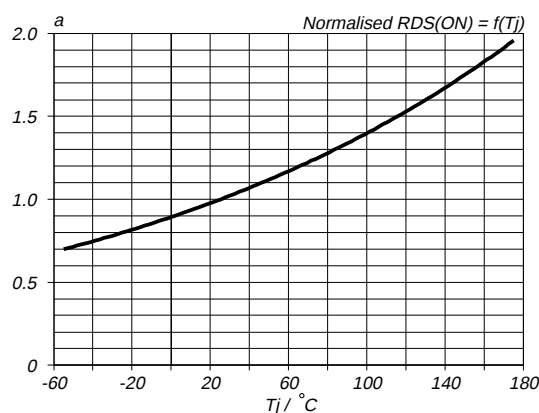
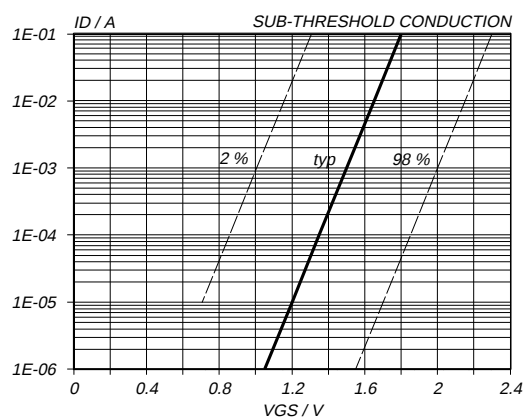
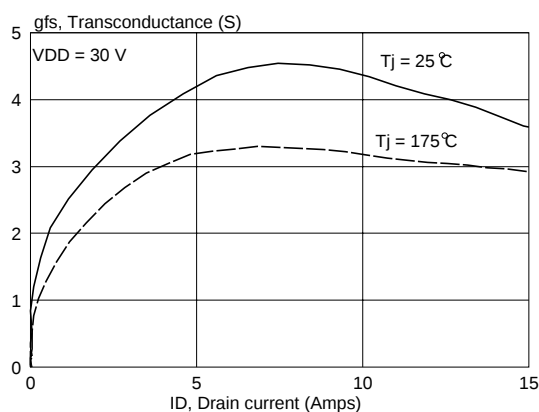
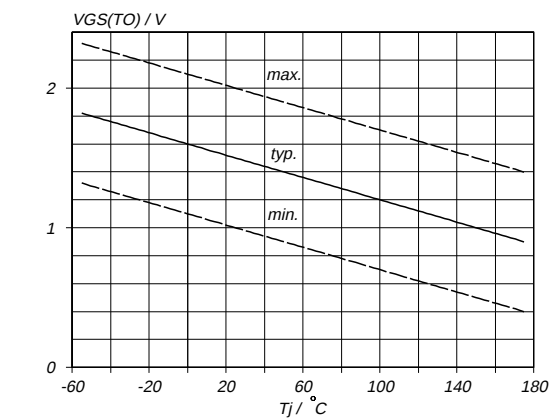
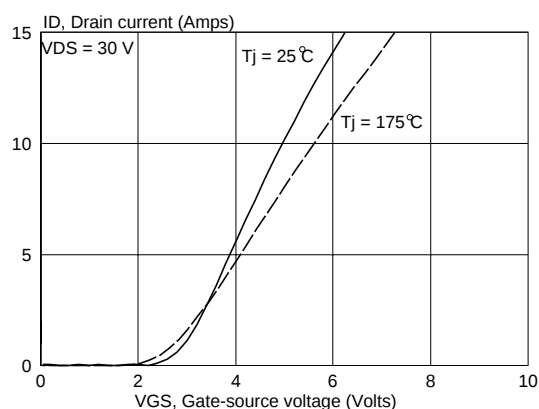


Fig.6. Typical on-state resistance.
 $R_{DS(on)} = f(I_D)$; parameter V_{GS}

PowerMOS transistor

Logic level FET

PHD3055L



PowerMOS transistor

Logic level FET

PHD3055L

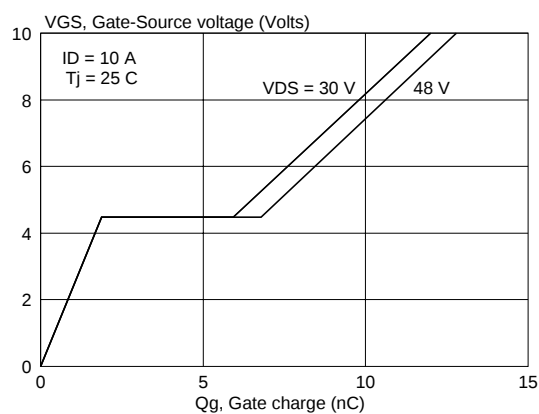


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; parameter V_{DS}

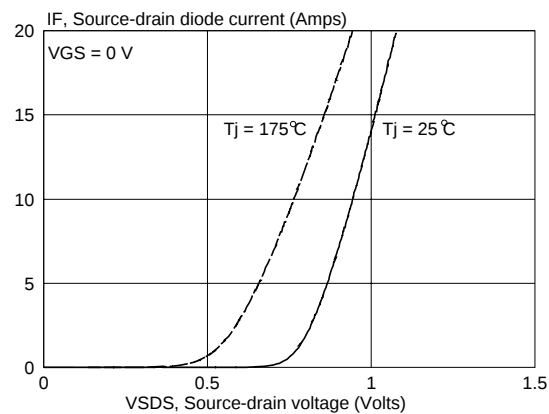


Fig.16. Source-Drain diode characteristic.
 $I_F = f(V_{SDS})$; parameter T_J

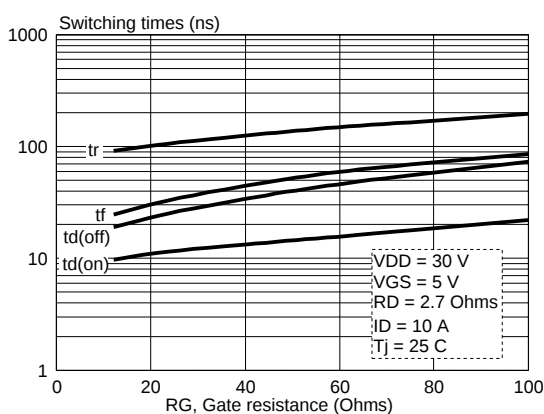


Fig.14. Typical switching times.
 $t_{d(on)}, t_r, t_{d(off)}, t_f = f(R_G)$

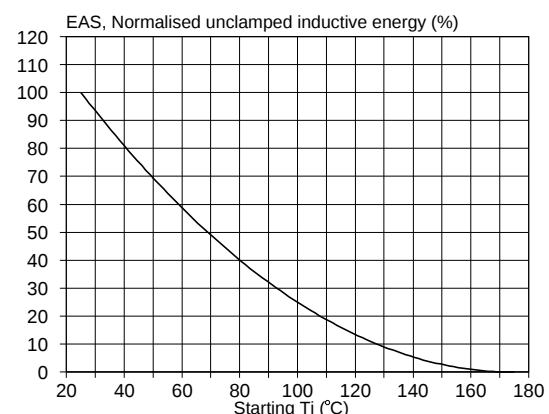


Fig.17. Normalised unclamped inductive energy.
 $E_{AS}\% = f(T_J)$

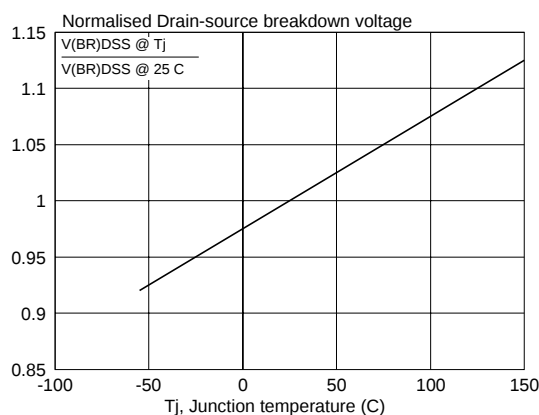


Fig.15. Normalised drain-source breakdown voltage.
 $V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_J)$

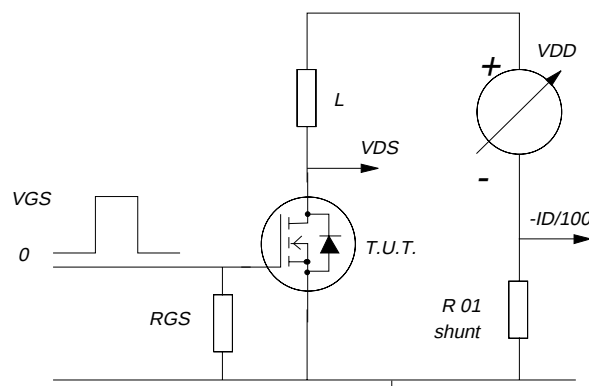
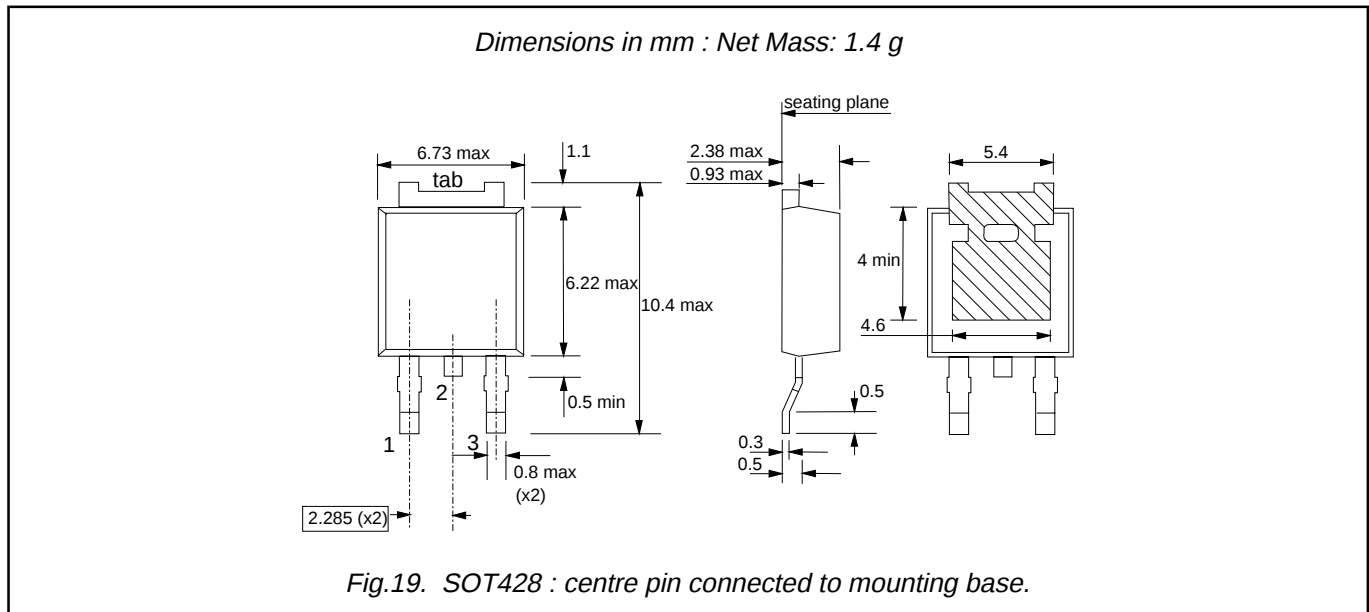


Fig.18. Unclamped inductive test circuit.
 $E_{AS} = 0.5 \cdot L I_D^2 \cdot V_{(BR)DSS} / (V_{(BR)DSS} - V_{DD})$

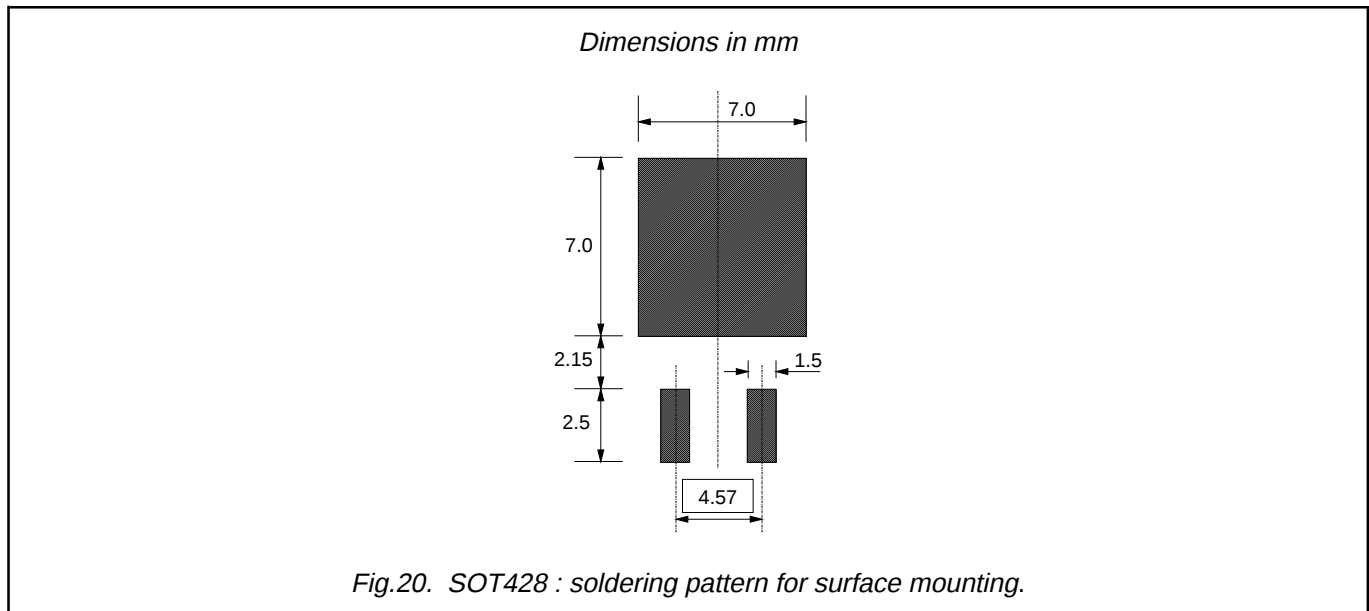
PowerMOS transistor Logic level FET

PHD3055L

MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

PowerMOS transistor
Logic level FET

PHD3055L

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 1997	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.