

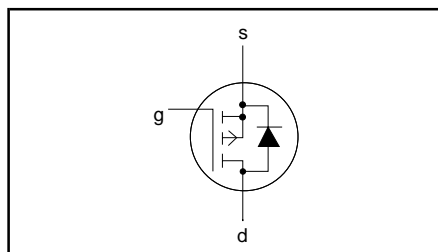
P-channel enhancement mode MOS transistor

PHK04P02T

FEATURES

- Very low threshold voltage
- Fast switching
- Logic level compatible
- Surface mount package

SYMBOL



QUICK REFERENCE DATA

$V_{DS} = -16 \text{ V}$
$I_D = -4.66 \text{ A}$
$R_{DS(ON)} \leq 0.15 \Omega (V_{GS} = -2.5 \text{ V})$
$V_{GS(TO)} \geq 0.4 \text{ V}$

GENERAL DESCRIPTION

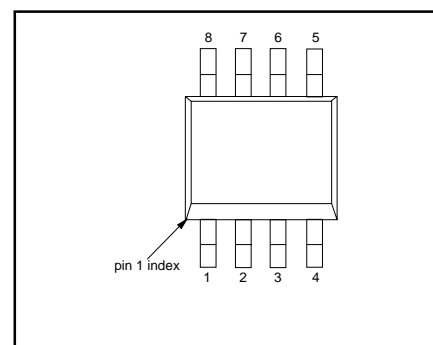
P-channel, enhancement mode, logic level, field-effect power transistor. This device has low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The PHK04P02T is supplied in the SOT96-1 (SO8) surface mounting package.

PINNING

PIN	DESCRIPTION
1,2,3	source
4	gate
5,6,7,8	drain

SOT96-1



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage		-	-16	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	-16	V
V_{GS}	Gate-source voltage		-	± 8	V
I_D	Drain current (DC)	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	-4.66	A
		$T_{sp} = 100 \text{ }^\circ\text{C}$	-	-1.87	A
I_{DM}	Drain current (pulse peak value)	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	-26.4	A
P_{tot}	Total power dissipation	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	5.0	W
		$T_{sp} = 100 \text{ }^\circ\text{C}$	-	2.0	W
T_{stg}, T_j	Storage & operating temperature		-55	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th \text{ j-sp}}$	Thermal resistance junction to solder point	mounted on metal clad substrate.	25	-	K/W

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ELECTRICAL CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = -10\ \mu\text{A}$	-16	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = -1\ \text{mA}$	-0.4	-0.6	-	V
		$T_j = 150^\circ\text{C}$	-0.1	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -1\ \text{A}$	-	80	120	$\text{m}\Omega$
		$V_{GS} = -2.5\text{ V}; I_D = -1\ \text{A}$	-	117	150	$\text{m}\Omega$
		$V_{GS} = -1.8\text{ V}; I_D = -0.5\ \text{A}$	-	140	180	$\text{m}\Omega$
		$V_{GS} = -2.5\text{ V}; I_D = -1\ \text{A}; T_j = 150^\circ\text{C}$	-	175	230	$\text{m}\Omega$
g_{fs}	Forward transconductance	$V_{DS} = -12.8\text{ V}; I_D = -1\ \text{A}$	1.5	4.5	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 8\text{ V}; V_{DS} = 0\ \text{V}$	-	± 10	± 100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = -12.8\text{ V}; V_{GS} = 0\ \text{V}; T_j = 150^\circ\text{C}$	-	-50	-100	nA
			-	-13	-100	μA
$Q_{g(\text{tot})}$	Total gate charge	$I_D = -1\ \text{A}; V_{DD} = -10\ \text{V}; V_{GS} = -4.5\ \text{V}$	-	7.2	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	1.83	-	nC
$t_{d\text{ on}}$	Turn-on delay time	$V_{DD} = -10\ \text{V}; I_D = -1\ \text{A};$	-	2	-	ns
t_r	Turn-on rise time	$V_{GS} = -8\ \text{V}; R_G = 6\ \Omega$	-	4.5	-	ns
$t_{d\text{ off}}$	Turn-off delay time	Resistive load	-	45	-	ns
t_f	Turn-off fall time		-	20	-	ns
C_{iss}	Input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = -12.8\ \text{V}; f = 1\ \text{MHz}$	-	528	-	pF
C_{oss}	Output capacitance		-	200	-	pF
C_{rss}	Feedback capacitance		-	57	-	pF

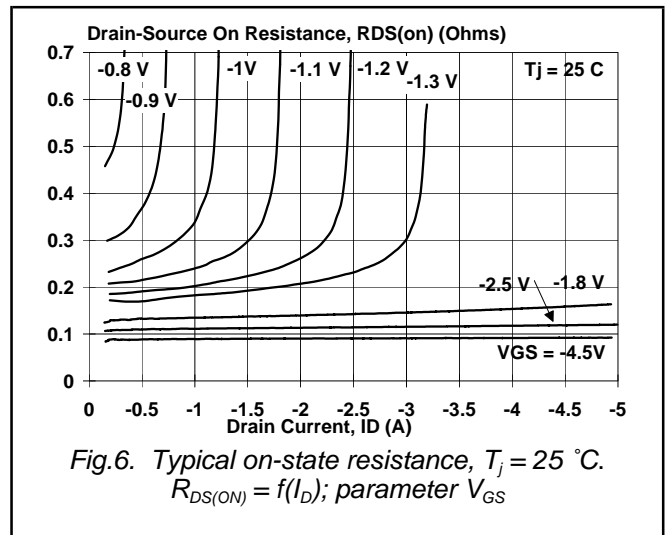
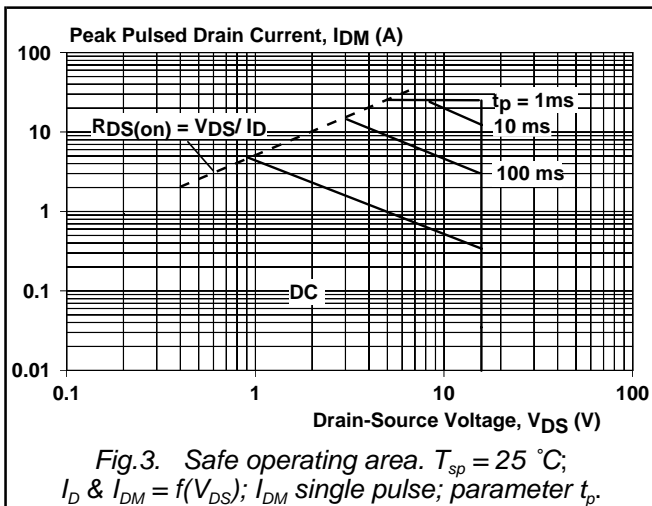
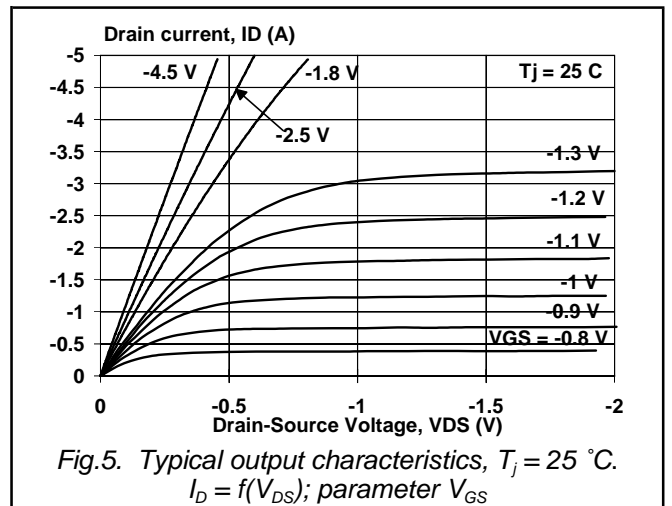
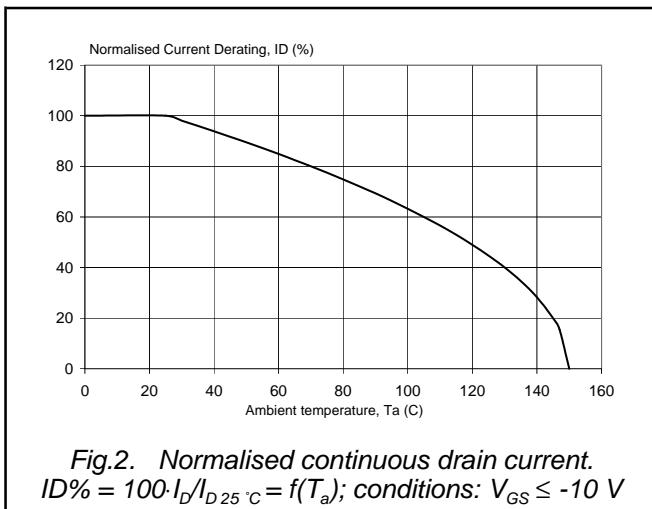
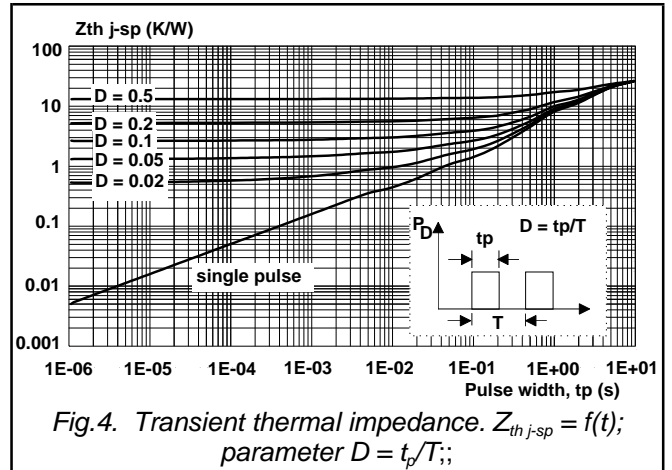
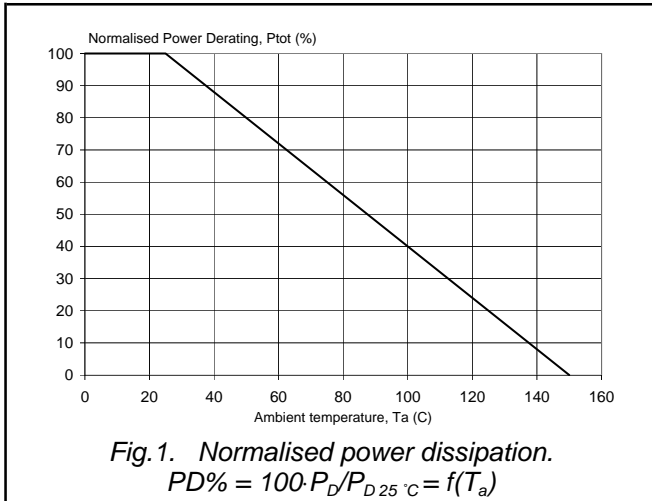
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	$T_{sp} = 25^\circ\text{C}, t \leq 5\ \text{s}$	-	-	-4.66	A
I_{DRM}	Pulsed reverse drain current		-	-	-26	A
V_{SD}	Diode forward voltage	$I_F = -0.62\ \text{A}; V_{GS} = 0\ \text{V}$	-	-0.62	-1.3	V
t_{rr}	Reverse recovery time	$I_F = -0.5\ \text{A}; -dI_F/dt = 100\ \text{A}/\mu\text{s};$	-	75	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\ \text{V}; V_R = -12.8\ \text{V}$	-	69	-	nC

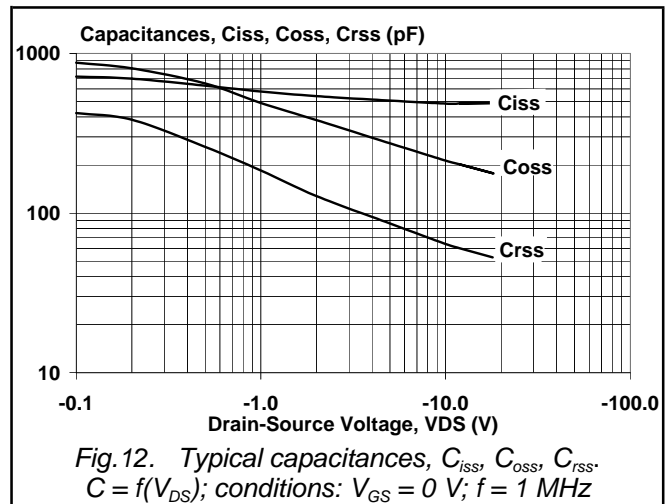
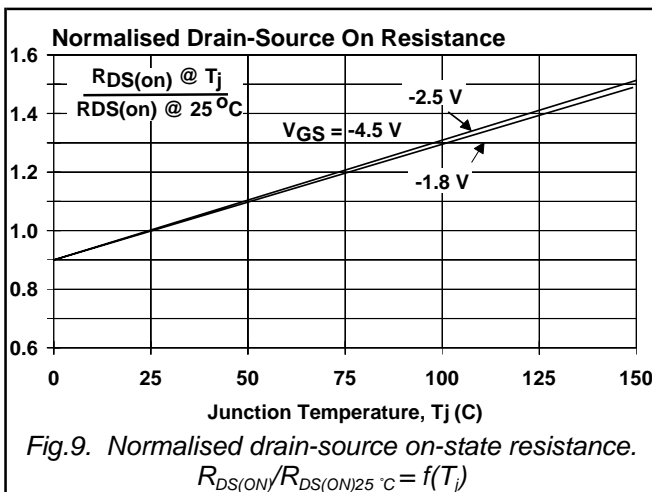
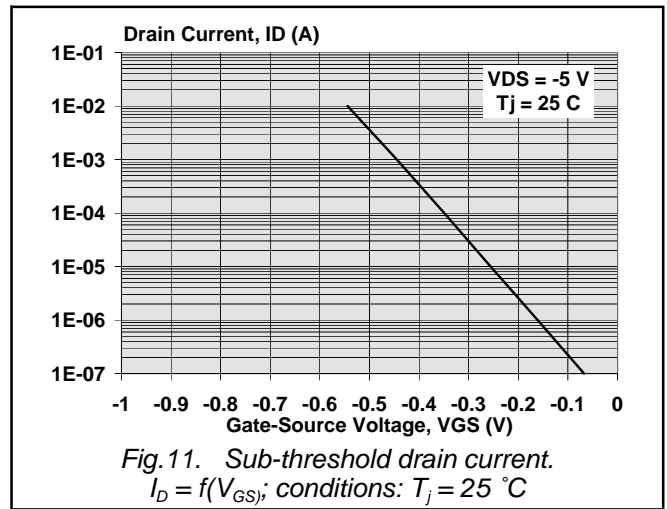
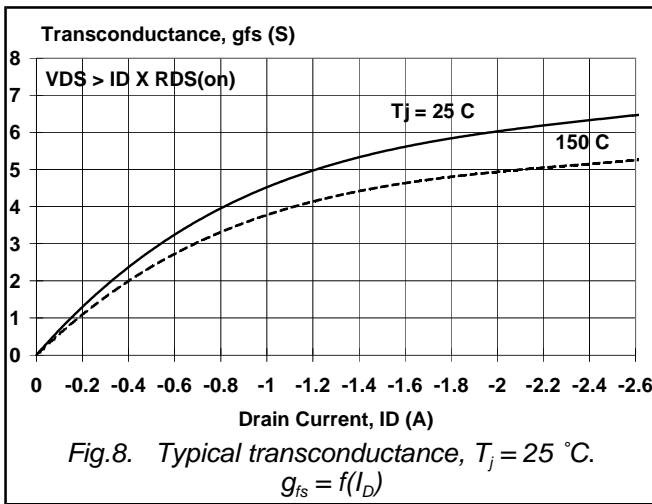
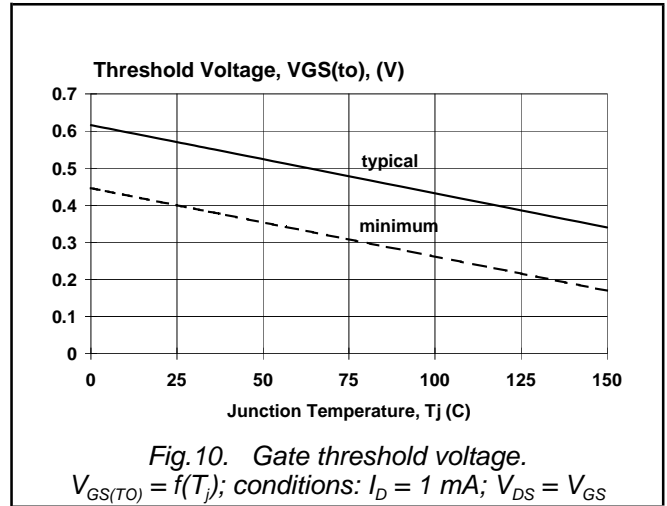
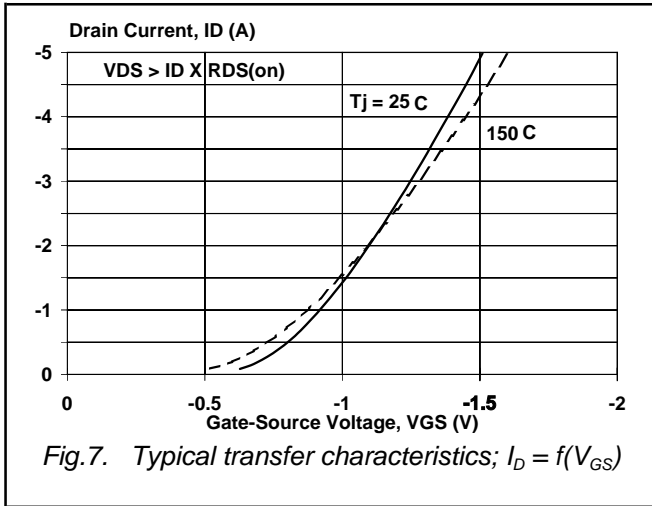
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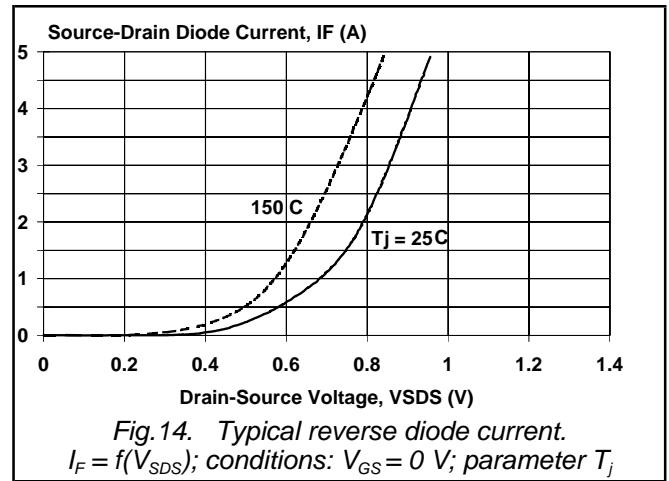
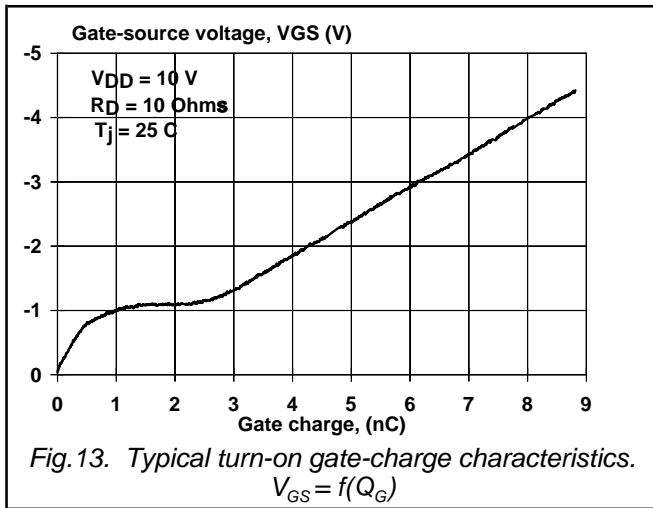
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MOS transistor

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P-channel enhancement mode
MOS transistor

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MECHANICAL DATA

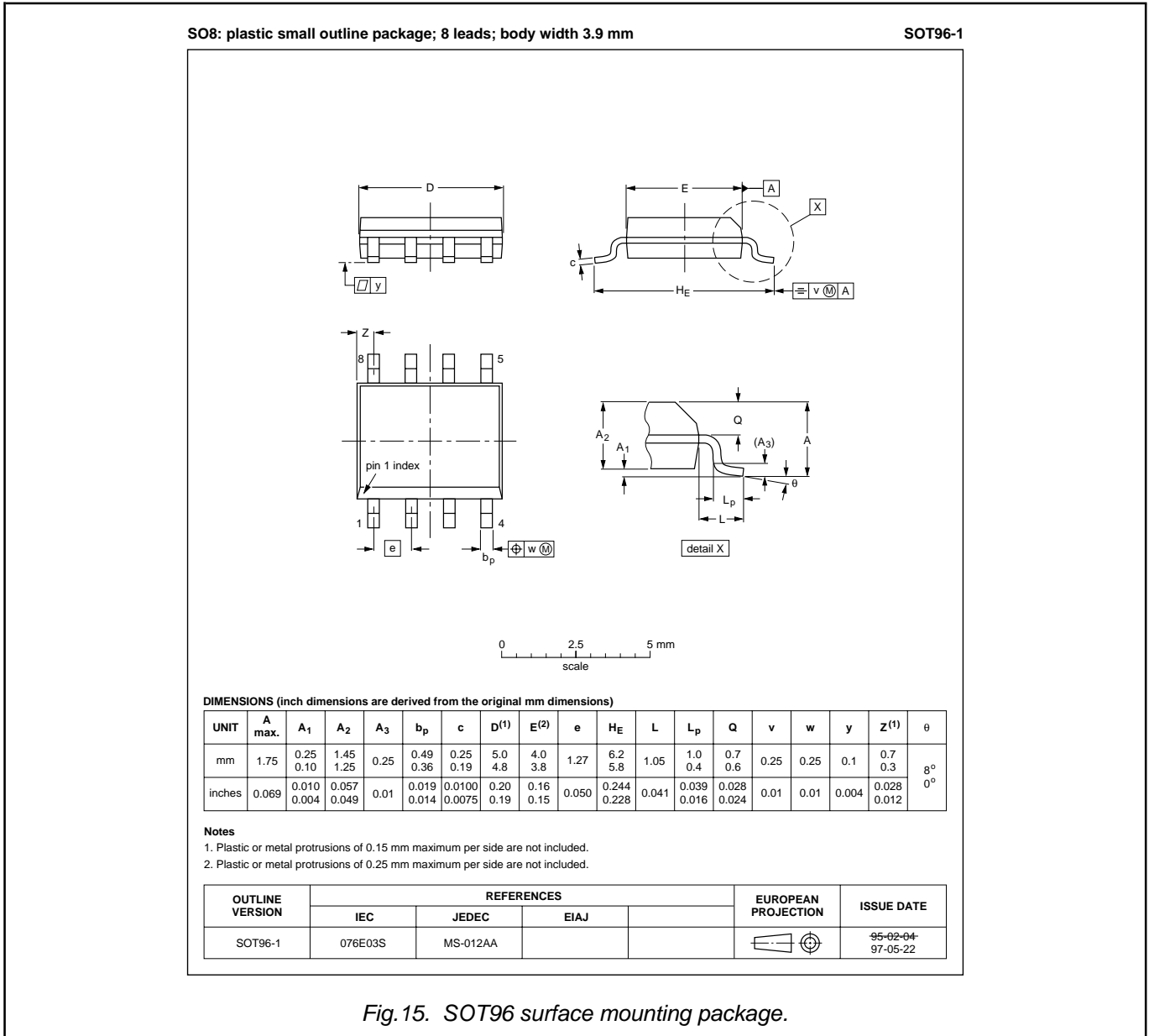


Fig. 15. SOT96 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS ¹	PRODUCT STATUS ²	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A
Limiting values		
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		
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