

# PHK12NQ03LT

TrenchMOS™ logic level FET

Rev. 01 — 22 March 2002

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™<sup>1</sup> technology.

Product availability:

PHK12NQ03LT in SOT96-1 (SO8).

### 1.2 Features

- Low on-state resistance
- Fast switching

### 1.3 Applications

- DC to DC converters
- Portable equipment applications

### 1.4 Quick reference data

- $V_{DS} = 30\text{ V}$
- $I_D = 12\text{ A}$
- $P_{tot} = 2.5\text{ W}$
- $R_{DS(on)} = 14\text{ m}\Omega$

## 2. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p style="text-align: center;">Top view MBK187</p> <p style="text-align: center;"><b>SOT96-1 (SO8)</b></p>	<p style="text-align: center;">MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.

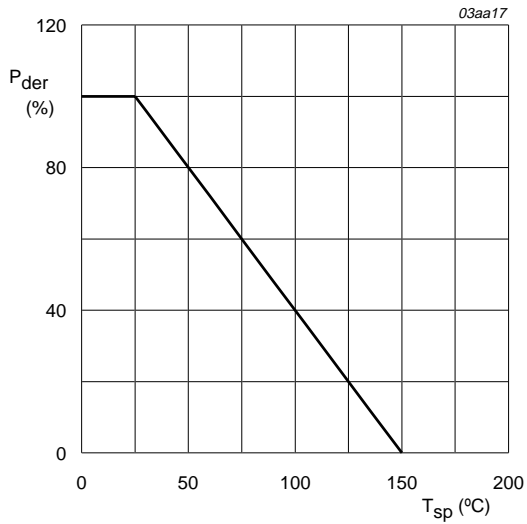


### 3. Limiting values

**Table 2: Limiting values**

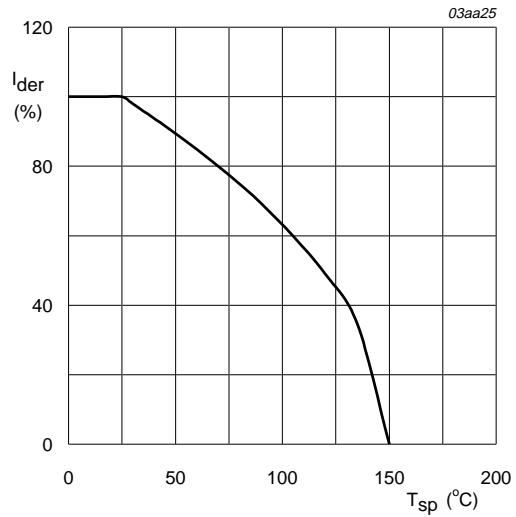
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $150$ °C	-	30	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current	$T_{sp} = 25$ °C; <b>Figure 2 and 3</b>	-	12	A
$I_{DM}$	peak drain current	$T_{sp} = 25$ °C; pulsed; <b>Figure 3</b>	-	45	A
$P_{tot}$	total power dissipation	$T_{sp} = 25$ °C; <b>Figure 1</b>	-	2.5	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	operating junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current	$T_{sp} = 25$ °C	-	12	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

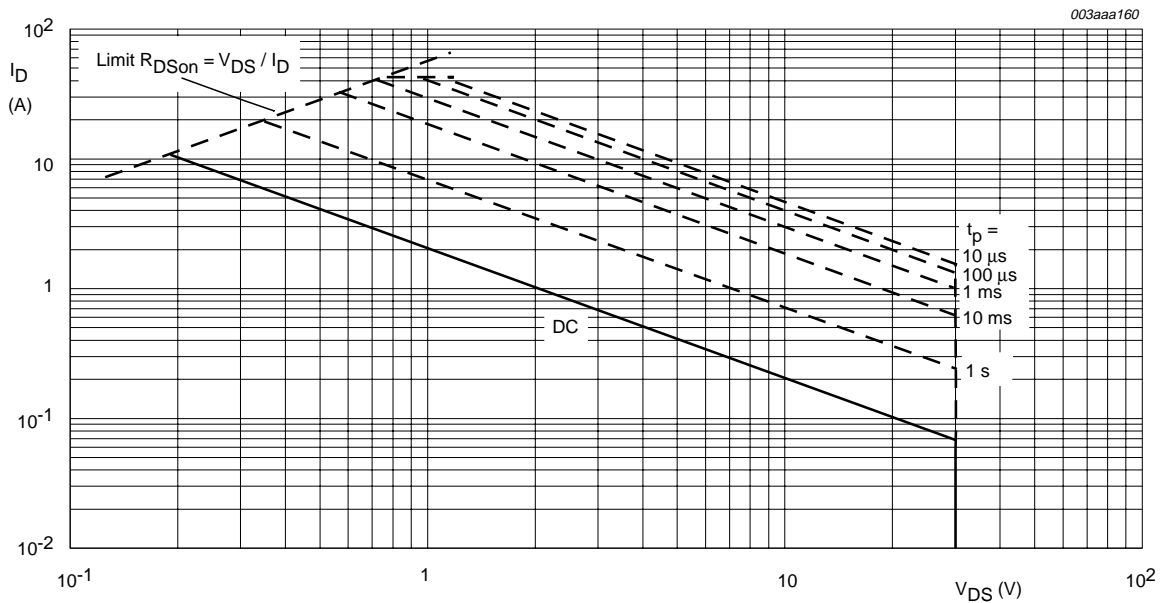
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

### 4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; $t_p \leq 10$ s; minimum footprint; Figure 4	-	60	-	K/W

#### 4.1 Transient thermal impedance

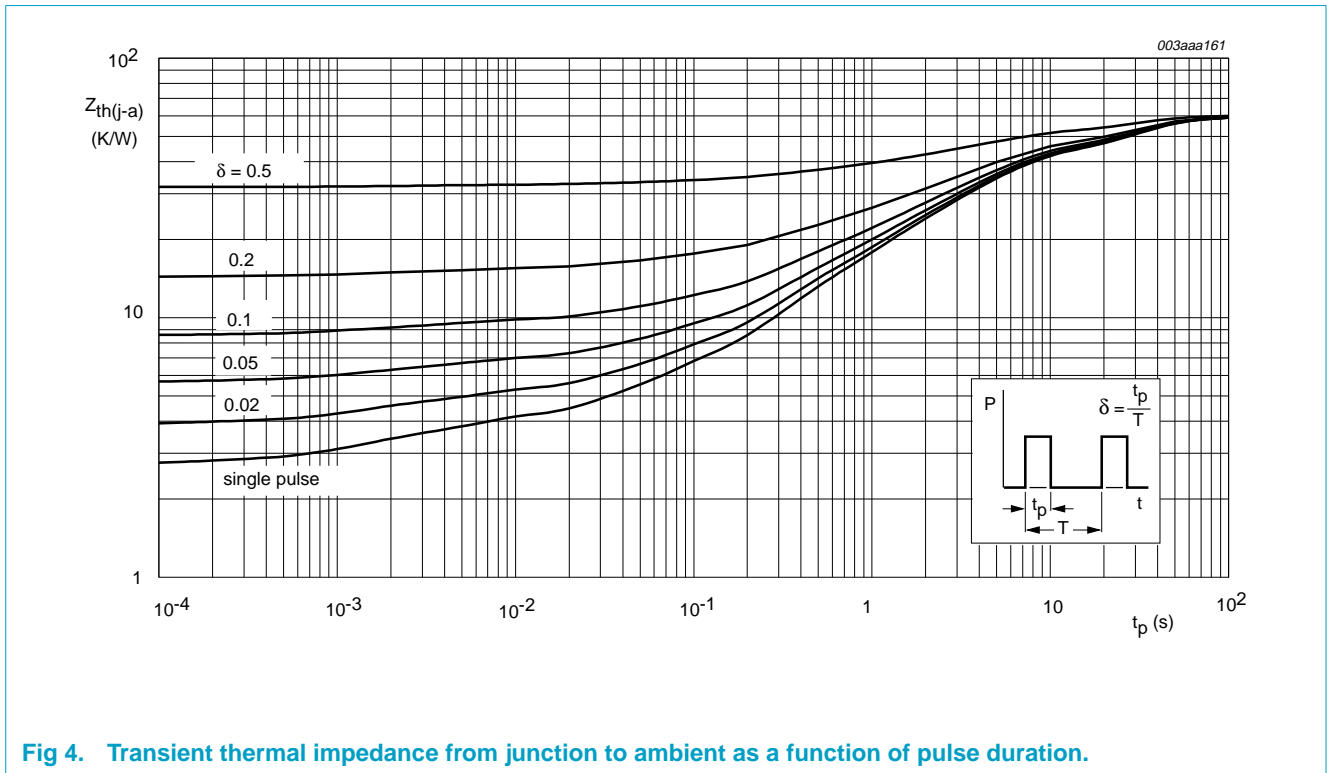
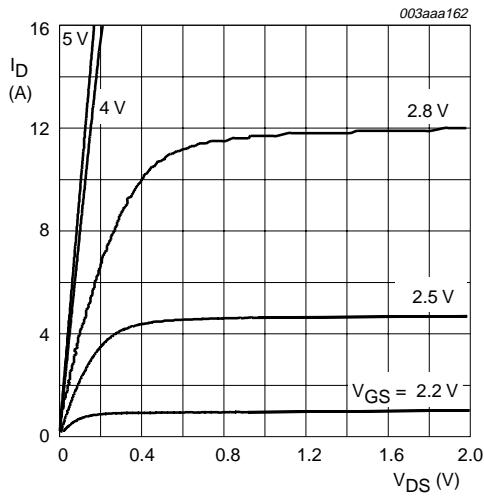


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

## 5. Characteristics

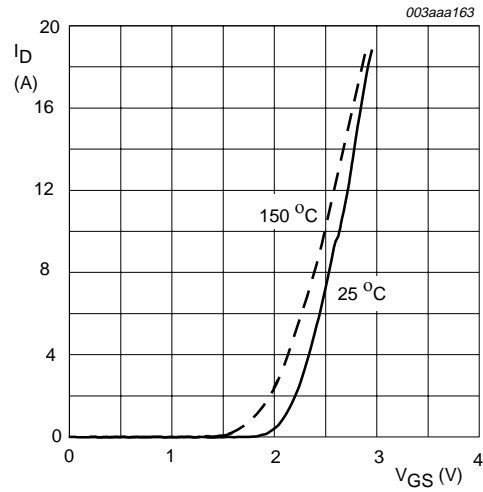
**Table 4: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V	30	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; <b>Figure 9</b>	1	-	2	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	-	-	1	μA
		T <sub>j</sub> = 100 °C	-	-	5	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±20 V; V <sub>DS</sub> = 0 V	-		100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A; <b>Figure 7 and 8</b>	-	11	14	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 12 A; <b>Figure 7 and 8</b>	-	8.9	10.5	mΩ
<b>Dynamic characteristics</b>						
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 10 A;	-	34	-	S
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 15 A; V <sub>DD</sub> = 16 V; V <sub>GS</sub> = 5 V; <b>Figure 13</b>	-	17.6	-	nC
Q <sub>gs</sub>	gate-source charge		-	4	-	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		-	4.4	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 16 V; f = 1 MHz; <b>Figure 11</b>	-	1335	-	pF
C <sub>oss</sub>	output capacitance		-	391	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	190	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 16 V; R <sub>D</sub> = 10 Ω; V <sub>GS</sub> = 10 V	-	10.6	-	ns
t <sub>r</sub>	rise time		-	11.7	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	37	-	ns
t <sub>f</sub>	fall time		-	19	-	ns
<b>Source-drain (reverse) diode</b>						
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 1 A; V <sub>GS</sub> = 0 V; <b>Figure 12</b>	-	0.7	1.0	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 2.3 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V	-	70	-	ns



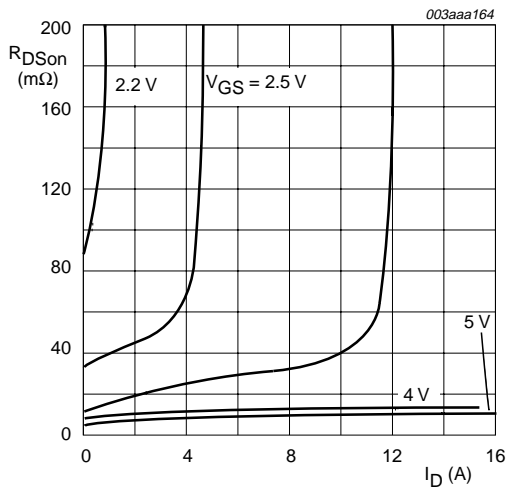
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



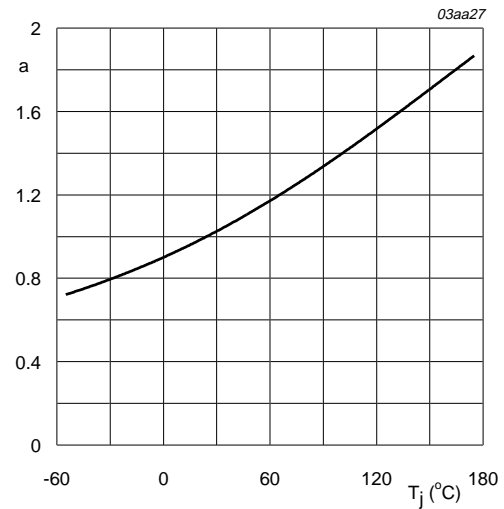
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



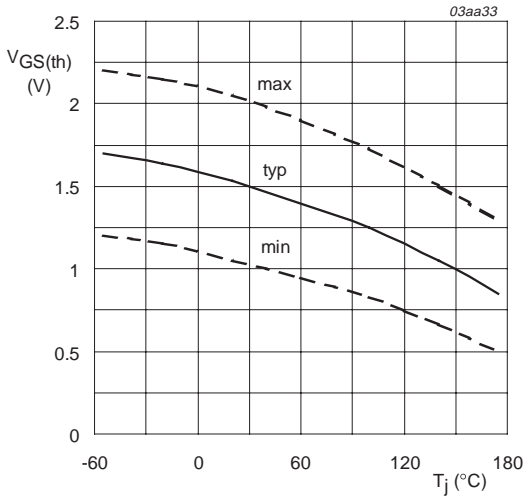
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



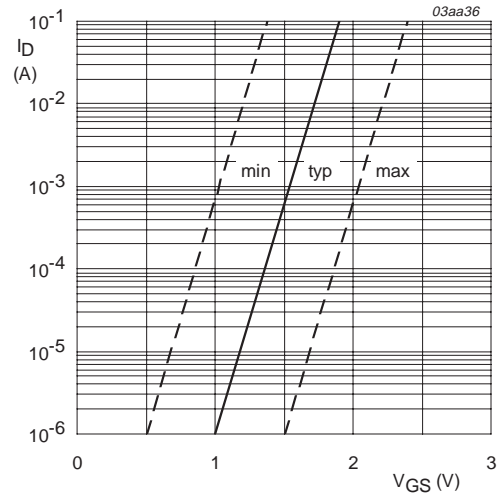
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



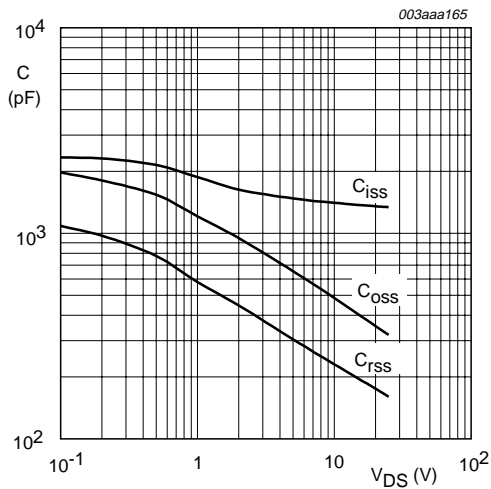
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



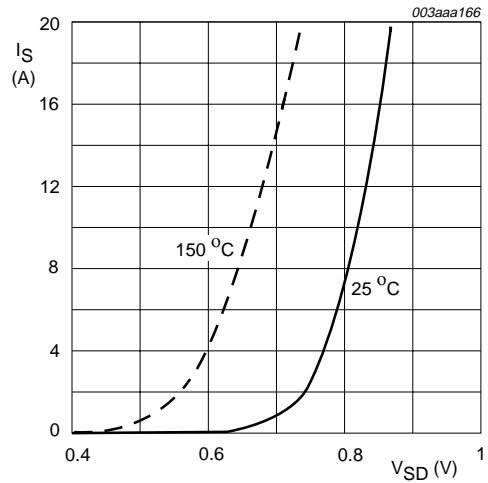
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



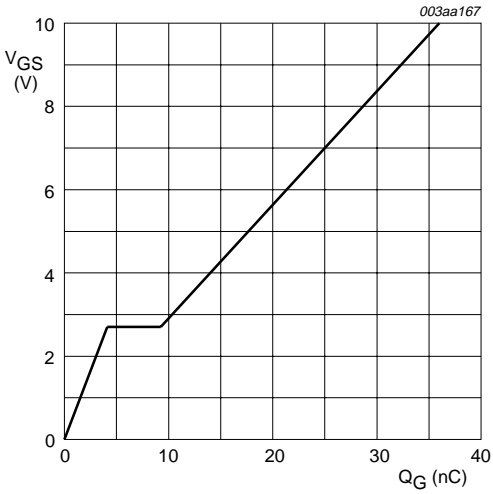
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



$T_j = 25 \text{ }^\circ\text{C}$  and  $150 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



I<sub>D</sub> = 15 A; V<sub>DD</sub> = 16 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

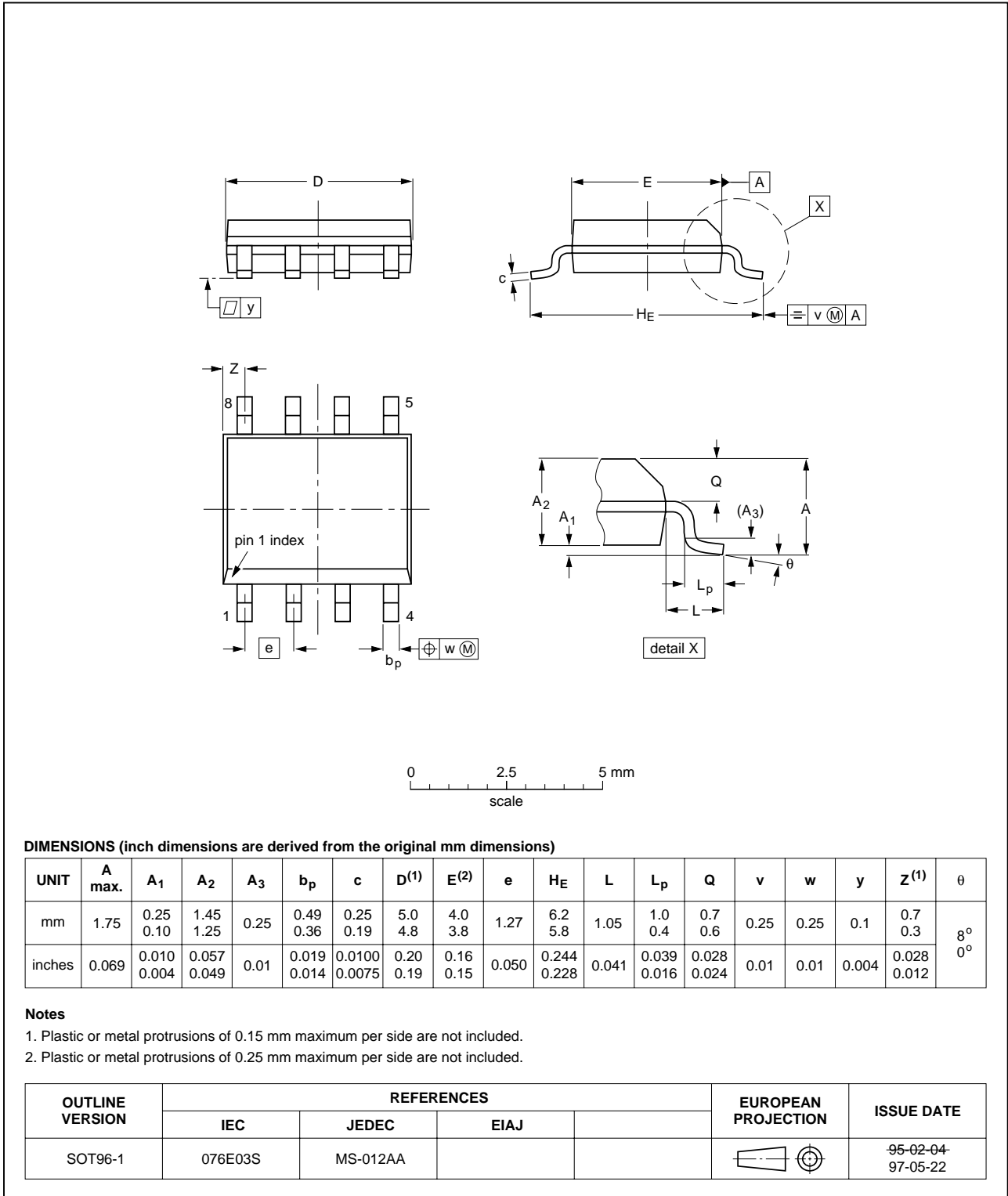


Fig 14. SOT96-1 (SO8).

## 7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20020322	-	Product data; initial version

## 8. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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