

DATA SHEET

PHP125

P-channel enhancement mode
MOS transistor

Product specification
Supersedes data of 1996 Apr 02
File under Discrete Semiconductors, SC13b

1997 Jun 18

P-channel enhancement mode
MOS transistor

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FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

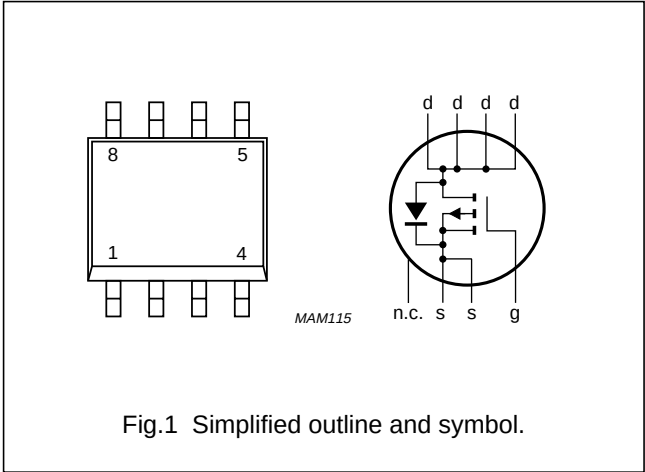
- Motor and actuator driver
- Power management
- Synchronized rectification.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.



CAUTION

The device is supplied in an antistatic package.
The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25\text{ A}$	–	–1.6	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1\text{ mA}; V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)	$T_s = 80\text{ °C}$	–	–2.5	A
R_{DSon}	drain-source on-state resistance	$I_D = -1\text{ A}; V_{GS} = -10\text{ V}$	–	0.25	Ω
P_{tot}	total power dissipation	$T_s = 80\text{ °C}$	–	2.8	W

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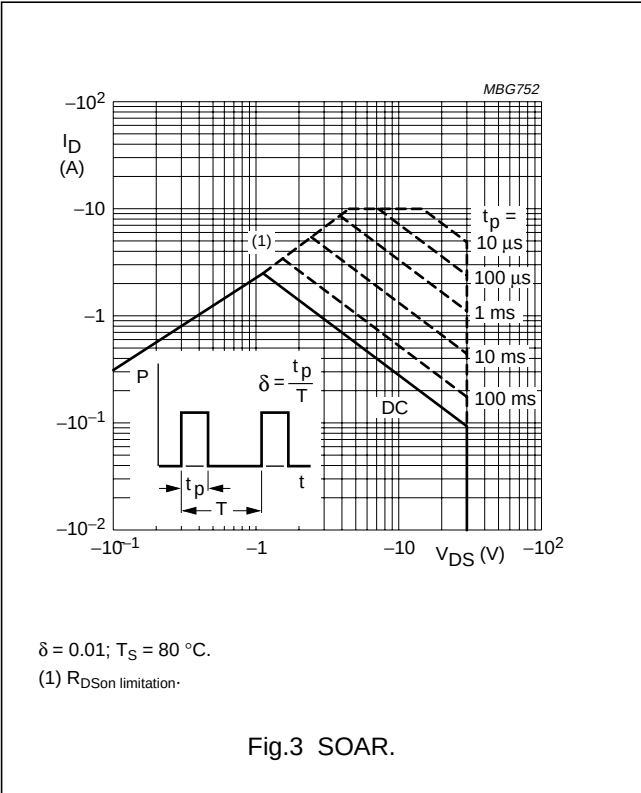
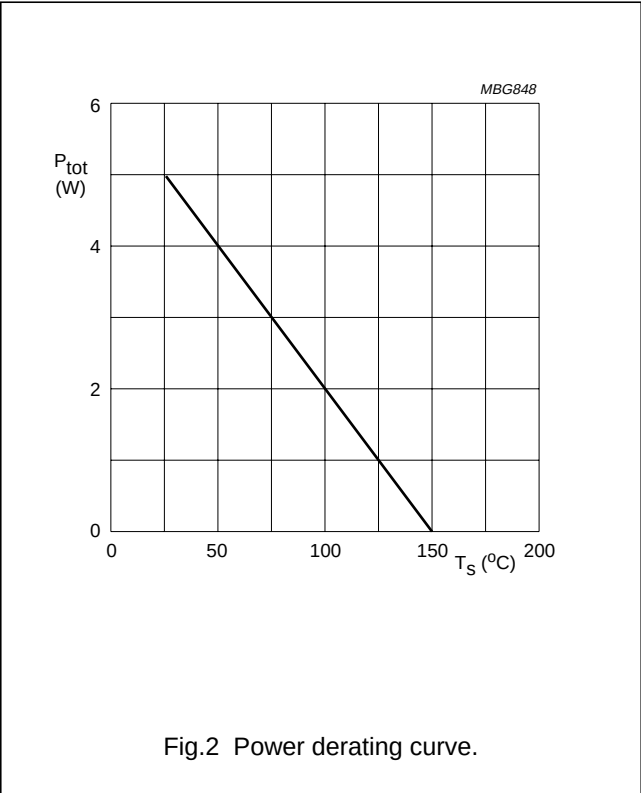
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage (DC)		–	–30	V
V _{GS}	gate-source voltage (DC)		–	±20	V
I _D	drain current (DC)	T _S = 80 °C; note 1	–	–2.5	A
I _{DM}	peak drain current	note 2	–	–10	A
P _{tot}	total power dissipation	T _S = 80 °C	–	2.8	W
		T _{amb} = 25 °C; note 3	–	2.4	W
		T _{amb} = 25 °C; note 4	–	1.1	W
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–65	+150	°C
Source-drain diode					
I _S	source current (DC)	T _S = 80 °C	–	–2	A
I _{SM}	peak pulsed source current	note 2	–	–8	A

Notes

1. T_S is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on a printed-circuit board with a R_{th a-tp} (ambient to tie-point) of 27.5 K/W.
4. Value based on a printed-circuit board with a R_{th a-tp} (ambient to tie-point) of 90 K/W.

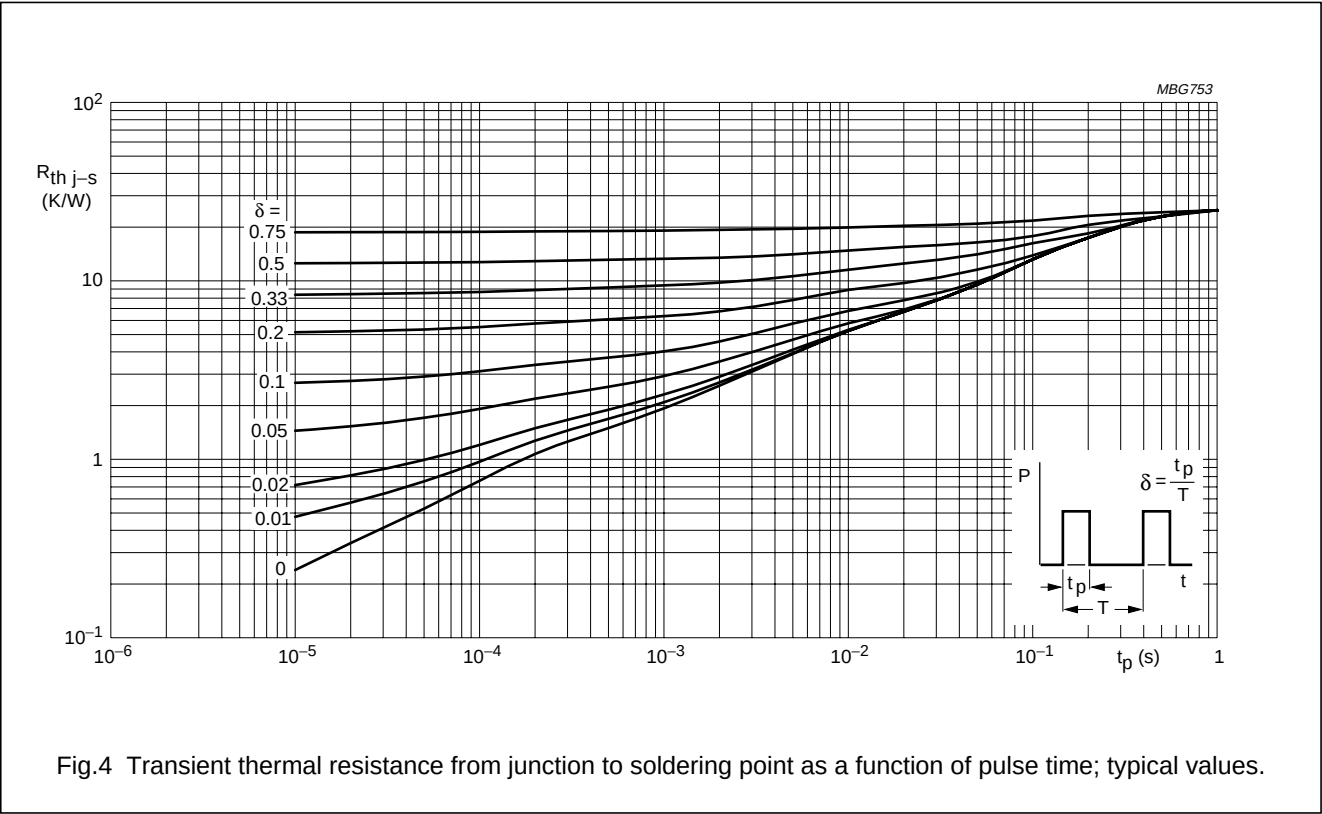


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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	25	K/W



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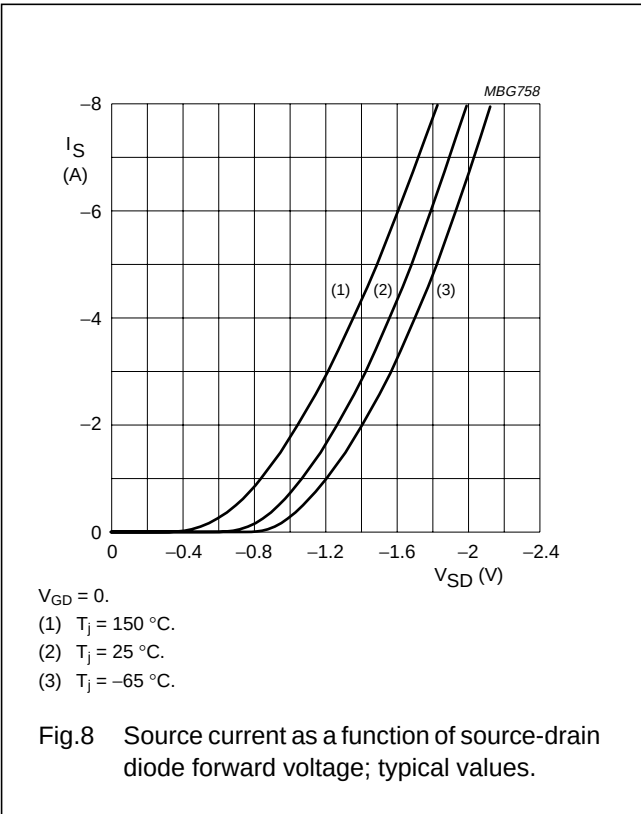
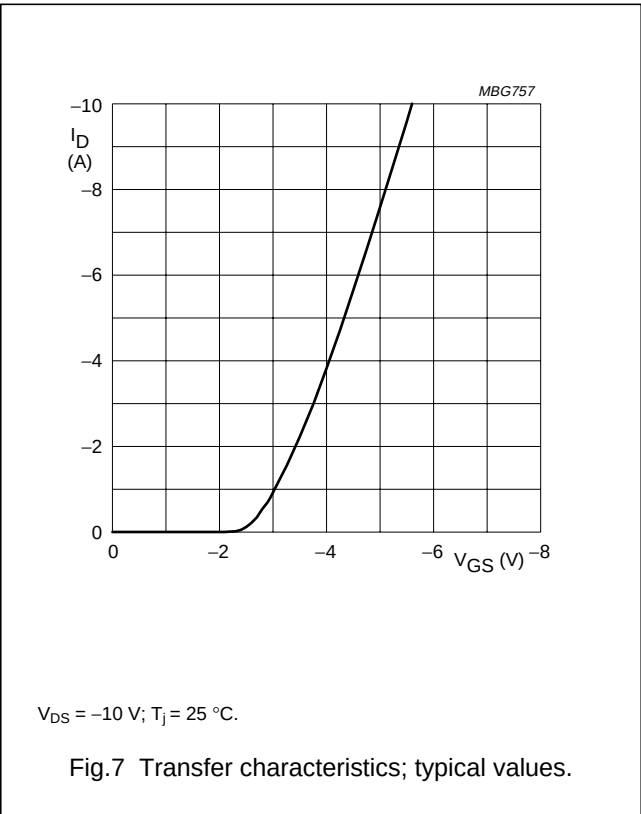
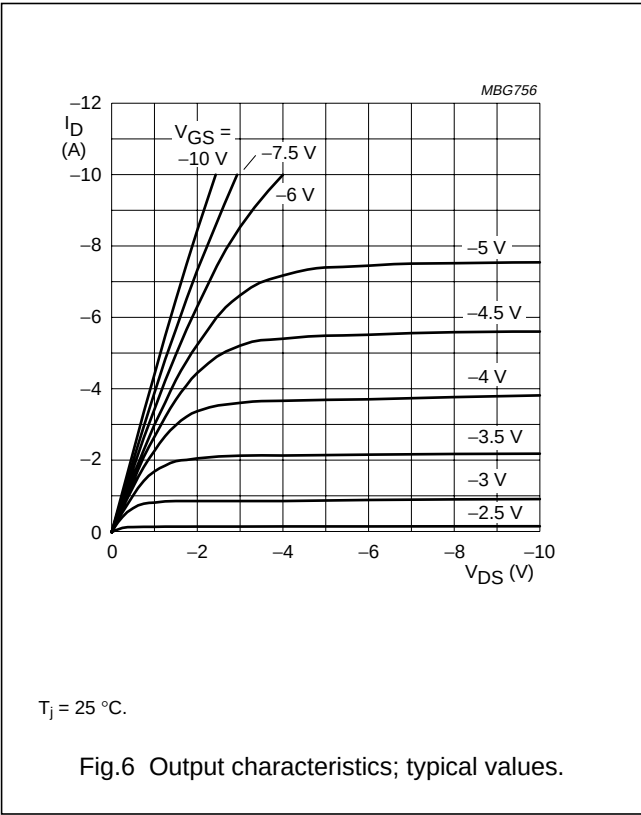
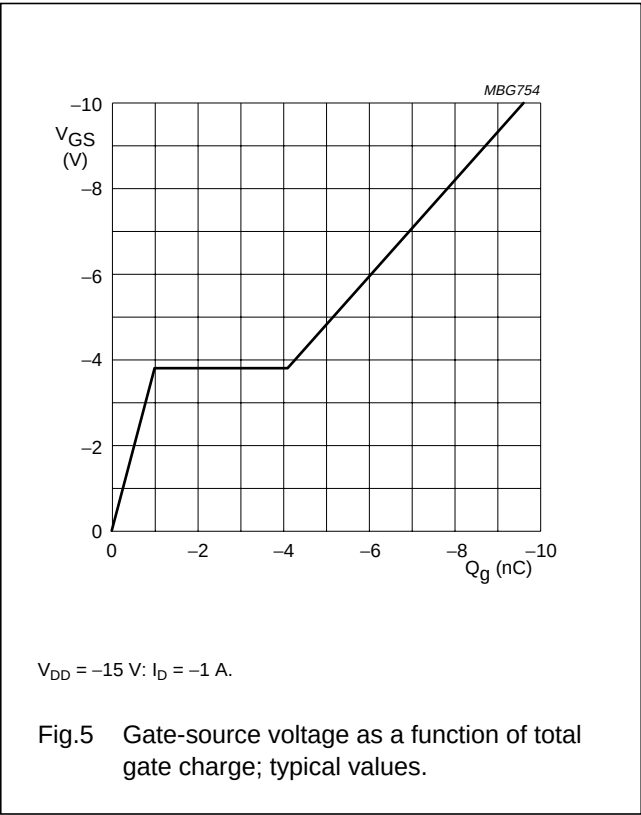
CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0; I _D = −10 μA	−30	−	−	V
V _{GSth}	gate-source threshold voltage	V _{GS} = V _{DS} ; I _D = −1 mA	−1	−	−2.8	V
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = −24 V	−	−	−100	nA
I _{GSS}	gate leakage current	V _{GS} = ±20 V; V _{DS} = 0	−	−	±100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = −4.5 V; I _D = −0.5 A	−	0.33	0.4	Ω
		V _{GS} = −10 V; I _D = −1 A	−	0.22	0.25	Ω
C _{iss}	input capacitance	V _{GS} = 0; V _{DS} = −24 V; f = 1 MHz	−	250	−	pF
C _{oss}	output capacitance	V _{GS} = 0; V _{DS} = −24 V; f = 1 MHz	−	140	−	pF
C _{rss}	reverse transfer capacitance	V _{GS} = 0; V _{DS} = −24 V; f = 1 MHz	−	50	−	pF
Q _G	total gate charge	V _{GS} = −10 V; V _{DS} = −15 V; I _D = −1 A	−	10	25	nC
Q _{GS}	gate-source charge	V _{GS} = −10 V; V _{DS} = −15 V; I _D = −1 A	−	1	−	nC
Q _{GD}	gate-drain charge	V _{GS} = −10 V; V _{DS} = −15 V; I _D = −1 A	−	3	−	nC
Switching times (see Fig.11)						
t _{d(on)}	turn-on delay time	V _{GS} = 0 to −10 V; V _{DD} = −15 V; I _D = −1 A; R _L = 15 Ω; R _{gen} = 6 Ω	−	4.5	−	ns
t _f	fall time		−	3.5	−	ns
t _{on}	turn-on switching time		−	8	16	ns
t _{d(off)}	turn-off delay time	V _{GS} = −10 to 0 V; V _{DD} = −15 V; I _D = −1 A; R _L = 15 Ω; R _{gen} = 6 Ω	−	25	−	ns
t _r	rise time		−	15	−	ns
t _{off}	turn-off switching time		−	40	80	ns
Source-drain diode						
V _{SD}	source-drain forward voltage	V _{GD} = 0; I _S = −1.25 A	−	−	−1.6	V
t _{rr}	reverse recovery time	I _S = −1.25 A; di/dt = 100 A/μs	−	150	200	ns

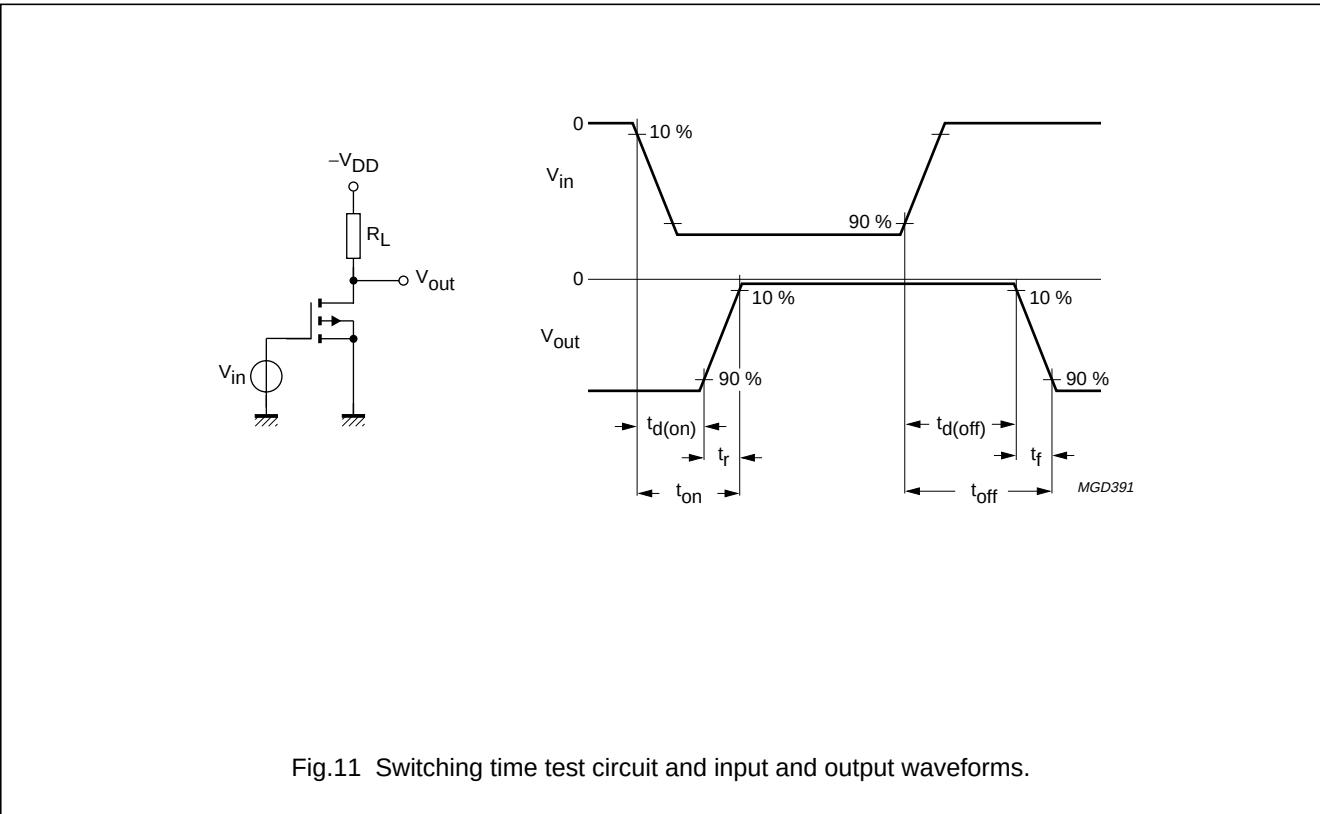
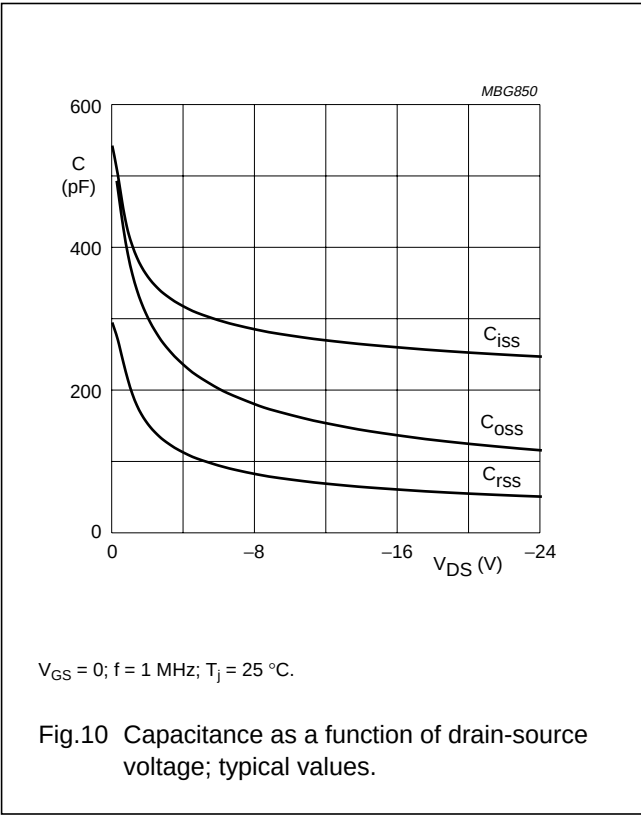
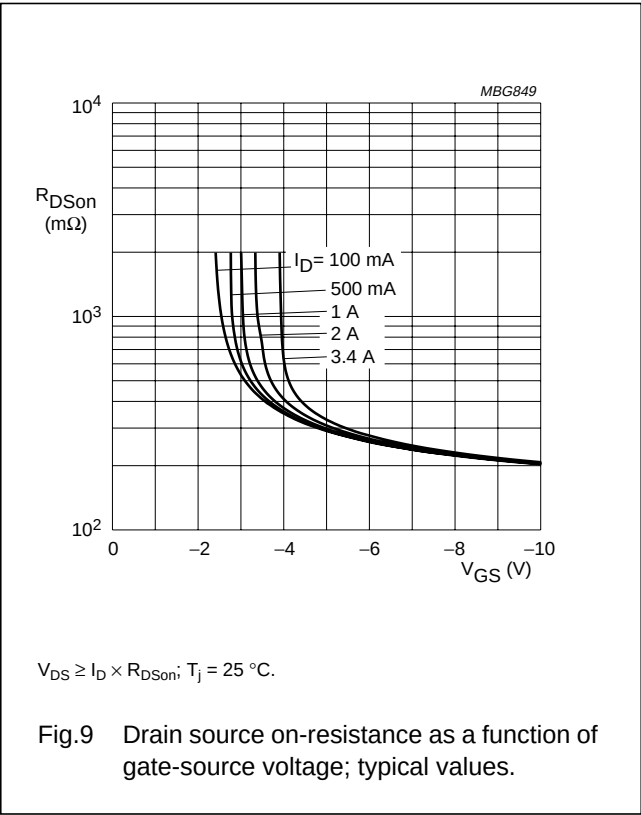
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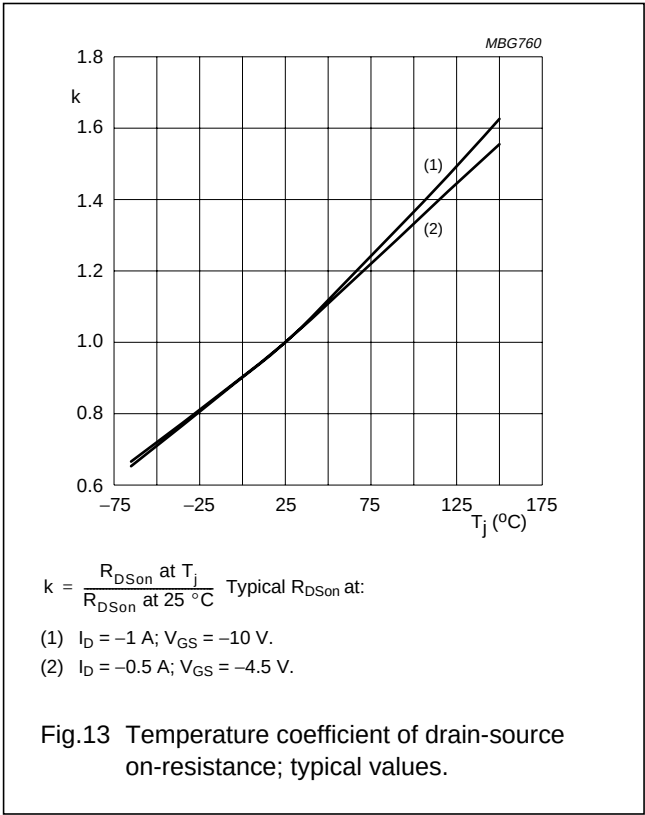
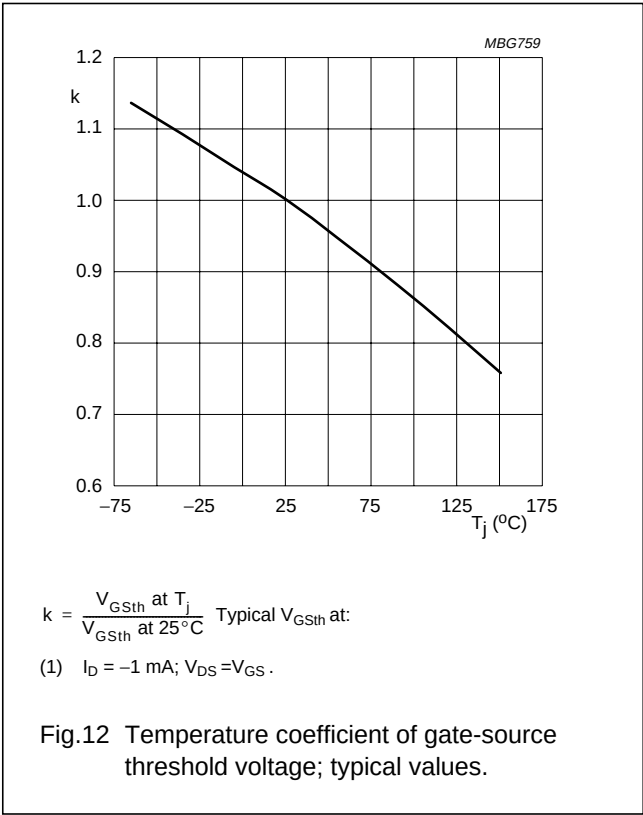
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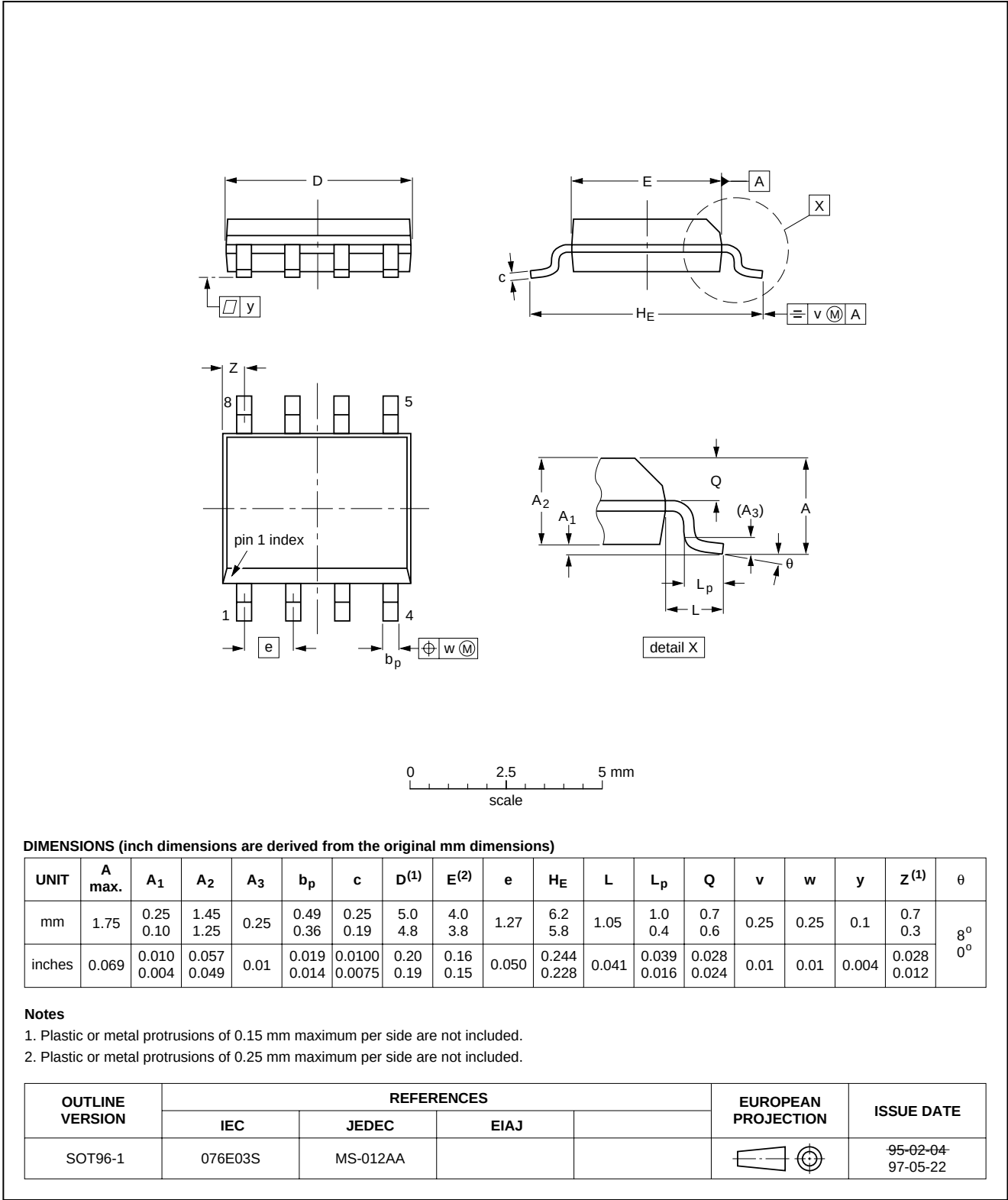
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PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



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PHP125**DEFINITIONS**

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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