

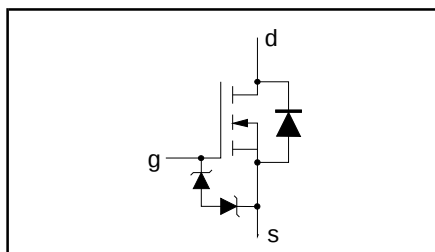
TrenchMOS™ transistor Logic level FET

PHP130N03LT, PHB130N03LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 30\text{ V}$
$I_D = 75\text{ A}$
$R_{DS(ON)} \leq 6\text{ m}\Omega$ ($V_{GS} = 5\text{ V}$)
$R_{DS(ON)} \leq 5\text{ m}\Omega$ ($V_{GS} = 10\text{ V}$)

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

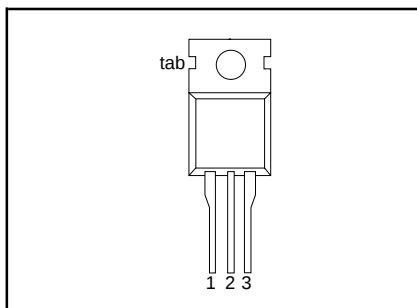
The PHP130N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.

The PHB130N03LT is supplied in the SOT404 surface mounting package.

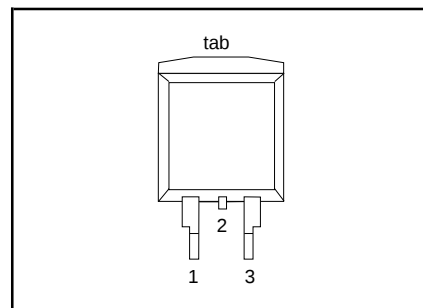
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

SOT78 (TO220AB)



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$ to $175\text{ }^{\circ}\text{C}$	-	30	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^{\circ}\text{C}$ to $175\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 5\text{ V}$	-	75	A
		$T_{mb} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 5\text{ V}$	-	75	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	240	A
P_D	Total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	187	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	$^{\circ}\text{C}$

¹ It is not possible to make connection to pin 2 of the SOT404 package.

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ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	0.8	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air	-	60	-	K/W
		SOT404 package, pcb mounted, minimum footprint	-	50	-	K/W

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.25\text{ mA}$; $T_j = -55^\circ\text{C}$	30 27	- -	- -	V V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = 1\text{ mA}$	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\text{ mA}$; $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1 0.5 -	1.5 - -	2 - 2.3	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$ $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$ $V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 175^\circ\text{C}$	- - -	5 4.5 -	6 5 11	mΩ mΩ mΩ
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}$; $I_D = 25\text{ A}$	20	40	-	S
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 5\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 175^\circ\text{C}$	-	0.02	1	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175^\circ\text{C}$	-	0.05	10	μA
$Q_{g(tot)}$	Total gate charge	$I_D = 75\text{ A}$; $V_{DD} = 24\text{ V}$; $V_{GS} = 5\text{ V}$	-	92	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	36	-	nC
t_{don}	Turn-on delay time	$V_{DD} = 15\text{ V}$; $I_D = 25\text{ A}$;	-	45	60	ns
t_r	Turn-on rise time	$V_{GS} = 5\text{ V}$; $R_G = 5\ \Omega$	-	120	170	ns
t_{doff}	Turn-off delay time	Resistive load	-	225	300	ns
t_f	Turn-off fall time		-	100	135	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$	-	5000	-	pF
C_{oss}	Output capacitance		-	1150	-	pF
C_{rss}	Feedback capacitance		-	500	-	pF

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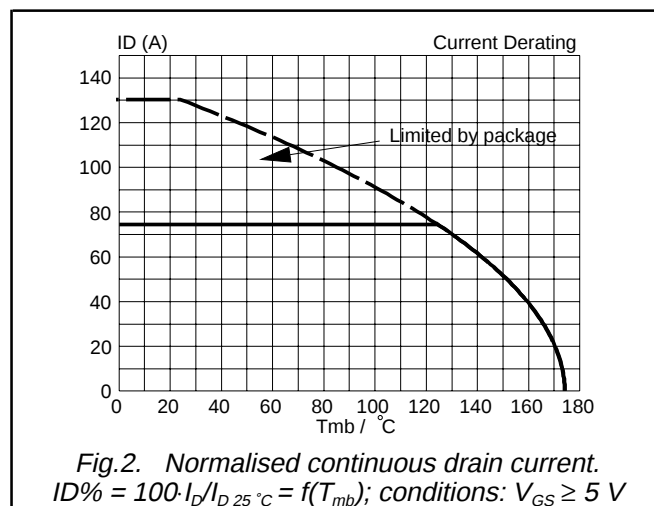
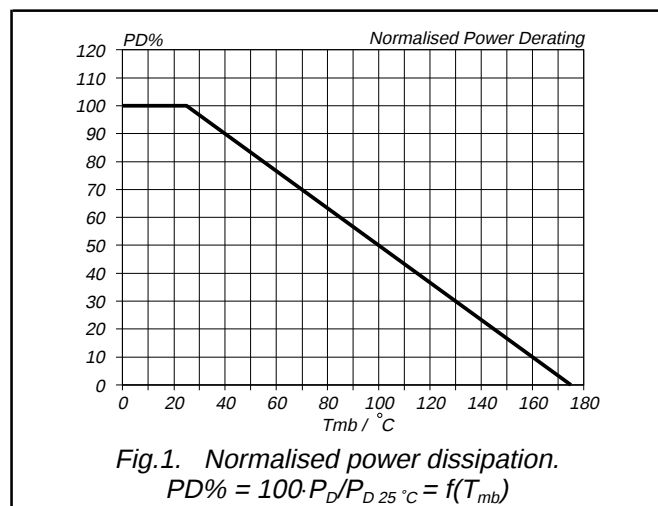
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)		-	-	75	A
I _{SM}	Pulsed source current (body diode)		-	-	240	A
V _{SD}	Diode forward voltage	I _F = 25 A; V _{GS} = 0 V I _F = 75 A; V _{GS} = 0 V	-	0.85 1.0	1.2 -	V
t _{rr}	Reverse recovery time	I _F = 75 A; -dI _F /dt = 100 A/μs; V _{GS} = -10 V; V _R = 25 V	-	100	-	ns
Q _{rr}	Reverse recovery charge		-	0.6	-	μC

AVALANCHE LIMITING VALUE

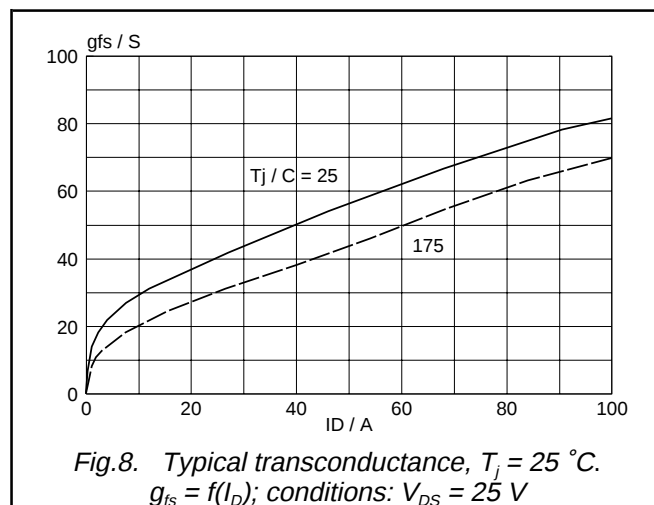
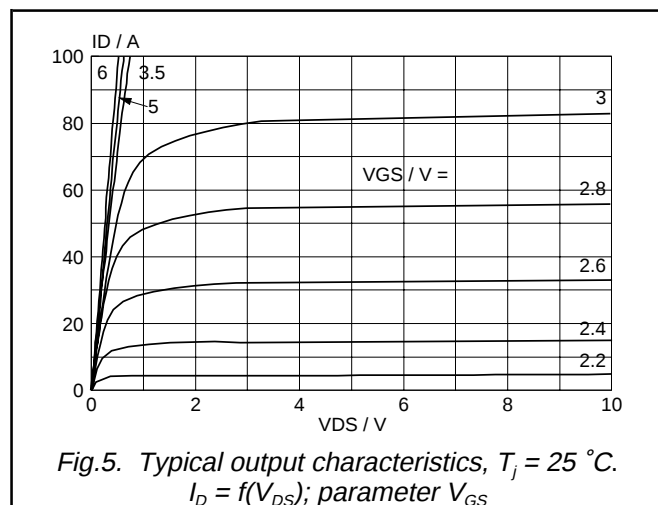
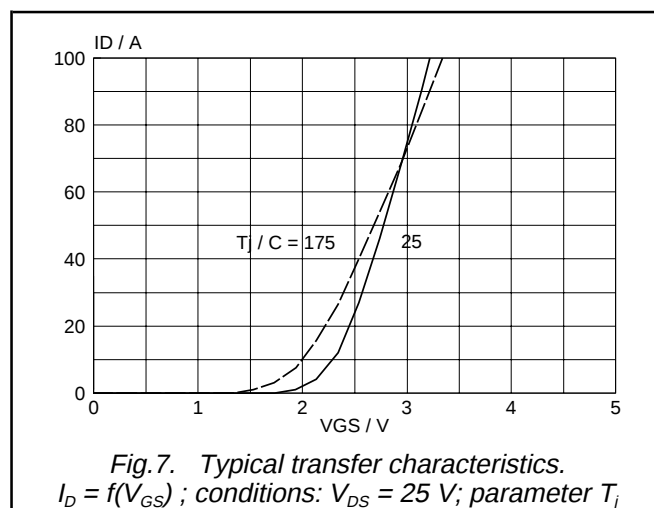
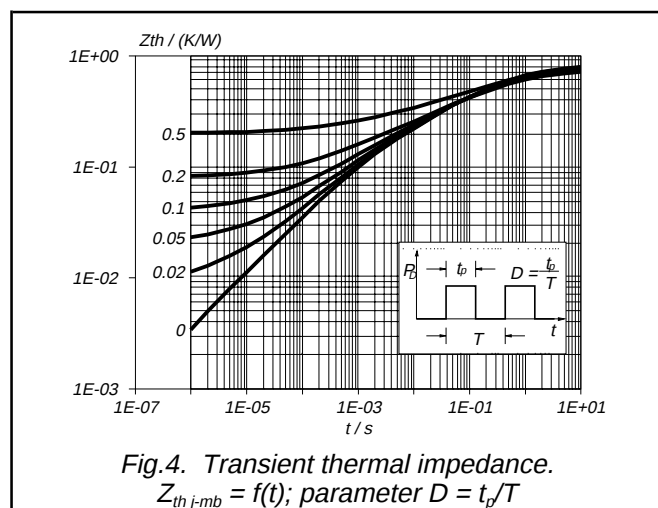
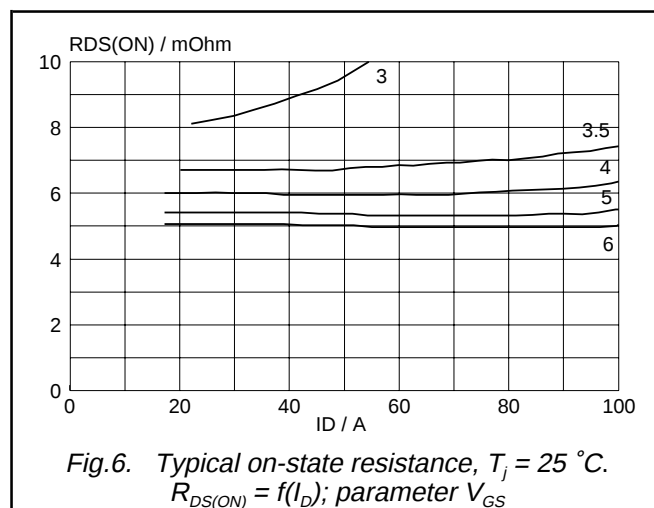
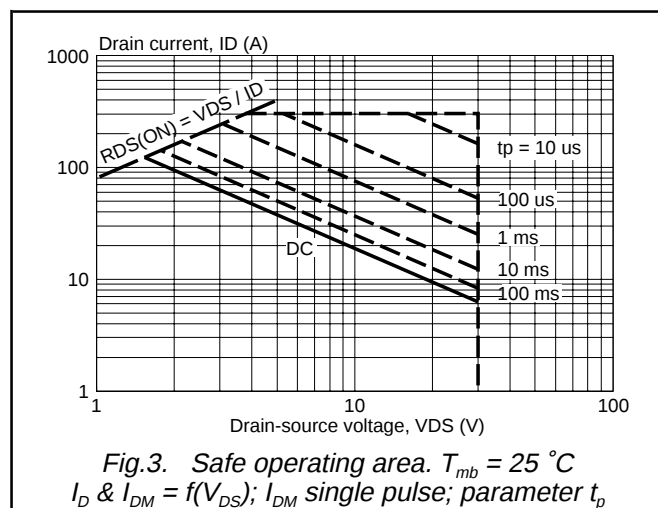
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W _{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I _D = 75 A; V _{DD} ≤ 15 V; V _{GS} = 5 V; R _{GS} = 50 Ω; T _{mb} = 25 °C	-	500	mJ



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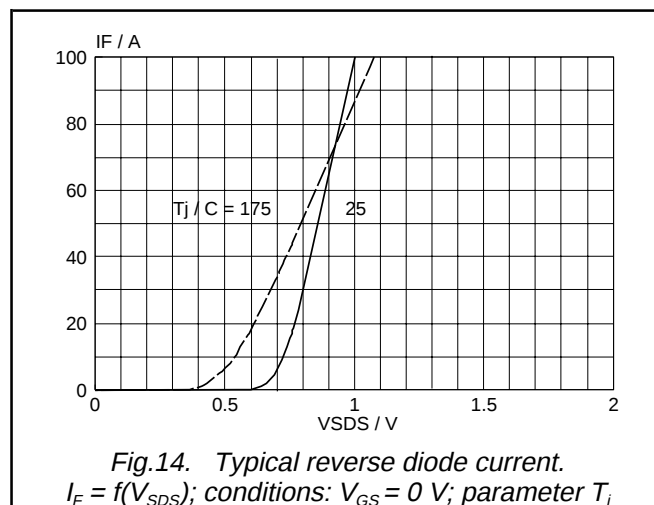
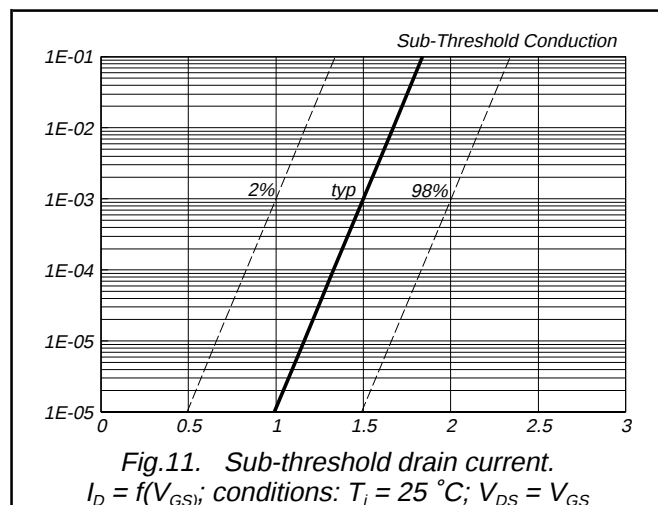
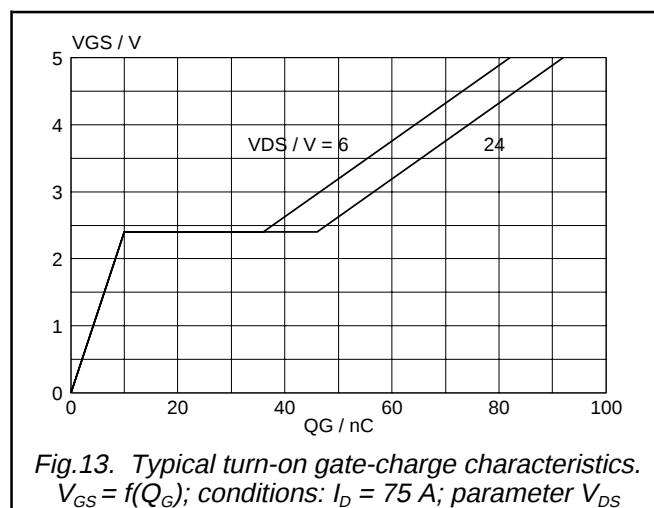
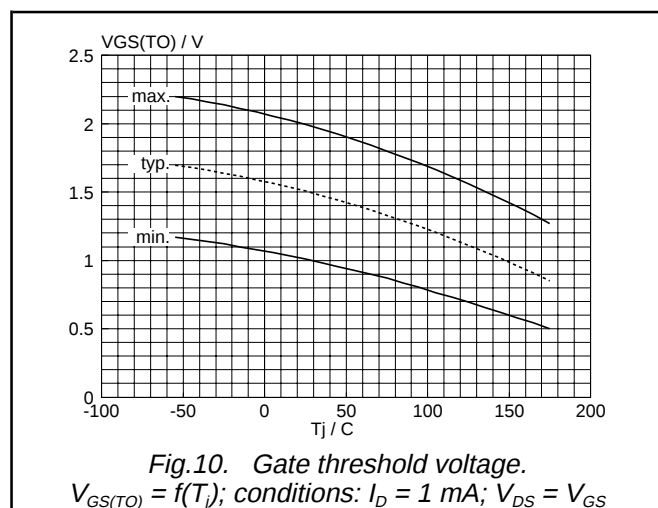
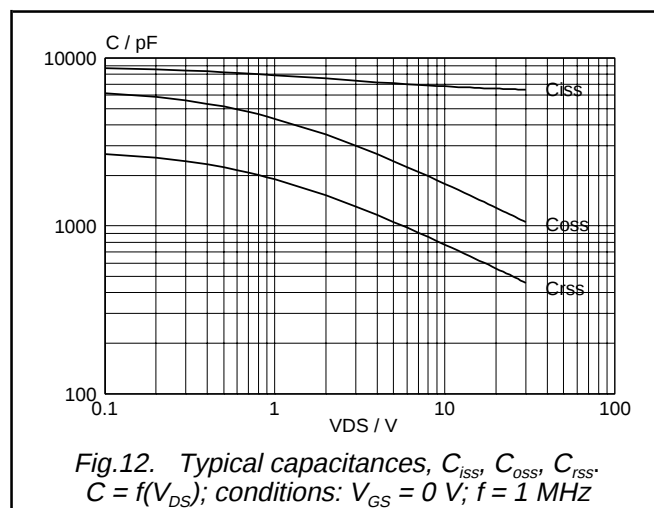
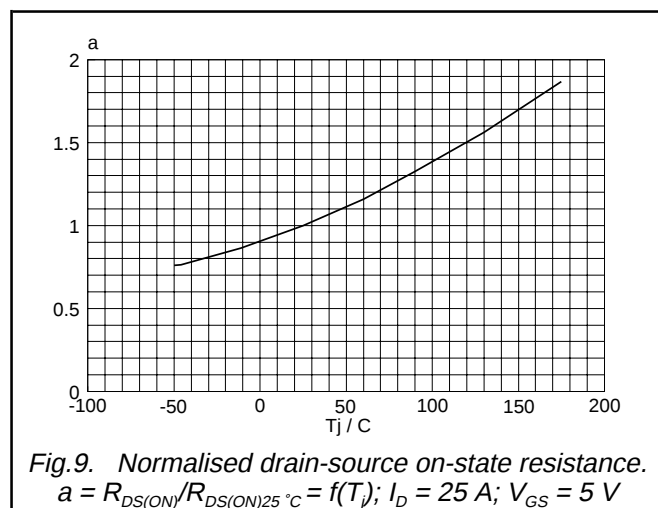
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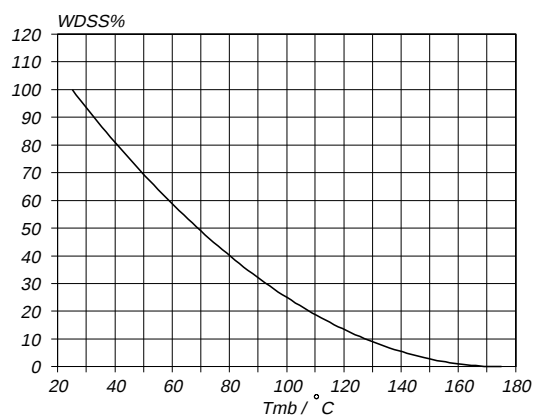


Fig.15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75\text{ A}$

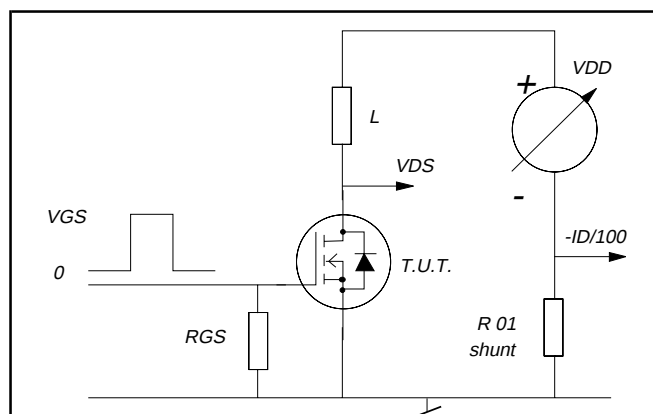


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$$