

# DATA SHEET

## **PHP212L**

Dual P-channel enhancement  
mode MOS transistor

Objective specification  
File under Discrete Semiconductors, SC13b

1997 Jun 20

# Dual P-channel enhancement mode MOS transistor

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## FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance
- Low threshold.

## APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

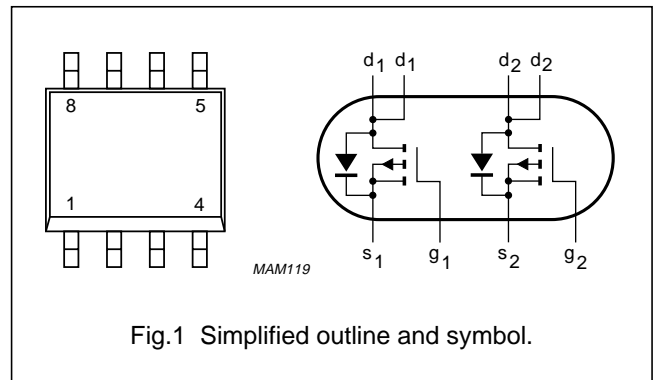
## DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

<b>CAUTION</b>
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

## PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s <sub>1</sub>	source 1
2	g <sub>1</sub>	gate 1
3	s <sub>2</sub>	source 2
4	g <sub>2</sub>	gate 2
5	d <sub>2</sub>	drain 2
6	d <sub>2</sub>	drain 2
7	d <sub>1</sub>	drain 1
8	d <sub>1</sub>	drain 1



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage (DC)		–	–30	V
V <sub>SD</sub>	source-drain diode forward voltage	I <sub>S</sub> = –1.25 A	–	–1.3	V
V <sub>GS</sub>	gate-source voltage (DC)		–	±12	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = –1 mA; V <sub>DS</sub> = V <sub>GS</sub>	–0.5	–1.1	V
I <sub>D</sub>	drain current (DC)	T <sub>S</sub> = 80 °C	–	–4	A
R <sub>DSon</sub>	drain-source on-state resistance	I <sub>D</sub> = –2 A; V <sub>GS</sub> = –4.5 V	–	0.12	Ω
P <sub>tot</sub>	total power dissipation	T <sub>S</sub> = 80 °C	–	3.5	W

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per P-channel</b>					
$V_{DS}$	drain-source voltage (DC)		–	–30	V
$V_{GS}$	gate-source voltage (DC)		–	±12	V
$I_D$	drain current (DC)	$T_s = 80\text{ °C}$ ; note 1	–	–4	A
$I_{DM}$	peak drain current	note 2	–	–16	A
$P_{tot}$	total power dissipation	$T_s = 80\text{ °C}$ ; note 3	–	3.5	W
		$T_{amb} = 25\text{ °C}$ ; note 4	–	2.6	W
		$T_{amb} = 25\text{ °C}$ ; note 5	–	1.1	W
		$T_{amb} = 25\text{ °C}$ ; note 6	–	1.5	W
$T_{stg}$	storage temperature		–55	+150	°C
$T_j$	operating junction temperature		–55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current (DC)	$T_s = 80\text{ °C}$	–	–2.6	A
$I_{SM}$	peak pulsed source current	note 2	–	–10	A

### Notes

- $T_s$  is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
- Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an  $R_{th\ a-tp}$  (ambient to tie-point) of 27.5 K/W.
- Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an  $R_{th\ a-tp}$  (ambient to tie-point) of 90 K/W.
- Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an  $R_{th\ a-tp}$  (ambient to tie-point) of 90 K/W.

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	20	K/W

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**CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per P-channel</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = -10\ \mu\text{A}$	-30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = -1\ \text{mA}$	-0.5	-	-1.1	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = -24\ \text{V}$	-	-	-100	nA
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 12\ \text{V}; V_{DS} = 0$	-	-	$\pm 100$	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -2.5\ \text{V}; I_D = -1\ \text{A}$	-	-	0.25	$\Omega$
		$V_{GS} = -4.5\ \text{V}; I_D = -2\ \text{A}$	-	-	0.12	$\Omega$
$C_{iss}$	input capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	-	450	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	-	200	-	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	-	100	-	pF
$Q_G$	total gate charge	$V_{GS} = -6\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}$	-	13	-	nC
$Q_{GS}$	gate-source charge	$V_{GS} = -6\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}$	-	1	-	nC
$Q_{GD}$	gate-drain charge	$V_{GS} = -6\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}$	-	4	-	nC
<b>Switching times</b>						
$t_{d(on)}$	turn-on delay time	$V_{GS} = 0\ \text{to}\ -6\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; R_{gen} = 6\ \Omega$	-	6	-	ns
$t_r$	rise time	$V_{GS} = 0\ \text{to}\ -6\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; R_{gen} = 6\ \Omega$	-	4	-	ns
$t_{on}$	turn-on switching time	$V_{GS} = 0\ \text{to}\ -6\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; R_{gen} = 6\ \Omega$	-	10	-	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = -6\ \text{to}\ 0\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; R_{gen} = 6\ \Omega$	-	29	-	ns
$t_f$	fall time	$V_{GS} = -6\ \text{to}\ 0\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; R_{gen} = 6\ \Omega$	-	16	-	ns
$t_{off}$	turn-off switching time	$V_{GS} = -6\ \text{to}\ 0\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; R_{gen} = 6\ \Omega$	-	45	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain diode forward voltage	$V_{GD} = 0; I_S = -1.25\ \text{A}$	-	-	-1.3	V
$t_{rr}$	reverse recovery time	$I_S = -1.25\ \text{A}; di/dt = 100\ \text{A}/\mu\text{s}$	-	75	-	ns

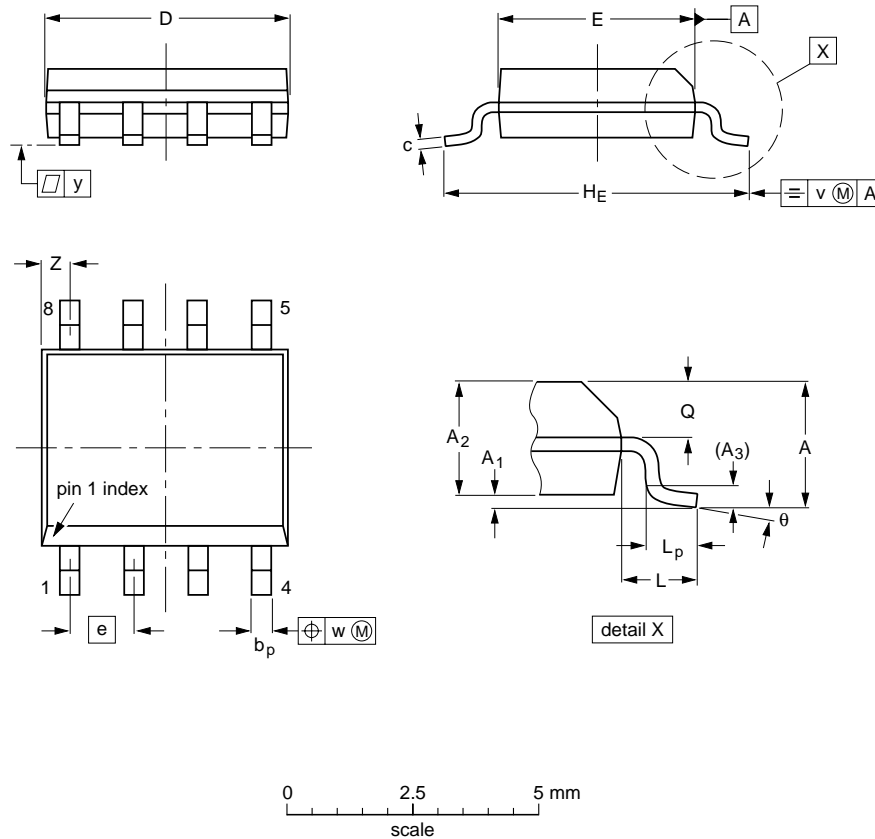
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## PACKAGE OUTLINE

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				95-02-04 97-05-22

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### DEFINITIONS

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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