

TrenchMOS™ transistor

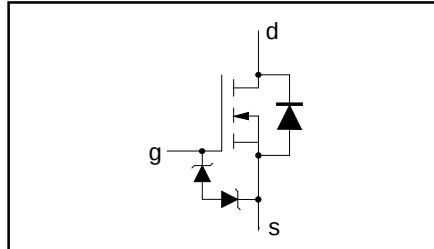
Logic level FET

PHT6N03LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Surface mounting package

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 30\text{ V}$
$I_D = 5.9\text{ A}$
$R_{DS(ON)} \leq 30\text{ m}\Omega$ ($V_{GS} = 5\text{ V}$)
$R_{DS(ON)} \leq 28\text{ m}\Omega$ ($V_{GS} = 10\text{ V}$)

GENERAL DESCRIPTION

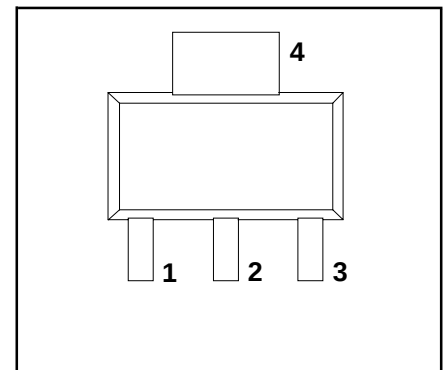
N-channel enhancement mode logic level field-effect power transistor using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHT6N03LT is supplied in the SOT223 surface mounting package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT223



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$	-	30	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$	-	5.9	A
		$T_{amb} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$	-	4.1	A
I_{DM}	Pulsed drain current		-	23.6	A
P_D	Total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	1.8	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	150	$^{\circ}\text{C}$

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 k Ω)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point	mounted on any pcb	-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	mounted on test pcb of fig:17	-	70	-	K/W

TrenchMOS™ transistor

Logic level FET

PHT6N03LT

ELECTRICAL CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55°C	30 27	- -	- -	V V
V _{(BR)GSS}	Gate-source breakdown voltage	I _G = 1 mA	10	-	-	V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA T _j = 150°C T _j = -55°C	1 0.6 -	1.5 - -	2 - 2.3	V V V
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 5 V; I _D = 3.2 A V _{GS} = 10 V; I _D = 3.2 A V _{GS} = 5 V; I _D = 3.2 A; T _j = 150°C	- - -	24 18 -	30 28 51	mΩ mΩ mΩ
g _{fs}	Forward transconductance	V _{DS} = 25 V; I _D = 5.9 A	8	14	-	S
I _{DSS}	Zero gate voltage drain current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 150°C	-	0.05	10	μA
I _{GSS}	Gate source leakage current	V _{GS} = ±5 V; V _{DS} = 0 V T _j = 150°C	-	0.02	1	μA
			-	-	10	μA
Q _{g(tot)}	Total gate charge	I _D = 5.9 A; V _{DD} = 24 V; V _{GS} = 5 V	-	24	-	nC
Q _{gs}	Gate-source charge		-	3	-	nC
Q _{gd}	Gate-drain (Miller) charge		-	11	-	nC
t _{d on}	Turn-on delay time	V _{DD} = 15 V; I _D = 5.9 A;	-	30	45	ns
t _r	Turn-on rise time	V _{GS} = 5 V; R _G = 5 Ω	-	80	130	ns
t _{d off}	Turn-off delay time	Resistive load	-	95	135	ns
t _f	Turn-off fall time		-	40	55	ns
L _d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L _d	Internal drain inductance	Measured from drain lead to centre of die	-	3.5	-	nH
L _s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	1050	-	pF
C _{oss}	Output capacitance		-	270	-	pF
C _{rss}	Feedback capacitance		-	140	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

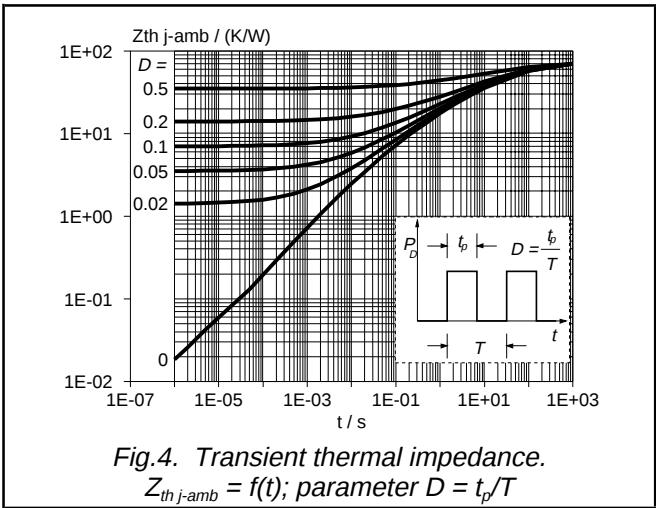
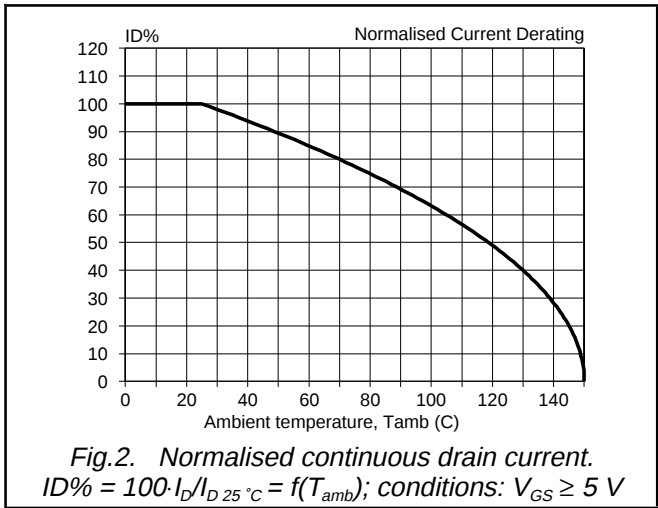
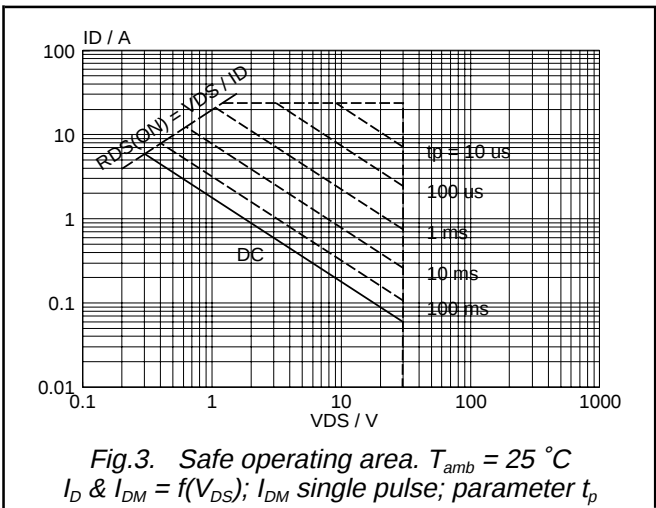
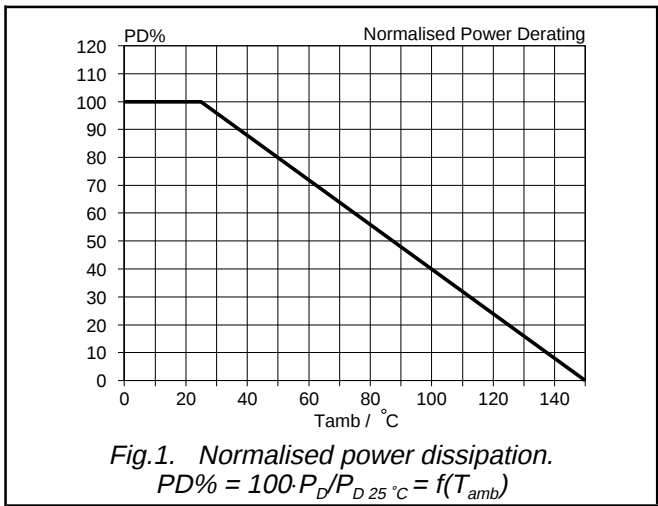
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)		-	-	5.9	A
I _{SM}	Pulsed source current (body diode)		-	-	10	A
V _{SD}	Diode forward voltage	I _F = 5.9 A; V _{GS} = 0 V	-	0.75	1.2	V
t _{rr}	Reverse recovery time	I _F = 5.9 A; -di _F /dt = 100 A/μs;	-	100	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = -10 V; V _R = 25 V	-	0.4	-	μC

TrenchMOS™ transistor
Logic level FET

PHT6N03LT

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 5.9\text{ A}$; $V_{DD} \leq 15\text{ V}$; $V_{GS} = 10\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $T_{amb} = 25\text{ }^\circ\text{C}$	-	60	mJ



TrenchMOS™ transistor

Logic level FET

PHT6N03LT

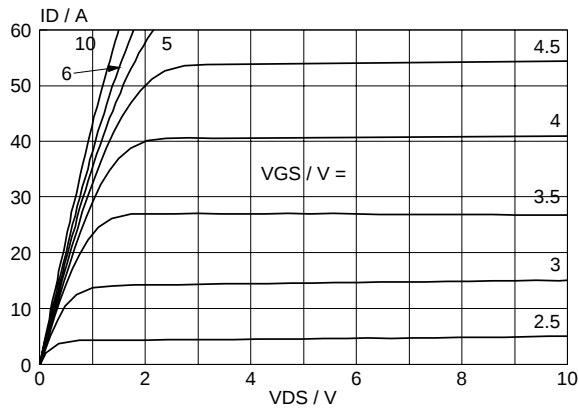


Fig.5. Typical output characteristics, $T_j = 25\text{ }^{\circ}\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

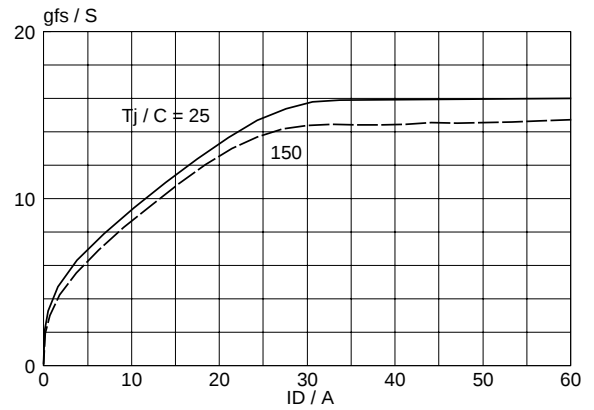


Fig.8. Typical transconductance, $T_j = 25\text{ }^{\circ}\text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

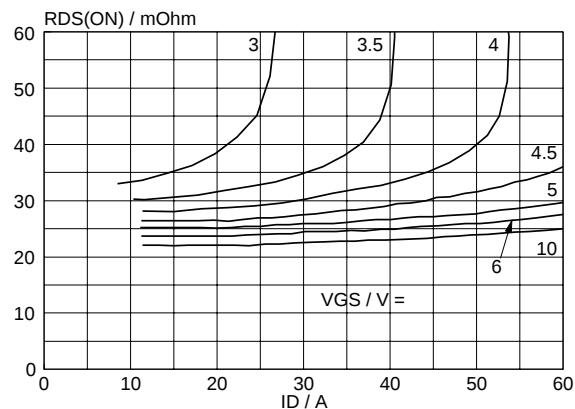


Fig.6. Typical on-state resistance, $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

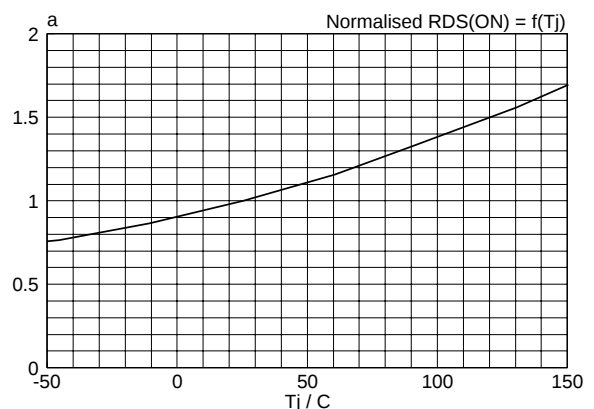


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ }^{\circ}\text{C}} = f(T_j)$; $I_D = 3.2\text{ A}$; $V_{GS} = 5\text{ V}$

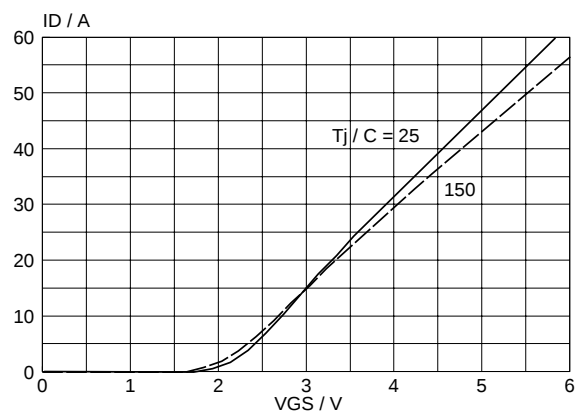


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

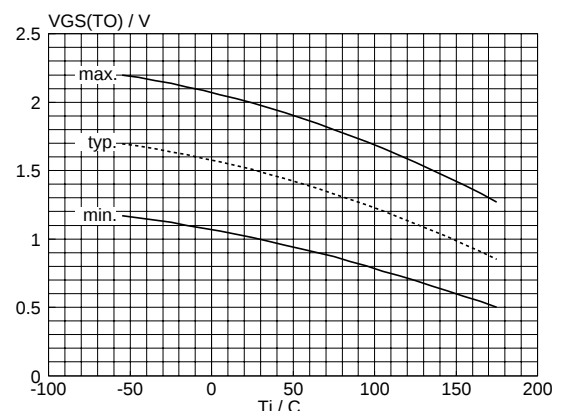
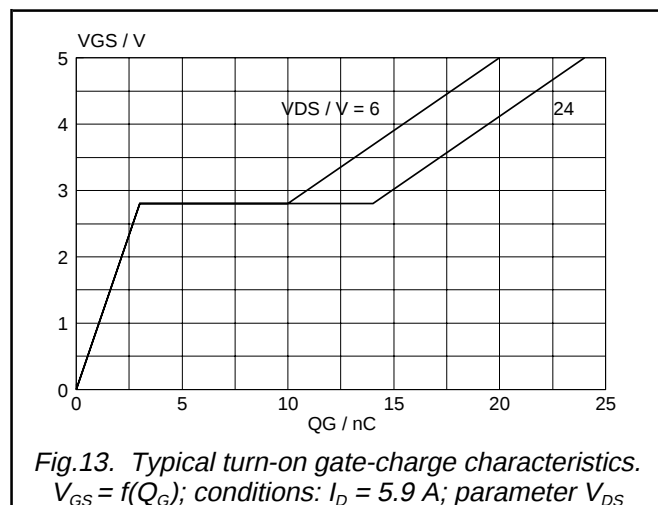
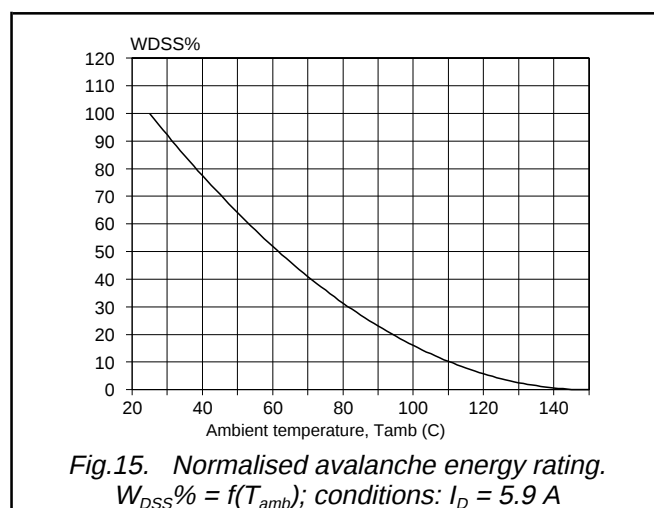
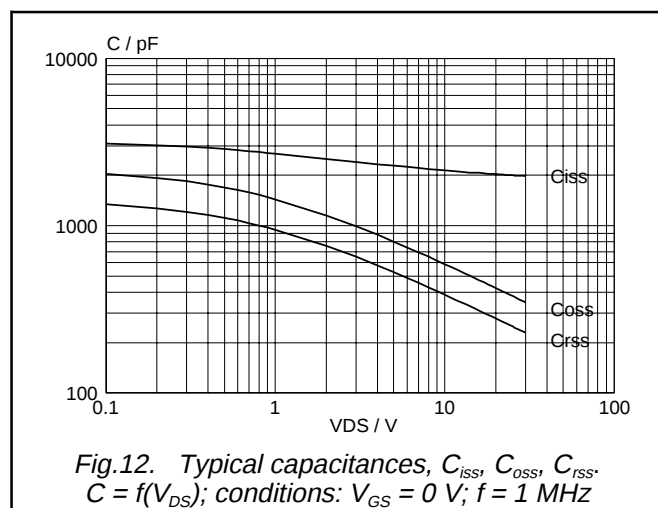
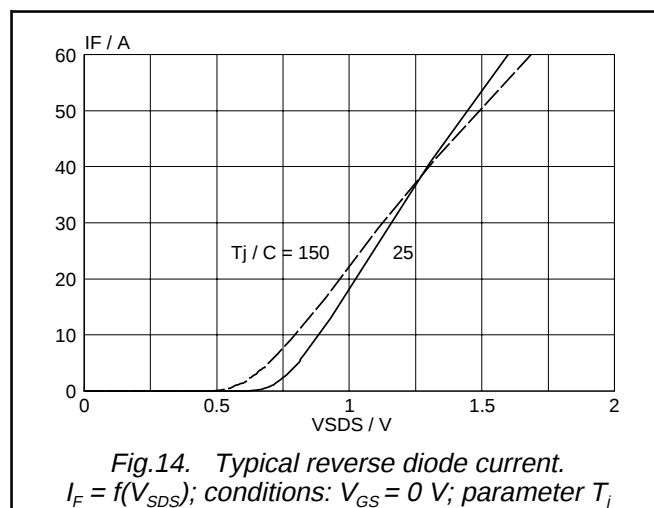
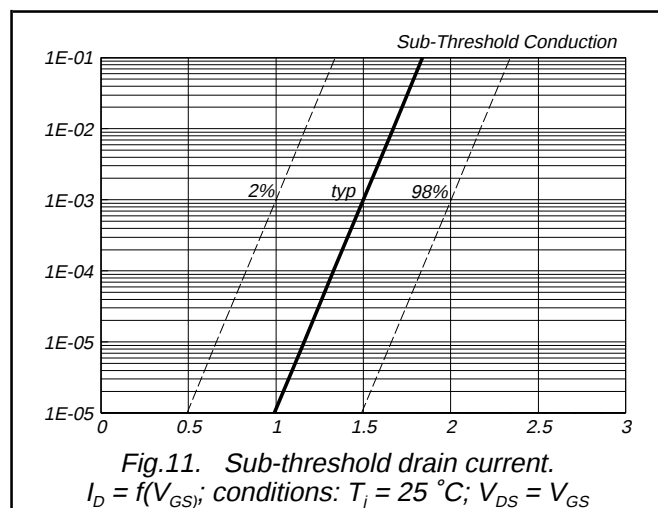


Fig.10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

TrenchMOS™ transistor

Logic level FET

PHT6N03LT



TrenchMOS™ transistor
Logic level FET**PHT6N03LT****PRINTED CIRCUIT BOARD**