Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

DESCRIPTION

The PLS100 (3-State) and PLS101 (Open Collector) are bipolar, fuse Programmable Logic Arrays (PLAs). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs and be ANDed together to comprise one P-term. All 48 P-terms can be selectively ORed to each output.

The PLS100 and PLS101 are fully TTL compatible, and chip enable control for expansion of input variables and output inhibit. They feature either Open Collector or 3-State outputs for ease of expansion of product terms and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

FEATURES

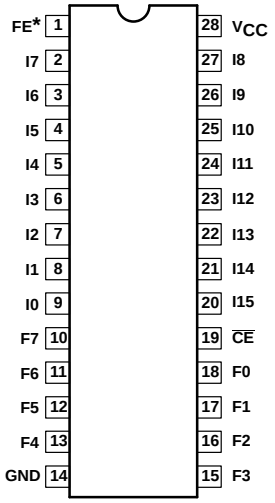
- Field-programmable (Ni-Cr link)
- Input variables: 16
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 50ns (max.)
- Power dissipation: 600mW (typ.)
- Input loading: –100μA (max.)
- Chip Enable input
- Output option:
  - PLS100: 3-State
  - PLS101: Open-Collector
- Output disable function:
  - 3-State: Hi-Z
  - Open-Collector: High

APPLICATIONS

- CRT display systems
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Data security encoders
- Fault detectors
- Frequency synthesizers
- 16-bit to 8-bit bus interface
- Random logic replacement

PIN CONFIGURATIONS

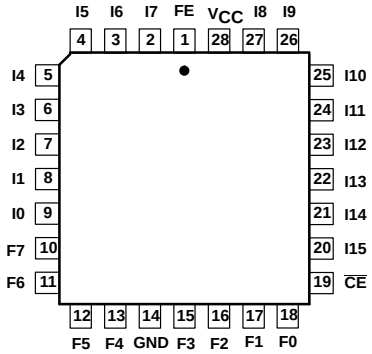
N Package



* Fuse Enable Pin: It is recommended that this pin be left open or connected to ground during normal operation.

N = Plastic DIP (600mil-wide)

A Package

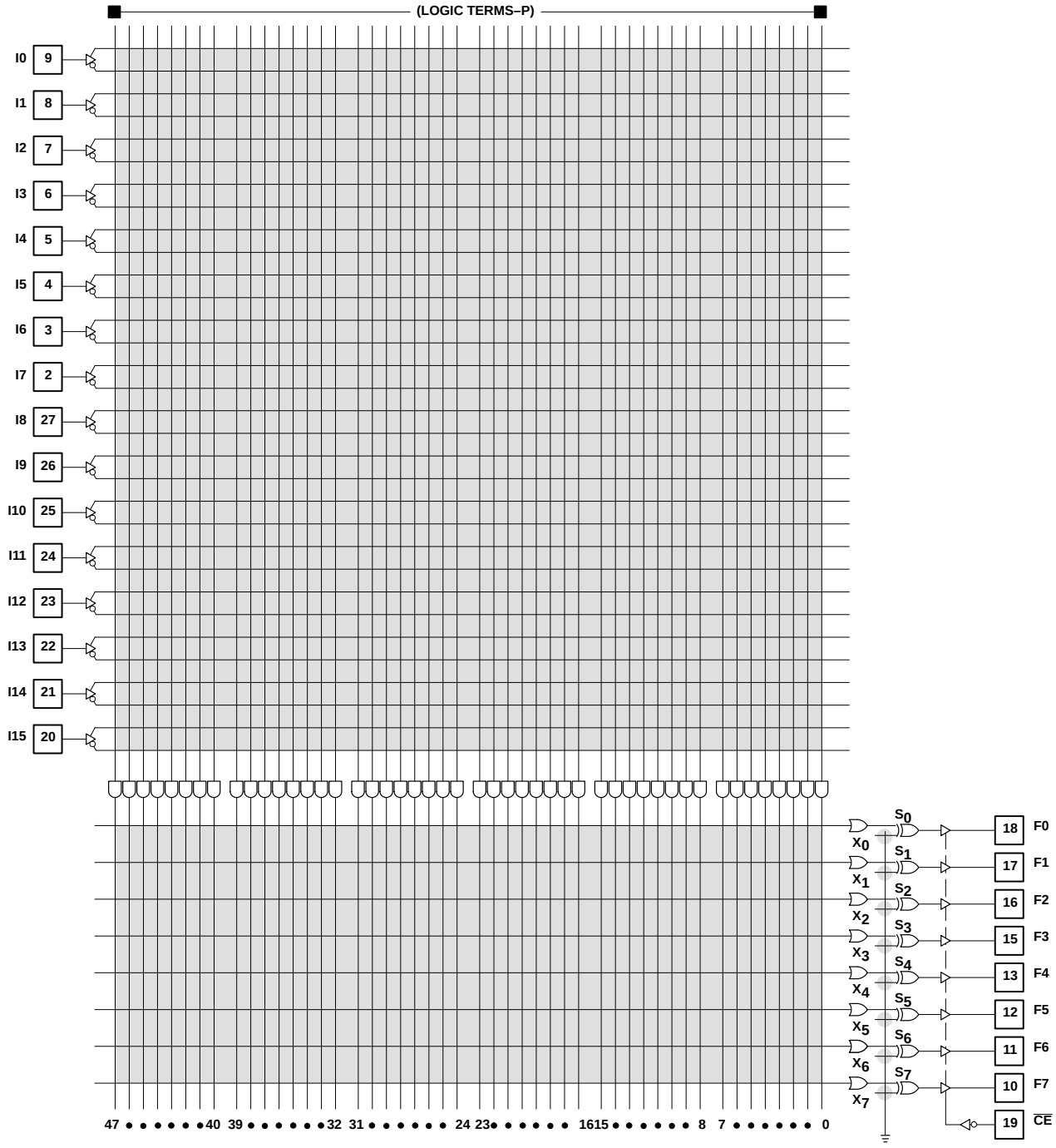


A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	3-STATE	OPEN COLLECTOR	DRAWING NUMBER
28-Pin Plastic Dual In-Line 600mil-wide	PLS100N	PLS101N	0413D
28-Pin Plastic Leaded Chip Carrier	PLS100A	PLS101A	0401F

LOGIC DIAGRAM

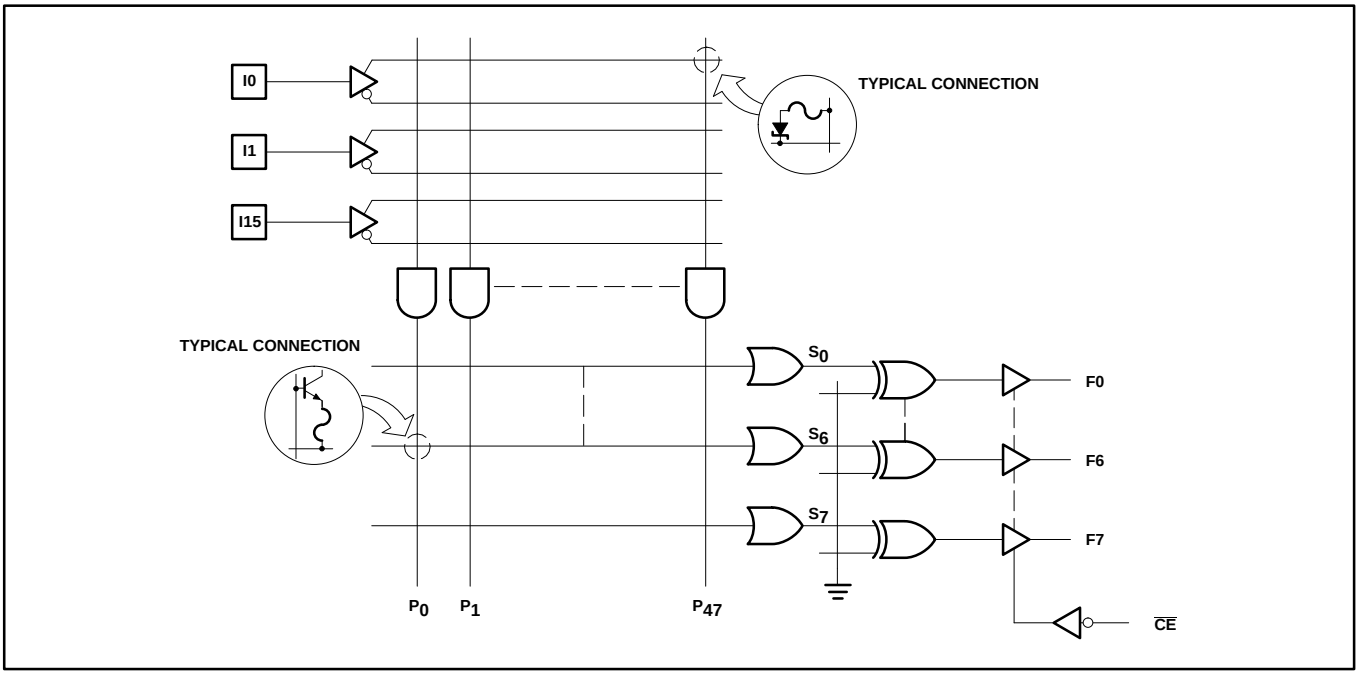


NOTES:
1. All AND gate inputs with a blown link float to a logic “1”.
2. All OR gate inputs with a blown fuse float to logic “0”.
3. ○ Programmable connection.

Programmable logic arrays ($16 \times 48 \times 8$)

PLS100/PLS101

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS100 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Philips Semiconductors Military Data Handbook.

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OH}	High (PLS100)[4]	I_{OH} = –2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 9.6mA		0.35	0.45	V
Input current						
I_{IH}	High	V_{IN} = 5.5V		< 1	25	µA
I_{IL}	Low	V_{IN} = 0.45V		–10	–100	µA
Output current						
$I_{O(OFF)}$	Hi-Z state (PLS100)	$\overline{CE}$ = High, V_{CC} = MAX				
		V_{OUT} = 5.5V		1	40	µA
		V_{OUT} = 0.45V		–1	–40	µA
I_{OS}	Short circuit (PLS100) [3, 6]	$\overline{CE}$ = Low, V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		120	170	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		8		pF
C_{OUT}	Output	V_{OUT} = 2.0V		17		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one pin at a time.
4. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
5. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the Chip Enable input grounded, all other inputs at 4.5V and the outputs open.

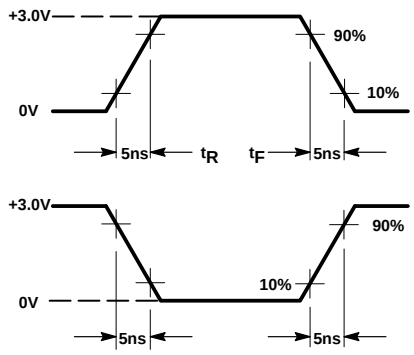
AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	TO	FROM	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Propagation delay[2]							
t_{PD}	Input	Output	Input		35	50	ns
t_{CE}	Chip Enable[3]	Output	Chip Enable		15	30	ns
Disable time							
t_{CD}	Chip Disable[3]	Output	Chip Enable		15	30	ns

NOTES:
1. All typical values are at $V_{CC} = 5V$. $T_{amb} = +25°C$.
2. All propagation delays are measured and specified under worst case conditions.
3. For 3-State output; output enable times are tested with $C_L = 30pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

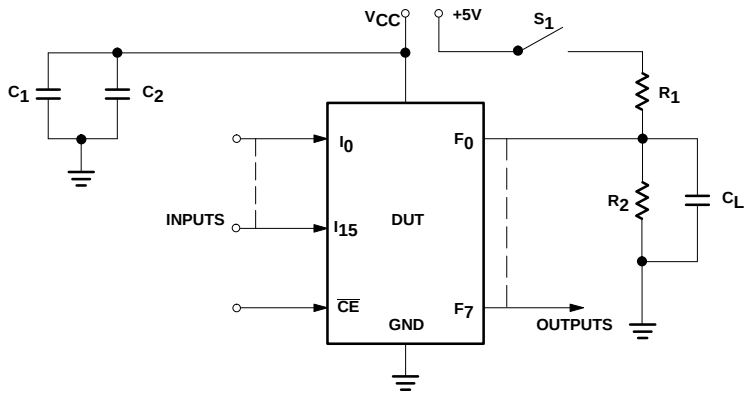
VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

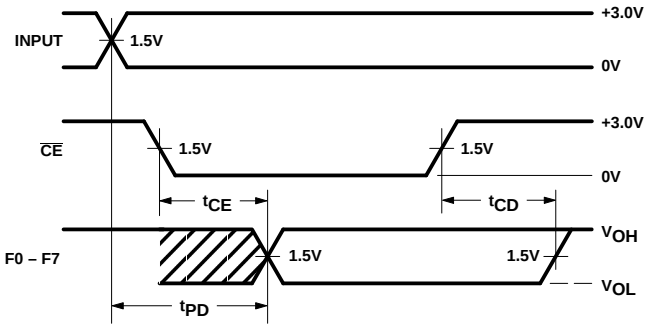


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with Input valid) and when Data Output becomes valid.
t_{CD}	Delay between when Chip Enable becomes High and Data Output is in off state (Hi-Z or High).
t_{PD}	Delay between beginning of valid Input (with Chip Enable Low) and when Data Output becomes valid.

TIMING DIAGRAM



Read Cycle

Programmable logic arrays ($16 \times 48 \times 8$)

PLS100/PLS101

LOGIC PROGRAMMING

PLS100/PLS101 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP, Data I/O Corporation's ABEL™ and Logical Devices Inc.'s CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

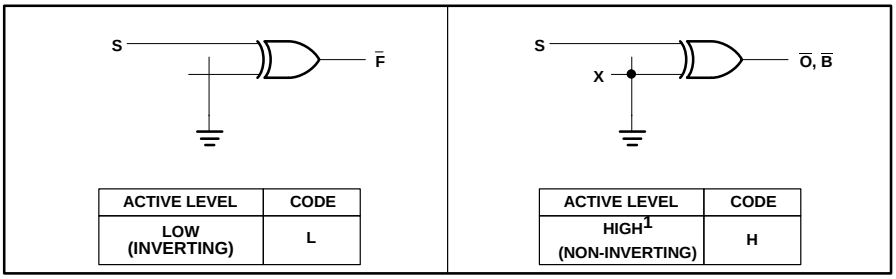
PLS100/PLS101 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Philips Semiconductors' SNAP PLD design software package.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The sumbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-party Programmer/ Software Support)* of this dat handbook for additional informational.

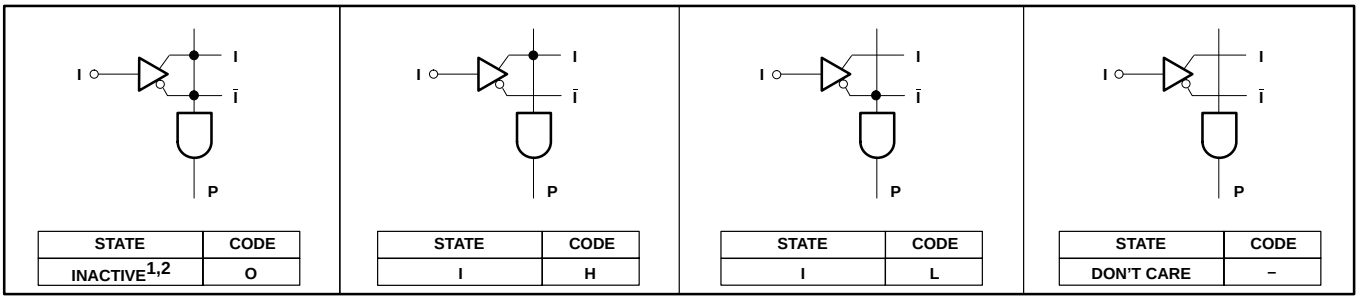
OUTPUT POLARITY – (F)



ACTIVE LEVEL	CODE
LOW (INVERTING)	L

ACTIVE LEVEL	CODE
HIGH[1] (NON-INVERTING)	H

"AND" ARRAY – (I)



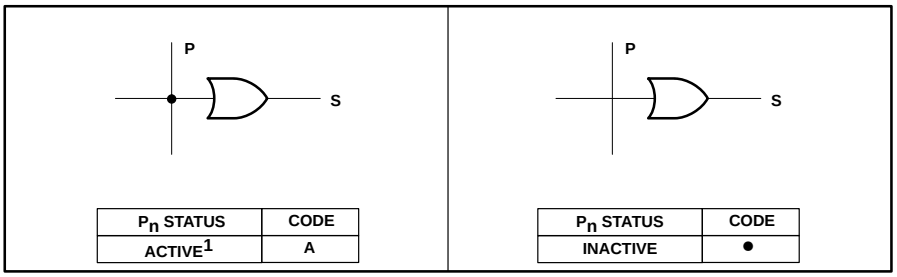
STATE	CODE
INACTIVE[1,2]	O

STATE	CODE
I	H

STATE	CODE
I	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY – (F)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	●

NOTES:
1. This is the initial unprogrammed state of all links. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

VIRGIN STATE

The PLS100/101 virgin devices are factory shipped in an unprogrammed state, with all fuses intact, such that:

1. All P_n terms are disabled (inactive) in the AND array.
2. All P_n terms are active in the OR array.
3. All outputs are Active-High.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable logic arrays ($16 \times 48 \times 8$)

PLS100/PLS101

PROGRAM TABLE

PROGRAM TABLE ENTRIES

INPUT VARIABLE

Im		
H	L	– (dash)

NOTE
Enter (–) for unused inputs of used P-terms.

OUTPUT FUNCTION

Prod. Term Present in Fp	Prod. Term Not Present in Fp
A	• (period)

NOTES
1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL

Active High	Active Low
H	L

NOTES
1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

CUSTOMER NAME _____

PURCHASE ORDER # _____

PHILIPS DEVICE # _____ **CF (XXXX)**

CUSTOMER SYMBOLIZED PART # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ **REV** ____ **DATE** ____

AND

TERM	INPUT (I_m)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																
1																
2																
3																
4																
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PIN NO.	20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9
VARIABLE NAME																

POLARITY

OR

OUTPUT (F_P)

7	6	5	4	3	2	1	0
10	11	12	13	15	16	17	18

SNAP RESOURCE SUMMARY DESIGNATIONS