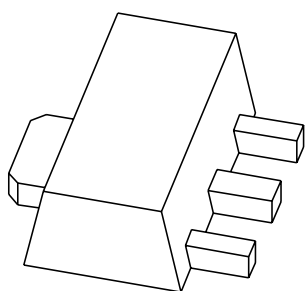


DATA SHEET



PXT3906 PNP switching transistor

Product specification
Supersedes data of 1997 May 05

1999 Apr 14

PNP switching transistor

PXT3906

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- High-speed saturated switching applications.

DESCRIPTION

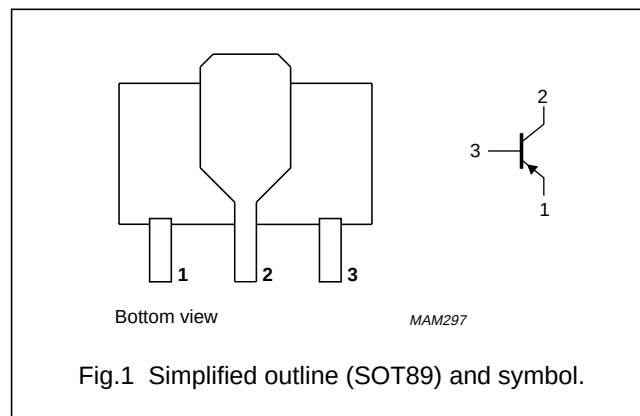
PNP switching transistor in a SOT89 plastic package.
NPN complement: PXT3904.

MARKING

TYPE NUMBER	MARKING CODE
PXT3906	p2A

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	—	–40	V
V_{CEO}	collector-emitter voltage	open base	—	–40	V
V_{EBO}	emitter-base voltage	open collector	—	–6	V
I_C	collector current (DC)		—	–100	mA
I_{CM}	peak collector current		—	–200	mA
I_{BM}	peak base current		—	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	—	1.2	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		—	150	°C
T_{amb}	operating ambient temperature		–55	+150	°C

Note

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 6 cm².
For other mounting conditions, see “Thermal considerations for SOT89 in the General Part of associated Handbook”.

PNP switching transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	104	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		24	K/W

Note

- Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 6 cm².
For other mounting conditions, see "Thermal considerations for SOT89 in the General Part of associated Handbook".

CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = -30\text{ V}$	–	–50	nA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = -6\text{ V}$	–	–50	nA
h_{FE}	DC current gain	$V_{CE} = -1\text{ V}$; (see Fig.2) $I_C = -0.1\text{ mA}$ $I_C = -1\text{ mA}$ $I_C = -10\text{ mA}$ $I_C = -50\text{ mA}$ $I_C = -100\text{ mA}$	60 80 100 60 30	– – 300 – –	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}$; $I_B = -1\text{ mA}$	–	–250	mV
		$I_C = -50\text{ mA}$; $I_B = -5\text{ mA}$	–	–400	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = -10\text{ mA}$; $I_B = -1\text{ mA}$	–650	–850	mV
		$I_C = -50\text{ mA}$; $I_B = -5\text{ mA}$	–	–950	mV
C_c	collector capacitance	$I_E = I_C = 0$; $V_{CB} = -5\text{ V}$; $f = 1\text{ MHz}$	–	4.5	pF
C_e	emitter capacitance	$I_C = I_E = 0$; $V_{EB} = -500\text{ mV}$; $f = 1\text{ MHz}$	–	10	pF
f_T	transition frequency	$I_C = -10\text{ mA}$; $V_{CE} = -20\text{ V}$; $f = 100\text{ MHz}$	250	–	MHz
F	noise figure	$I_C = -100\text{ }\mu\text{A}$; $V_{CE} = -5\text{ V}$; $R_S = 1\text{ k}\Omega$; $f = 10\text{ Hz to }15.7\text{ kHz}$	–	4	dB

Switching times (between 10% and 90% levels); (see Fig.3)

t_{on}	turn-on time	$I_{Con} = -10\text{ mA}$; $I_{Bon} = -1\text{ mA}$; $I_{Boff} = 1\text{ mA}$	–	65	ns
t_d	delay time		–	35	ns
t_r	rise time		–	35	ns
t_{off}	turn-off time		–	300	ns
t_s	storage time		–	225	ns
t_f	fall time		–	75	ns

PNP switching transistor

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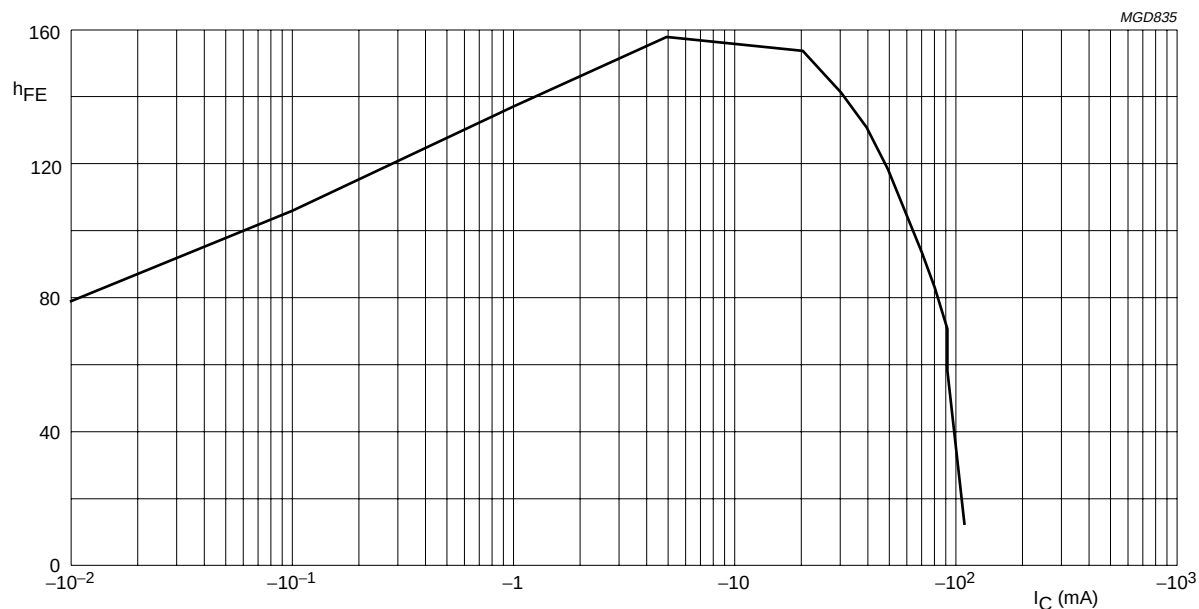
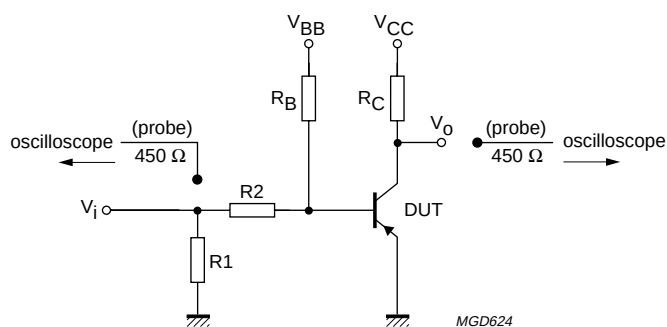
 $V_{CE} = -1$ V.

Fig.2 DC current gain; typical values.



$V_i = 5$ V; $T = 500$ μ s; $t_p = 10$ μ s; $t_r = t_f \leq 3$ ns.
 $R_1 = 56$ Ω ; $R_2 = 2.5$ k Ω ; $R_B = 3.9$ k Ω ; $R_C = 270$ Ω .
 $V_{BB} = 1.9$ V; $V_{CC} = -3$ V.
 Oscilloscope: input impedance $Z_i = 50$ Ω .

Fig.3 Test circuit for switching times.

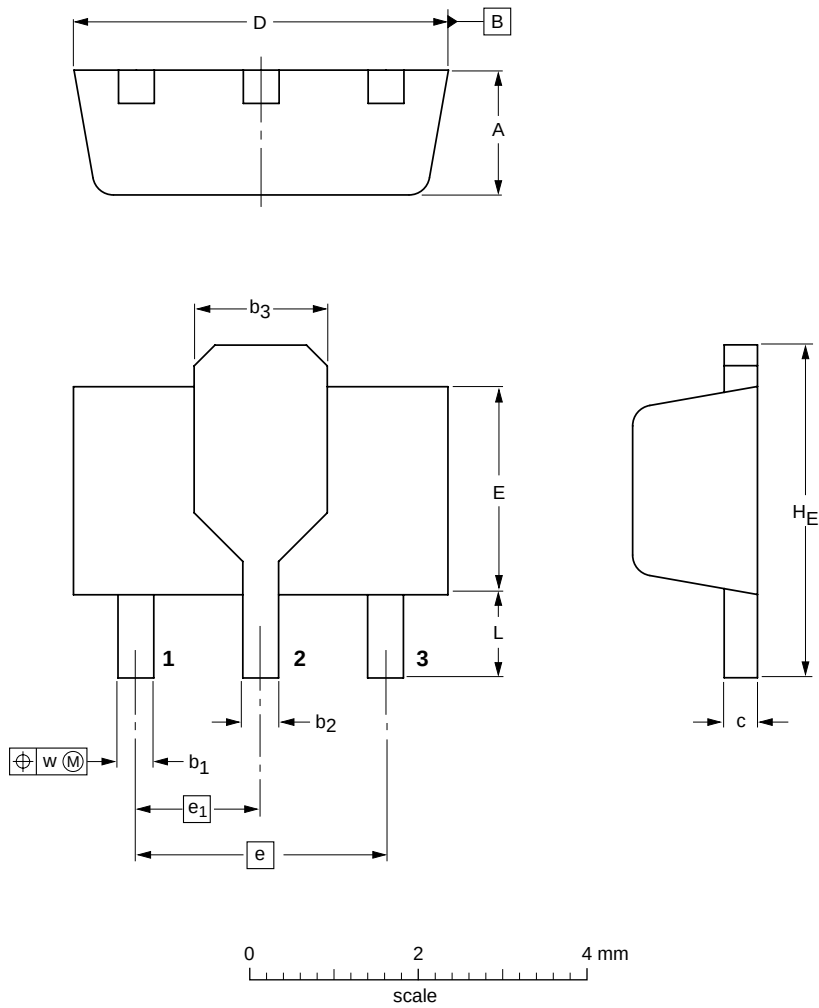
PNP switching transistor

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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b ₁	b ₂	b ₃	c	D	E	e	e ₁	H _E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

PNP switching transistor

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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PNP switching transistor

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Printed in The Netherlands

115002/00/03/pp8

Date of release: 1999 Apr 14

Document order number: 9397 750 05627

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