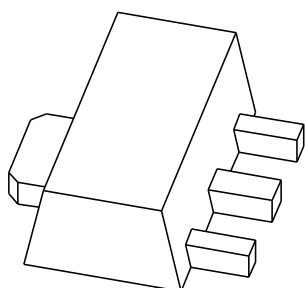


DATA SHEET



PXTA64 PNP Darlington transistor

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC04

1997 Apr 24

PNP Darlington transistor

PXTA64

FEATURES

- High current (max. 500 mA)
- Low voltage (max. 30 V).

APPLICATIONS

- High input impedance preamplifiers.

DESCRIPTION

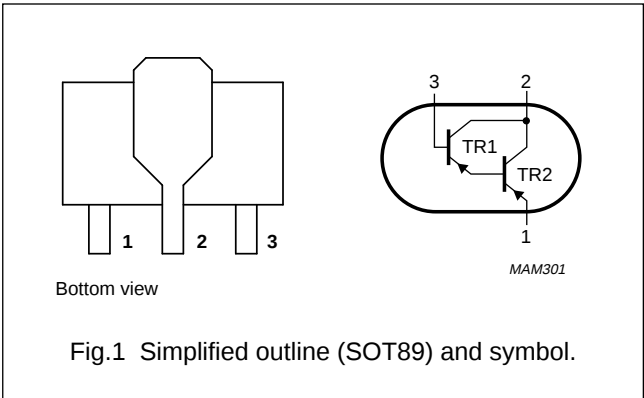
PNP Darlington transistor in a SOT89 plastic package.
NPN complement: PXTA14.

MARKING

TYPE NUMBER	MARKING CODE
PXTA64	p2V

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–30	V
V_{CES}	collector-emitter voltage	$V_{BE} = 0$	–	–30	V
I_C	collector current (DC)		–	–500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	–	1.3	W
h_{FE}	DC current gain	$I_C = -10\text{ mA}$; $V_{CE} = -5\text{ V}$	10000	–	
f_T	transition frequency	$I_C = -100\text{ mA}$; $V_{CE} = -5\text{ V}$; $f = 100\text{ MHz}$	125	–	MHz

PNP Darlington transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–30	V
V_{CES}	collector-emitter voltage	$V_{BE} = 0$	–	–30	V
V_{EBO}	emitter-base voltage	open collector	–	–10	V
I_C	collector current (DC)		–	–500	mA
I_{CM}	peak collector current		–	–1	A
I_B	base current (DC)		–	–200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Device mounted on a printed-circuit board, single sided copper, tinplated, mounting pad for collector 1 cm².
For other mounting conditions, see *“Thermal considerations for the SOT89 in the General part of handbook SC04”*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	93	K/W
$R_{th\ j-s}$	thermal resistance from junction to solder point		12	K/W

Note

1. Device mounted on a printed-circuit board, single sided copper, tinplated, mounting pad for collector 1 cm².
For other mounting conditions, see *“Thermal considerations for the SOT89 in the General part of handbook SC04”*.

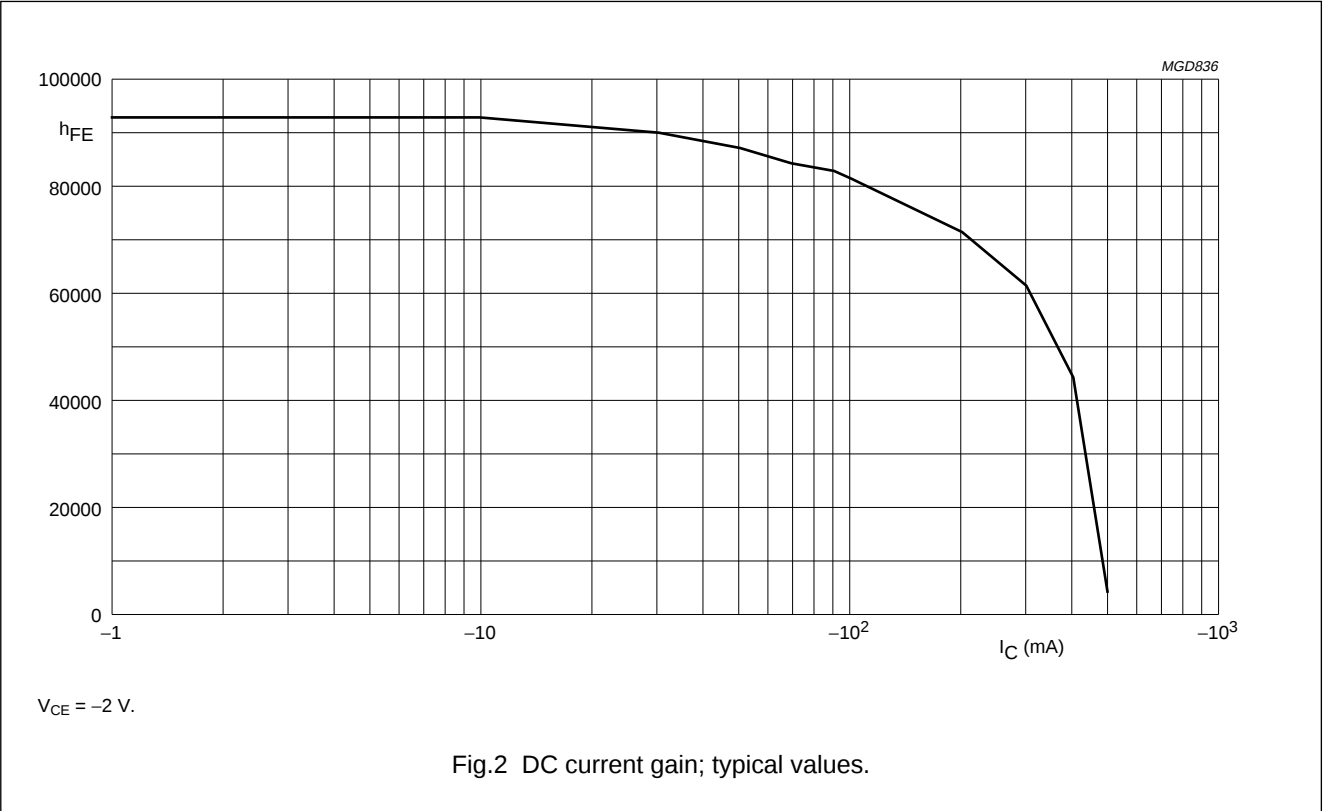
PNP Darlington transistor

PXTA64

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I _{CBO}	collector cut-off current	I _E = 0; V _{CB} = -30 V	-	-100	nA
I _{CES}	collector cut-off current	V _{BE} = 0; V _{CE} = -30 V	-	-100	nA
I _{EBO}	emitter cut-off current	I _C = 0; V _{BE} = -10 V	-	-100	nA
h _{FE}	DC current gain	I _C = -10 mA; V _{CE} = -5 V; see Fig.2	10000	-	
		I _C = -100 mA; V _{CE} = -5 V; see Fig.2	20000	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -100 mA; I _B = -0.1 mA	-	-1.5	V
V _{BEsat}	base-emitter saturation voltage	I _C = -100 mA; I _B = -0.1 mA	-	-1.5	V
V _{BEon}	base-emitter on-state voltage	I _C = -100 mA; V _{CE} = -5 V	-	-2	V
f _T	transition frequency	I _C = -100 mA; V _{CE} = -5 V; f = 100 MHz	125	-	MHz



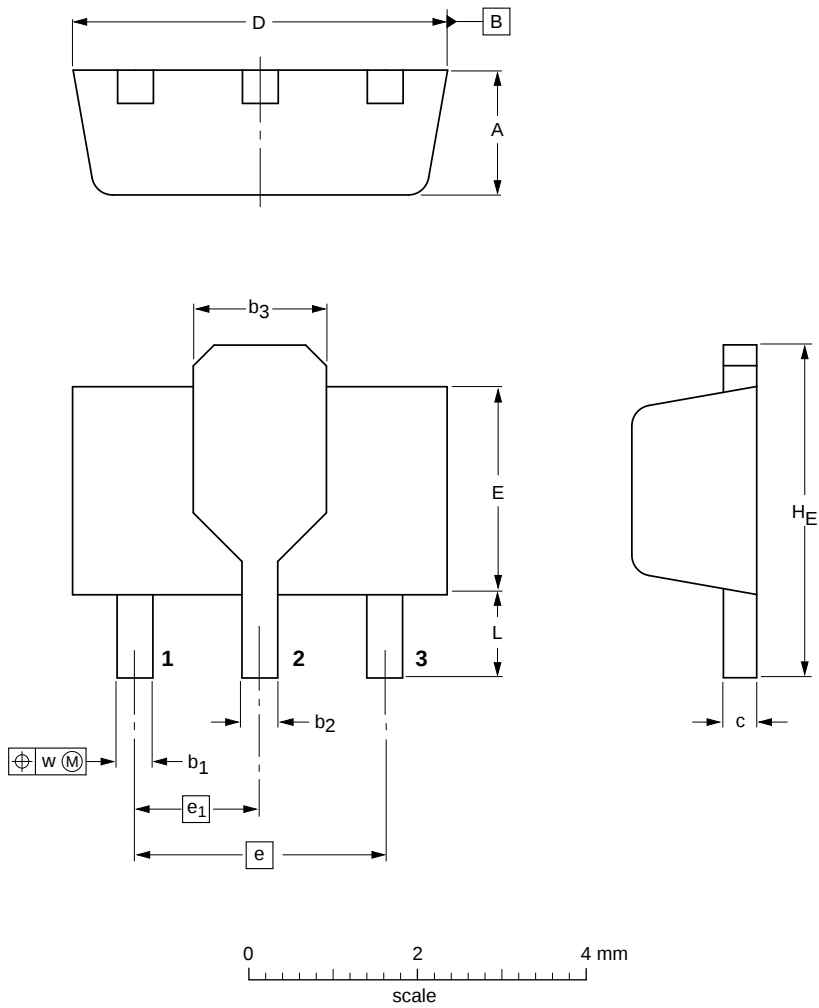
PNP Darlington transistor

PXTA64

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b ₁	b ₂	b ₃	c	D	E	e	e ₁	H _E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

PNP Darlington transistor**PXTA64**

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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PNP Darlington transistor

PXTA64

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