

# Si4800

N-channel enhancement mode field-effect transistor

Rev. 01 — 13 July 2001

Product data

## 1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™<sup>1</sup> technology.

Product availability:

Si4800 in SOT96-1 (SO8).

## 2. Features

- Low on-state resistance
- Fast switching
- TrenchMOS™ technology.

## 3. Applications

- DC to DC convertors
- DC motor control
- Lithium-ion battery applications
- Notebook PC
- Portable equipment applications.

## 4. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBK187</p> <p><b>SOT96-1 (SO8)</b></p>	<p>MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		

1. TrenchMOS is a trademark of Royal Philips Electronics.



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## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $150$ °C	–	30	V
$I_D$	drain current	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	9	A
$P_{tot}$	total power dissipation	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	2.5	W
$T_j$	junction temperature		–	150	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 9$ A; $T_j = 25$ °C	15.5	18.5	mΩ
		$V_{GS} = 4.5$ V; $I_D = 7$ A; $T_j = 25$ °C	27.5	33	mΩ

## 6. Limiting values

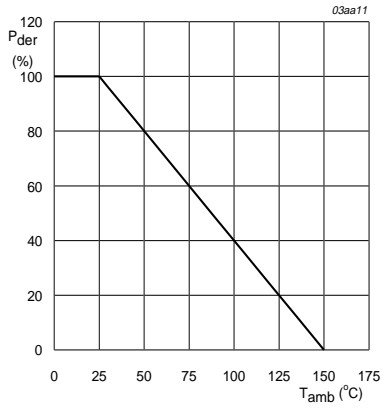
**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $150$ °C	–	30	V
$V_{GS}$	gate-source voltage (DC)		–	±20	V
$I_D$	drain current	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s; <b>Figure 2 and 3</b>	–	9	A
		$T_{amb} = 70$ °C; pulsed; $t_p \leq 10$ s; <b>Figure 2</b>	–	7	A
$I_{DM}$	peak drain current	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ μs; <b>Figure 3</b>	–	40	A
$P_{tot}$	total power dissipation	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s; <b>Figure 1</b>	–	2.5	W
		$T_{amb} = 70$ °C; pulsed; $t_p \leq 10$ s; <b>Figure 1</b>	–	1.6	W
$T_{stg}$	storage temperature		–55	+150	°C
$T_j$	operating junction temperature		–55	+150	°C

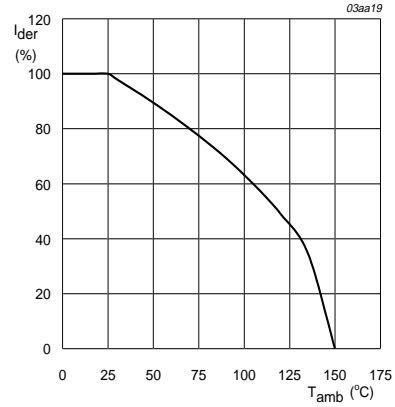
### Source-drain diode

$I_S$	source (diode forward) current	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	2.3	A
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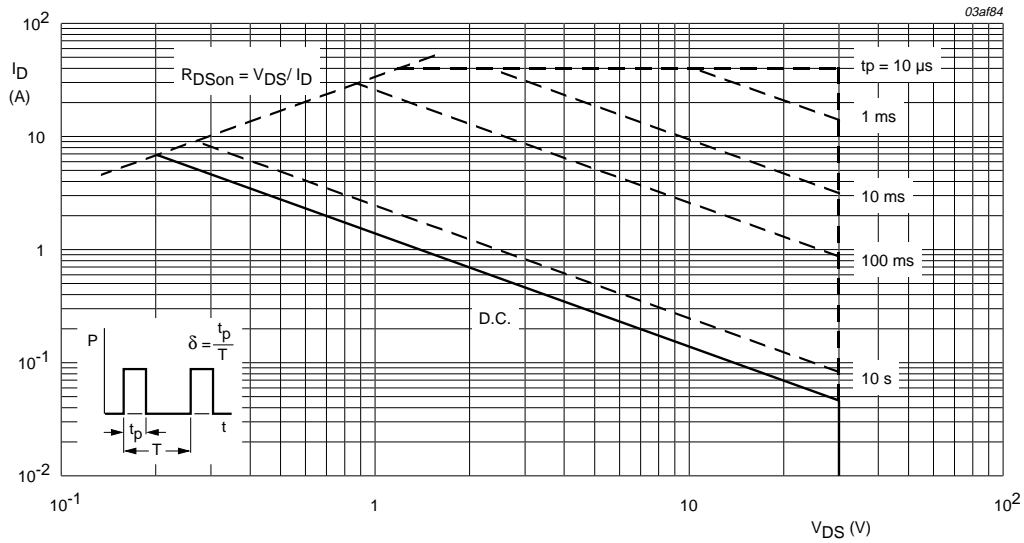
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T<sub>amb</sub> = 25 °C; I<sub>DM</sub> is single pulse.

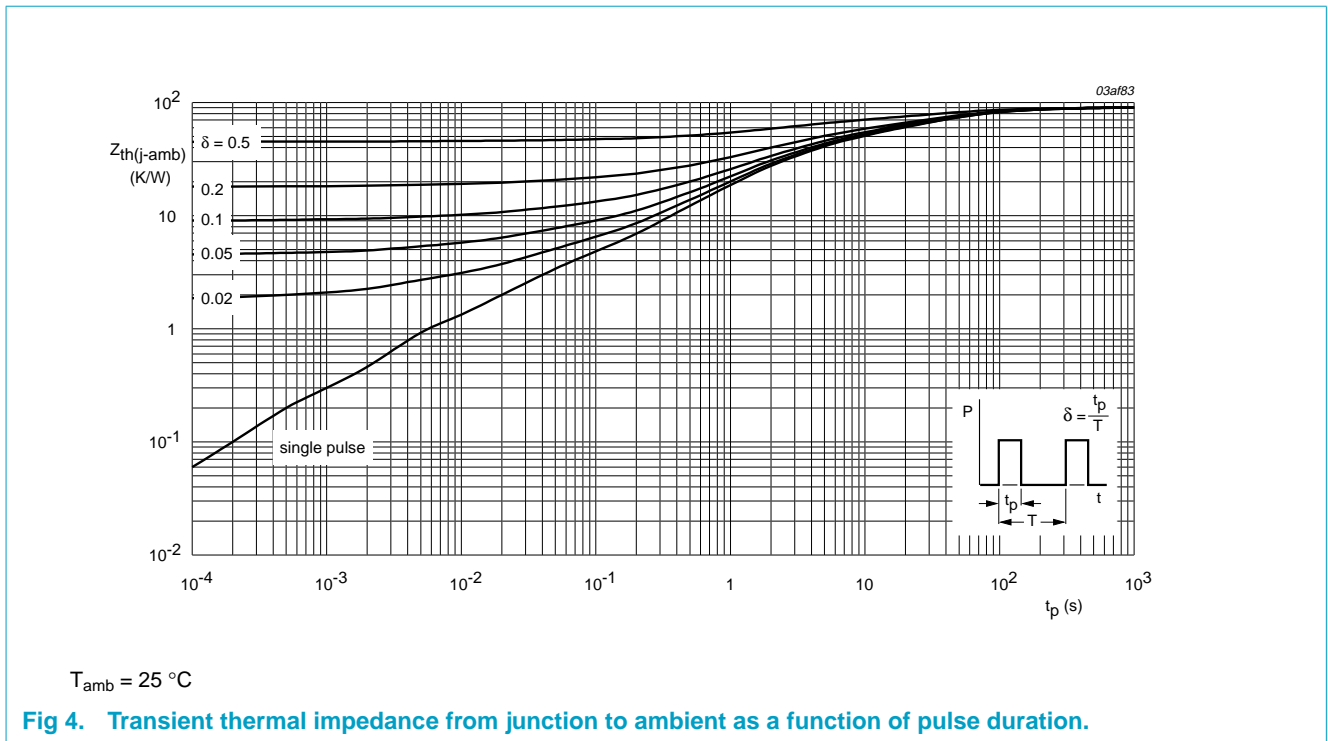
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; $t_p \leq 10$ s; minimum footprint; <a href="#">Figure 4</a>	50	K/W

### 7.1 Transient thermal impedance

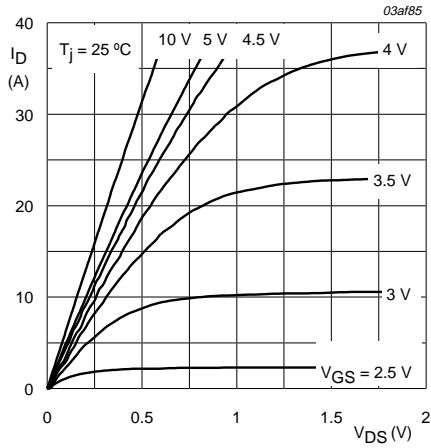


## 8. Characteristics

**Table 5: Characteristics**

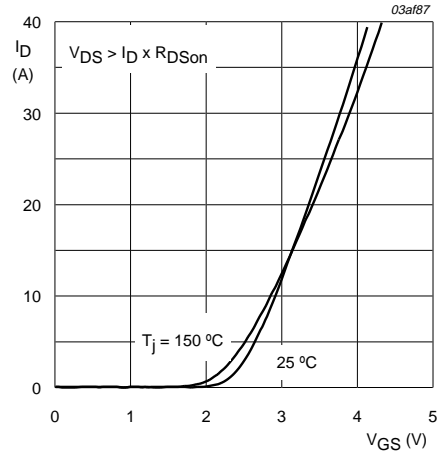
$T_j = 25\text{ °C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250\ \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\text{ °C}$	0.8	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 24\text{ V}$ ; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	–	–	1	$\mu\text{A}$
		$T_j = 55\text{ °C}$	–	–	5	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$ ; $V_{DS} = 0\text{ V}$	–	–	100	nA
$I_{D(on)}$	On-state drain current	$V_{DS} \geq 5$ ; $V_{GS} = 10\text{ V}$	30	–	–	A
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 9\text{ A}$ ; <b>Figure 7 and 8</b>	–	15.5	18.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ ; $I_D = 7\text{ A}$ ; <b>Figure 7 and 8</b>	–	27.5	33	m $\Omega$
<b>Dynamic characteristics</b>						
$g_{fs}$	forward transconductance	$V_{DS} = 15\text{ V}$ ; $I_D = 9\text{ A}$	–	19	–	S
$Q_{g(tot)}$	total gate charge	$I_D = 9\text{ A}$ ; $V_{DD} = 15\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; <b>Figure 13</b>	–	19	–	nC
$Q_{gs}$	gate-source charge		–	4	–	nC
$Q_{gd}$	gate-drain (Miller) charge		–	7.5	–	nC
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\text{ V}$ ; $R_D = 15\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $R_G = 6\ \Omega$	–	11	16	ns
$t_r$	rise time		–	8	15	ns
$t_{d(off)}$	turn-off delay time		–	22	30	ns
$t_f$	fall time		–	9	15	ns
<b>Source-drain (reverse) diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 2.3\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; <b>Figure 12</b>	–	0.7	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 2.3\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$	–	50	80	ns



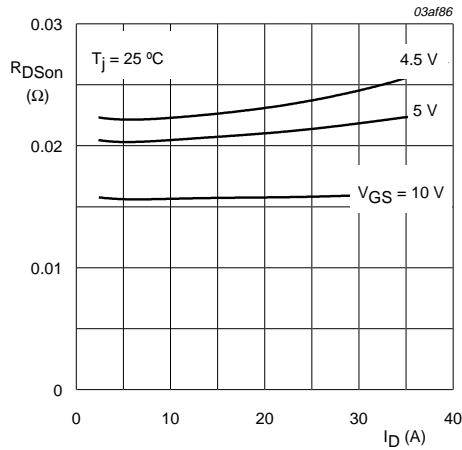
$T_j = 25\text{ °C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



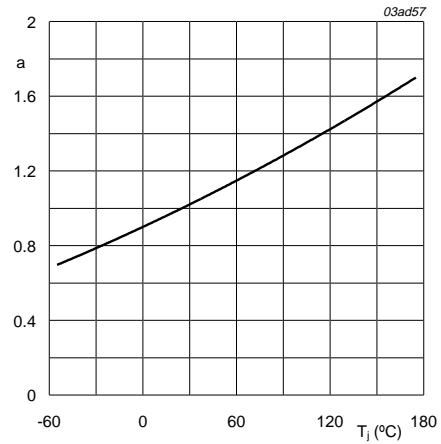
$T_j = 25\text{ °C}$  and  $150\text{ °C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



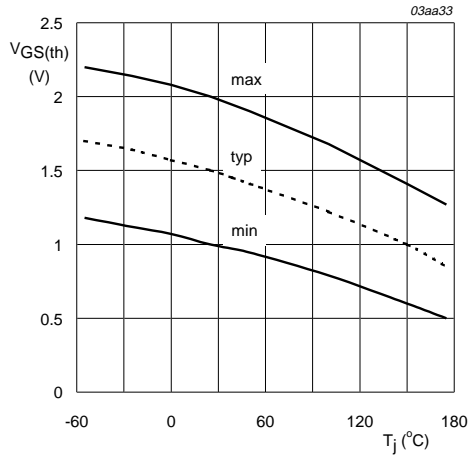
$T_j = 25\text{ °C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



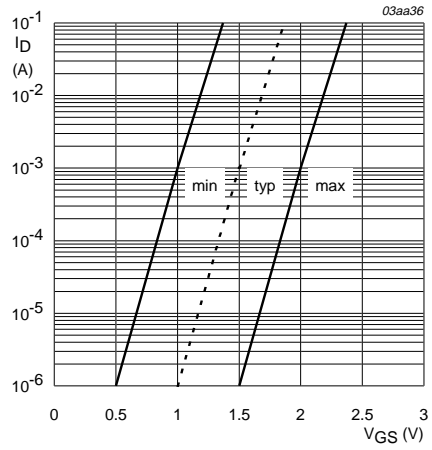
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



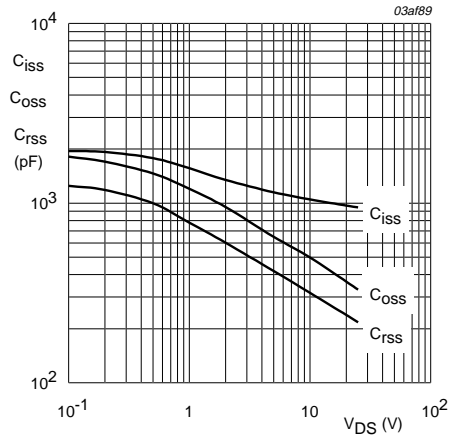
$I_D = 250 \mu A; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



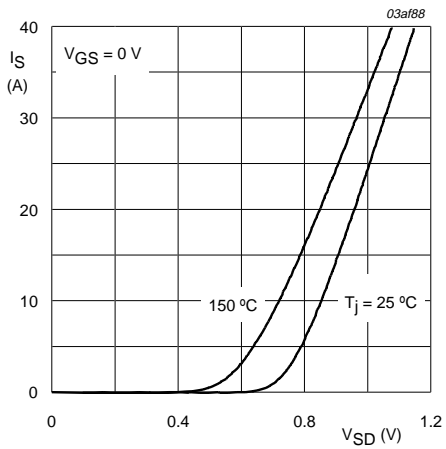
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



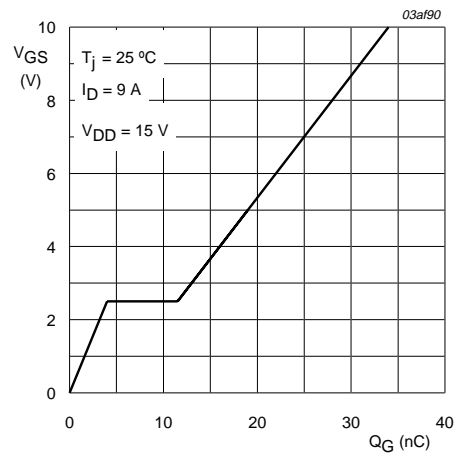
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 9\text{ A}$ ;  $V_{DD} = 15\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**



9. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

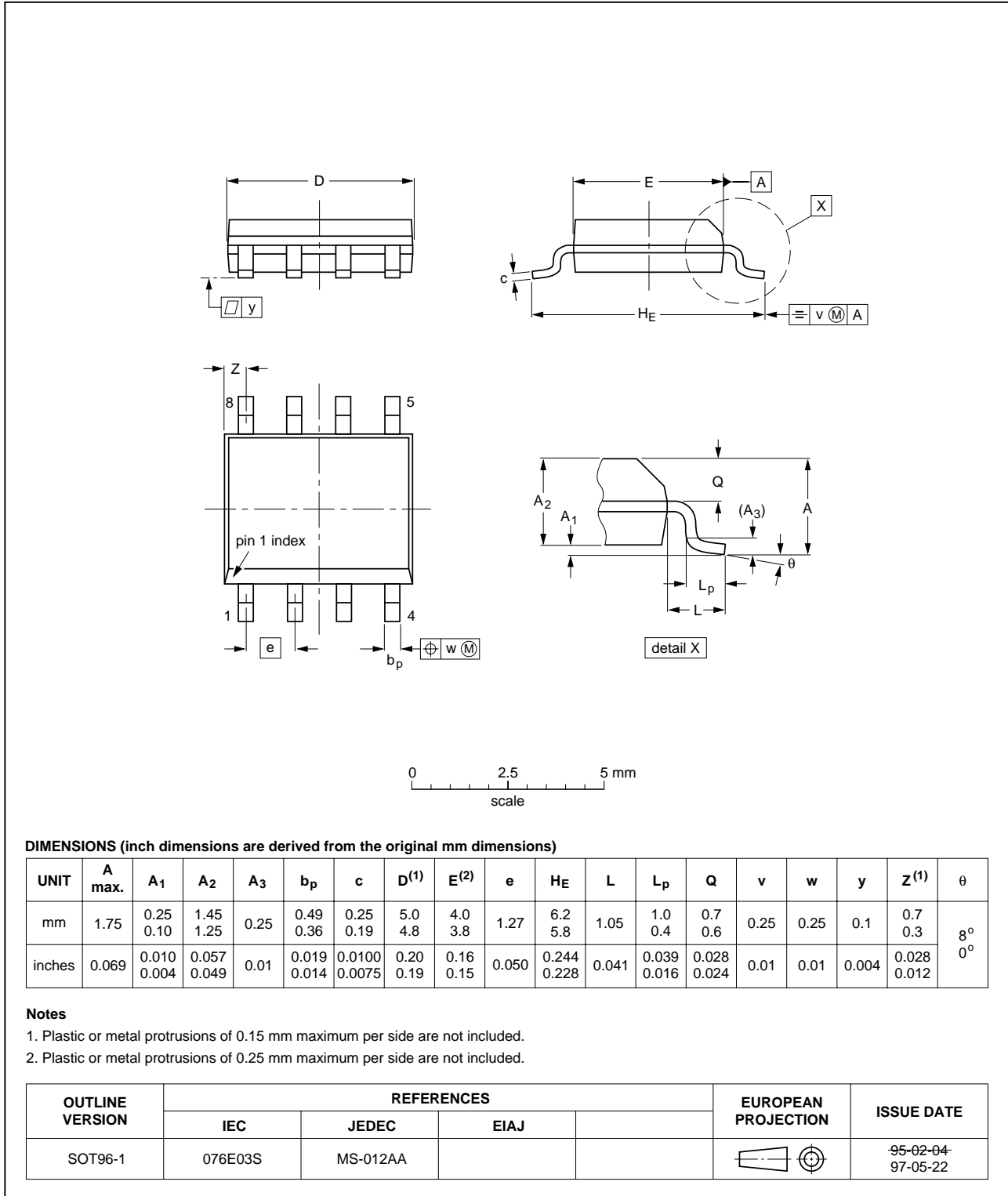


Fig 14. SOT96-1 (SO8).

## 10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010713	-	Product specification; initial version

## 11. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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