

# SI4884

TrenchMOS™ logic level FET

Rev. 02 — 12 April 2002

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

SI4884 in SOT96-1 (SO8).

### 1.2 Features

- Low on-state resistance
- Fast switching.

### 1.3 Applications

- DC to DC converters
- Portable equipment applications.

### 1.4 Quick reference data

- $V_{DS} = 30\text{ V}$
- $I_D = 12\text{ A}$
- $P_{tot} = 2.5\text{ W}$
- $R_{DS(on)} = 16.5\text{ m}\Omega$ .

## 2. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p style="text-align: center;">Top view MBK187</p> <p style="text-align: center;"><b>SOT96-1 (SO8)</b></p>	<p style="text-align: center;">MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		



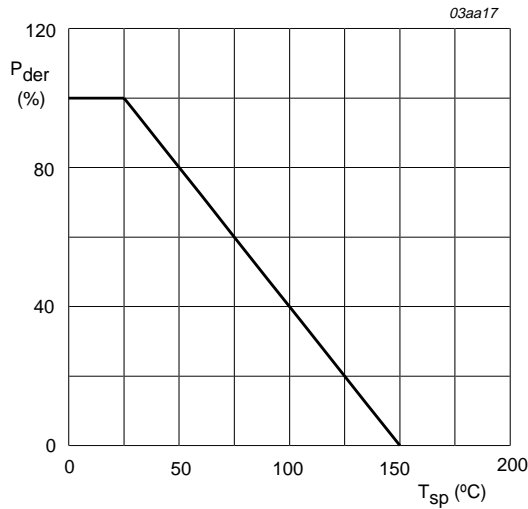
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### 3. Limiting values

**Table 2: Limiting values**

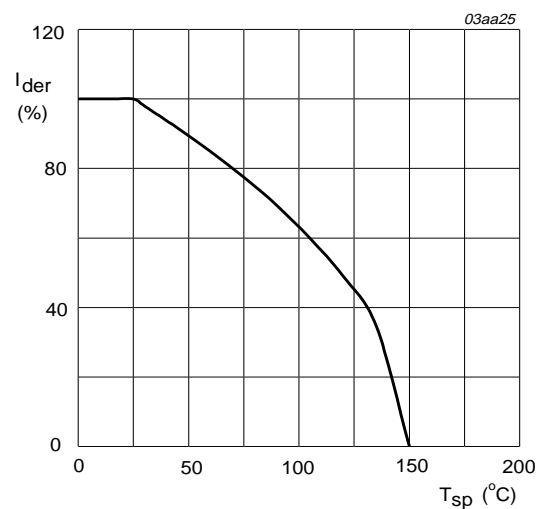
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $150$ °C	-	30	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current	$T_{sp} = 25$ °C; <b>Figure 2 and 3</b>	-	12	A
$I_{DM}$	peak drain current	$T_{sp} = 25$ °C; pulsed; <b>Figure 3</b>	-	45	A
$P_{tot}$	total power dissipation	$T_{sp} = 25$ °C; <b>Figure 1</b>	-	2.5	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current	$T_{sp} = 25$ °C	-	12	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

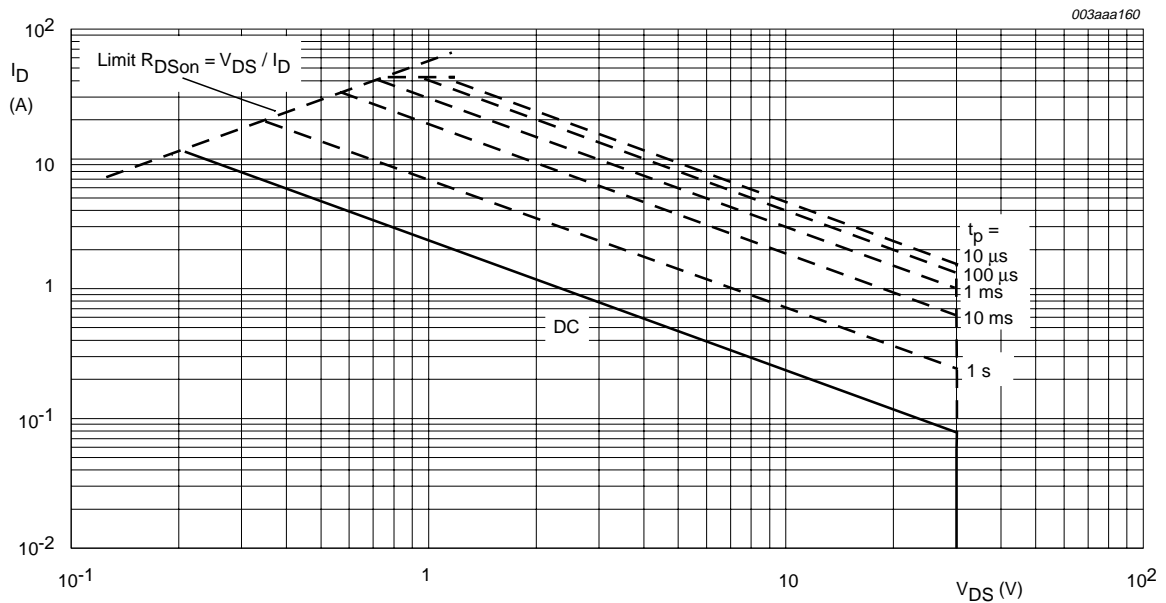
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; $t_p \leq 10$ s; minimum footprint; Figure 4	-	60	-	K/W

### 4.1 Transient thermal impedance

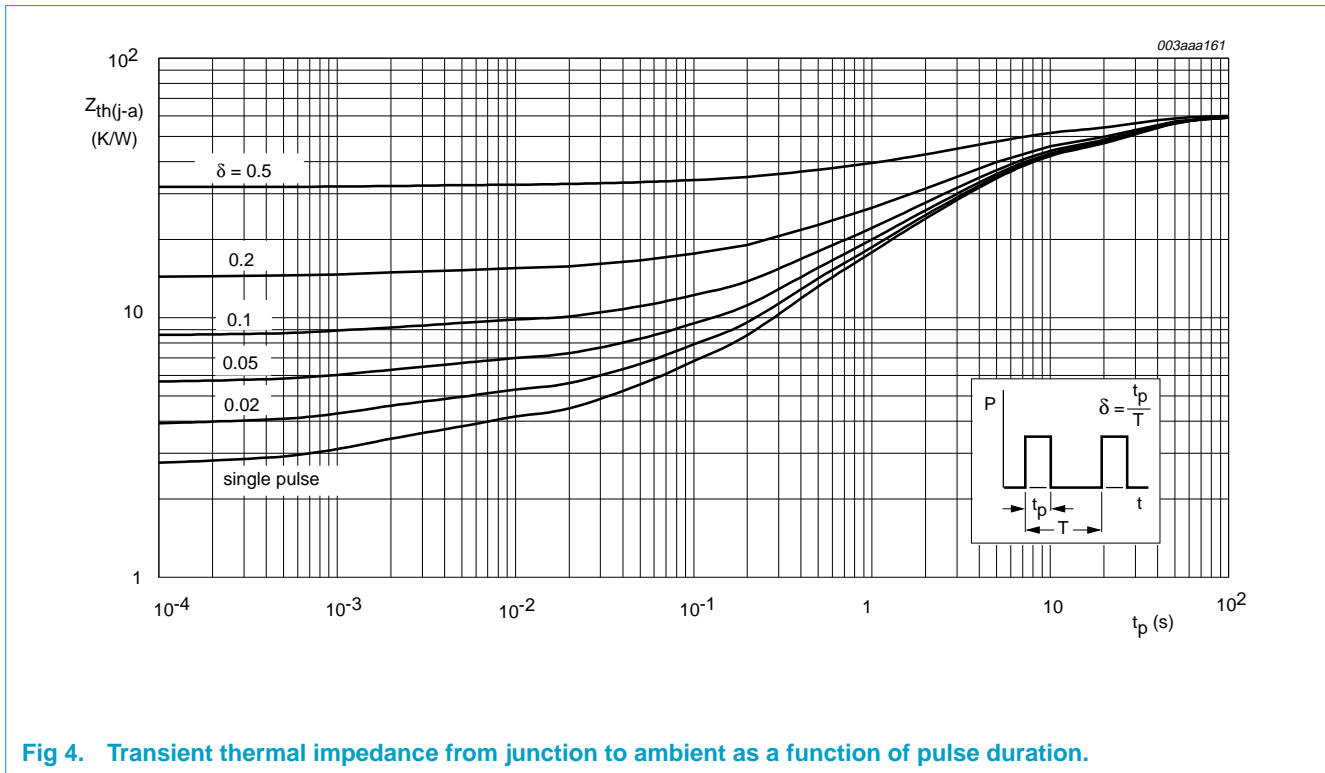


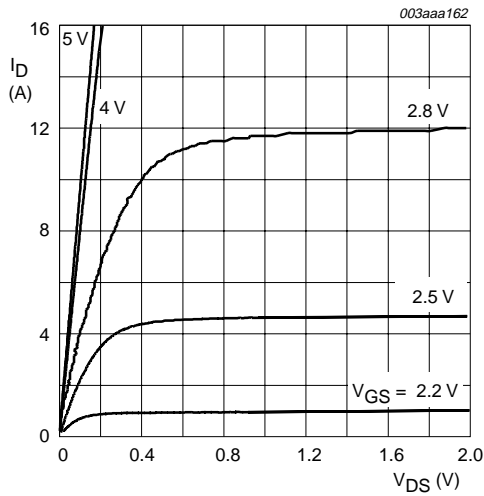
Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

## 5. Characteristics

**Table 4: Characteristics**

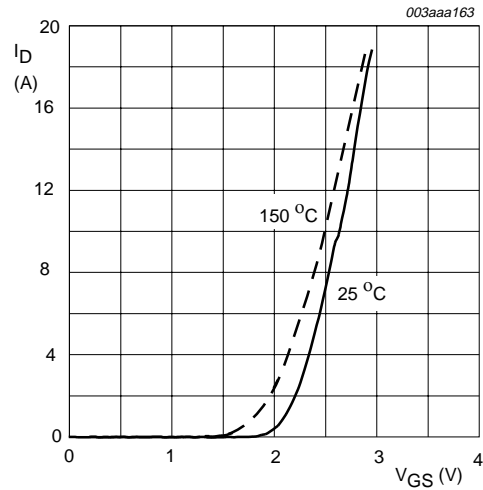
$T_j = 25\text{ °C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250\ \mu\text{A}; V_{DS} = V_{GS}$ ; <b>Figure 9</b>	1	-	2	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 24\ \text{V}; V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$	-	-	1	$\mu\text{A}$
			-	-	5	$\mu\text{A}$
			-	-	-	-
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}; I_D = 10\ \text{A}$ ; <b>Figure 7 and 8</b>	-	11	16.5	$\text{m}\Omega$
		$V_{GS} = 10\ \text{V}; I_D = 12\ \text{A}$ ;	-	8.9	10.5	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$g_{fs}$	forward transconductance	$V_{DS} = 15\ \text{V}; I_D = 10\ \text{A}$ ;	-	34	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 15\ \text{A}; V_{DD} = 16\ \text{V}; V_{GS} = 5\ \text{V}$ ; <b>Figure 13</b>	-	17.6	-	nC
$Q_{gs}$	gate-source charge		-	4	-	nC
$Q_{gd}$	gate-drain (Miller) charge		-	4.4	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 16\ \text{V}; f = 1\ \text{MHz}$ ; <b>Figure 11</b>	-	1335	-	pF
$C_{oss}$	output capacitance		-	391	-	pF
$C_{rss}$	reverse transfer capacitance		-	190	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 16\ \text{V}; R_D = 10\ \Omega; V_{GS} = 10\ \text{V}$	-	10.6	-	ns
$t_r$	rise time		-	11.7	-	ns
$t_{d(off)}$	turn-off delay time		-	37	-	ns
$t_f$	fall time		-	19	-	ns
<b>Source-drain (reverse) diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 1\ \text{A}; V_{GS} = 0\ \text{V}$ ; <b>Figure 12</b>	-	0.7	1.0	V
$t_{rr}$	reverse recovery time	$I_S = 2.3\ \text{A}; dI_S/dt = -100\ \text{A}/\mu\text{s}; V_{GS} = 0\ \text{V}$	-	70	-	ns



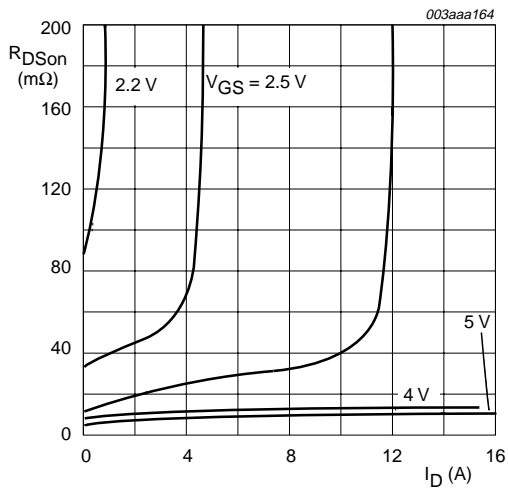
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



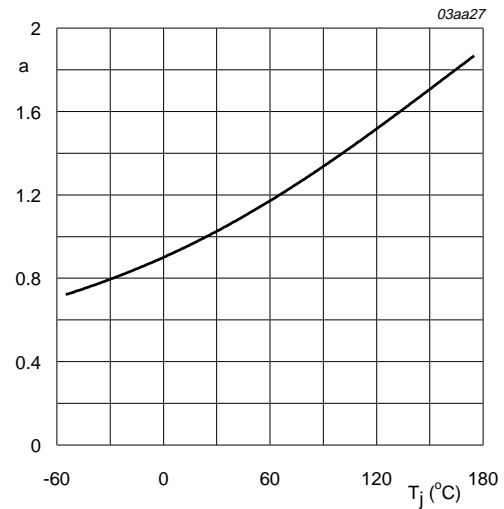
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



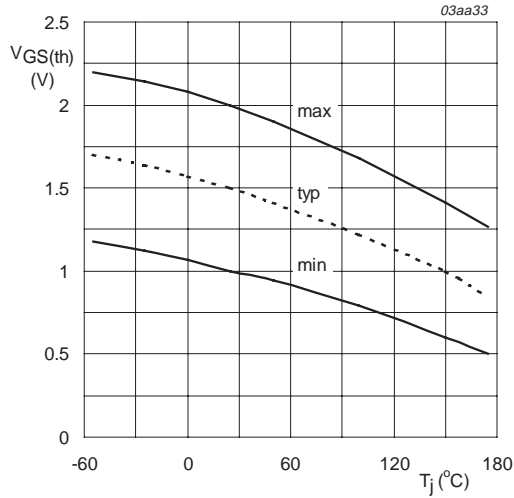
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



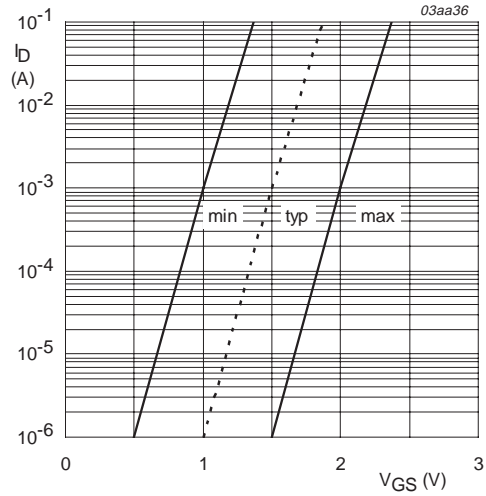
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



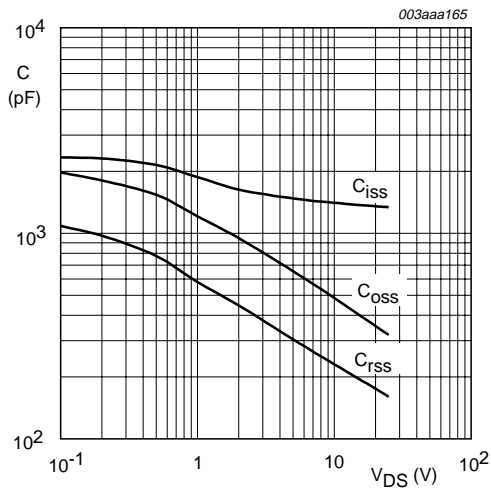
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



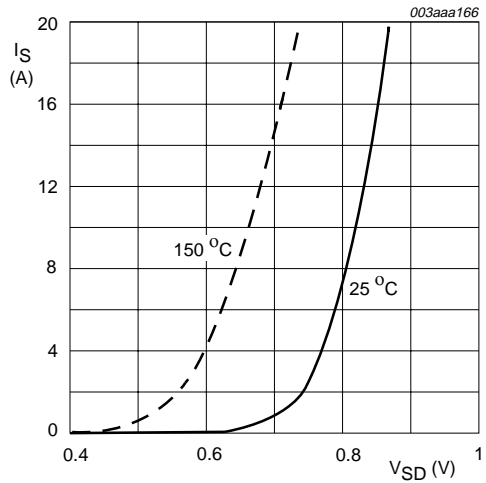
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



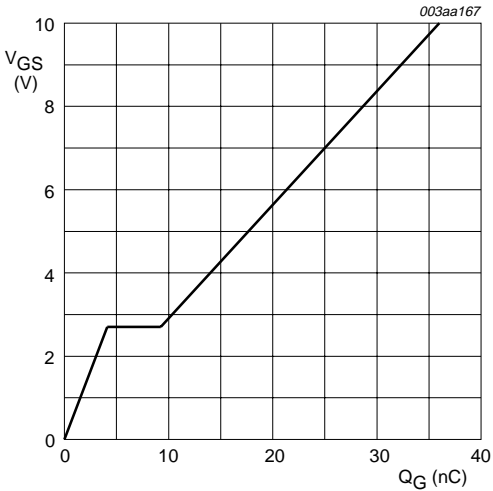
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



$T_j = 25 \text{ °C and } 150 \text{ °C}; V_{GS} = 0 \text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



I<sub>D</sub> = 15 A; V<sub>DD</sub> = 16 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.



6. Package outline

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

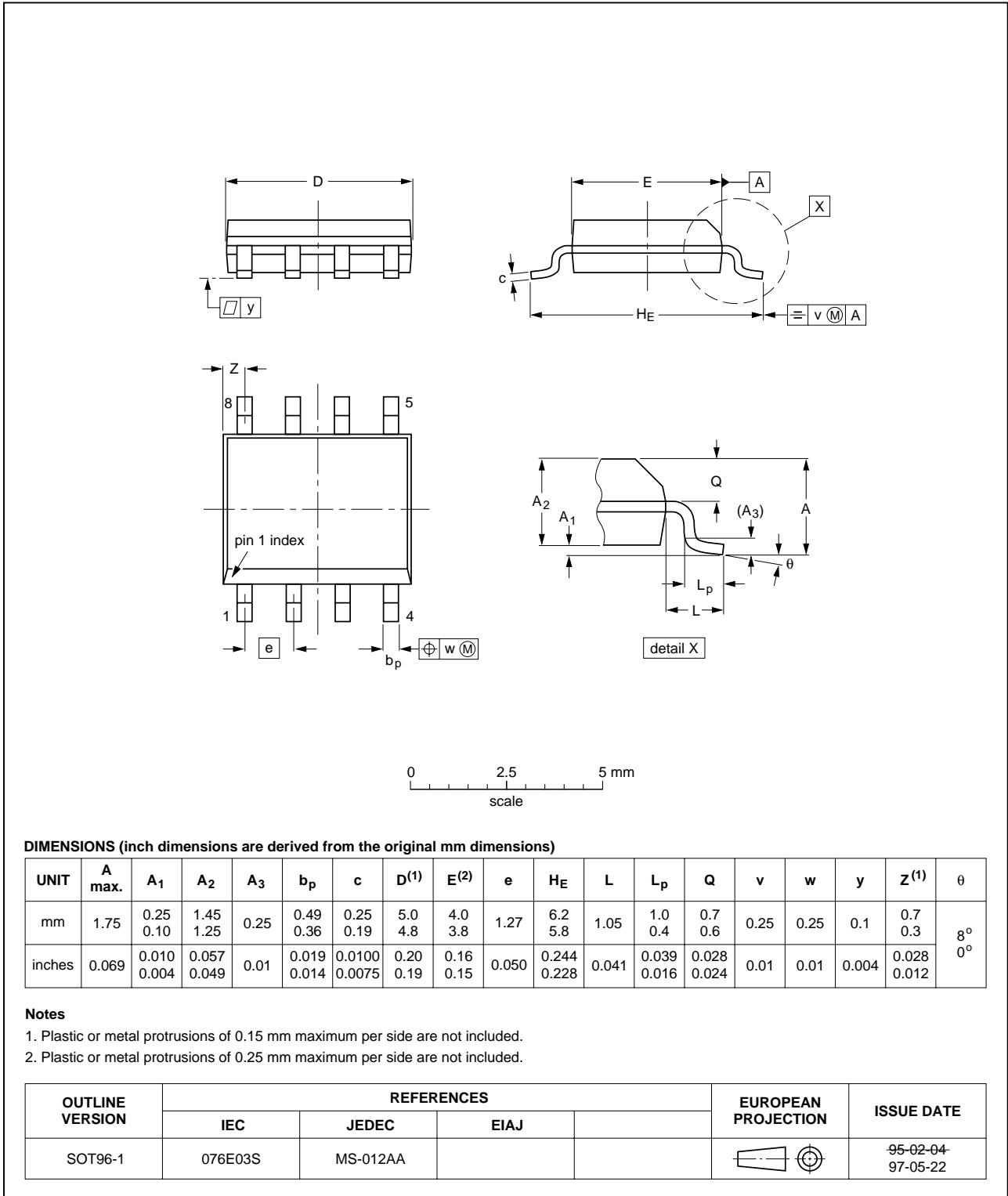


Fig 14. SOT96-1 (S08).

## 7. Revision history

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Table 5: Revision history

Rev	Date	CPCN	Description
02	20020412	-	<b>Product data; version 02. Supersedes data of 15 March 2002.</b> Figure 3 $t_p$ label error corrected.
01	20020315	-	<b>Product data; initial version</b>

## 8. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## Contents

<b>1</b>	<b>Product profile</b> .....	<b>1</b>
1.1	Description .....	1
1.2	Features .....	1
1.3	Applications .....	1
1.4	Quick reference data .....	1
<b>2</b>	<b>Pinning information</b> .....	<b>1</b>
<b>3</b>	<b>Limiting values</b> .....	<b>2</b>
<b>4</b>	<b>Thermal characteristics</b> .....	<b>4</b>
4.1	Transient thermal impedance .....	4
<b>5</b>	<b>Characteristics</b> .....	<b>5</b>
<b>6</b>	<b>Package outline</b> .....	<b>9</b>
<b>7</b>	<b>Revision history</b> .....	<b>10</b>
<b>8</b>	<b>Data sheet status</b> .....	<b>11</b>
<b>9</b>	<b>Definitions</b> .....	<b>11</b>
<b>10</b>	<b>Disclaimers</b> .....	<b>11</b>
<b>11</b>	<b>Trademarks</b> .....	<b>11</b>

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