

DATA SHEET

TDA3505

TDA3506

Video control combination circuit
with automatic cut-off control

Product specification
File under Integrated Circuits, IC02

November 1987

Video control combination circuit with automatic cut-off control

TDA3505
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GENERAL DESCRIPTION

The TDA3505 and TDA3506 are monolithic integrated circuits which perform video control functions in a PAL/SECAM decoder. The TDA3505 is for negative colour difference signals $-(R-Y)$, $-(B-Y)$ and the TDA3506 is for positive colour difference signals $+(R-Y)$, $+(B-Y)$.

The required input signals are: luminance and colour difference (negative or positive) and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages. The circuits provide automatic cut-off control of the picture tube.

Features

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G-Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Peak beam current limiting input
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- 3 DC gain controls for the RGB output signals (white point adjustment)
- Emitter-follower outputs for driving the RGB output stages
- Input for automatic cut-off control with compensation for leakage current of the picture tube

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 6)		$V_P = V_{6-24}$	–	12	–	V
Supply current		$I_P = I_6$	–	95	–	mA
Composite video input signal (peak-to-peak value)		$V_{15-24(p-p)}$	–	0,45	–	V
Colour difference input signals (peak-to-peak value)						
$-(B-Y)$ or $+(B-Y)$ respectively		$V_{18-24(p-p)}$	–	1,33	–	V
$-(R-Y)$ or $+(R-Y)$ respectively		$V_{17-24(p-p)}$	–	1,05	–	V
Inserted RGB signals (black-to-white value)		$V_{12,13,14-24}$	–	1,0	–	V
Three-level sandcastle pulse		V_{10-24}	–	2,5	–	V
			–	4,5	–	V
			–	8,0	–	V
Control voltage ranges						
brightness		V_{20-24}	1,0	–	3,0	V
contrast		V_{19-24}	2,0	–	4,3	V
saturation		V_{16-24}	2,0	–	4,3	V

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117); SOT117-1; 1996 November 20.

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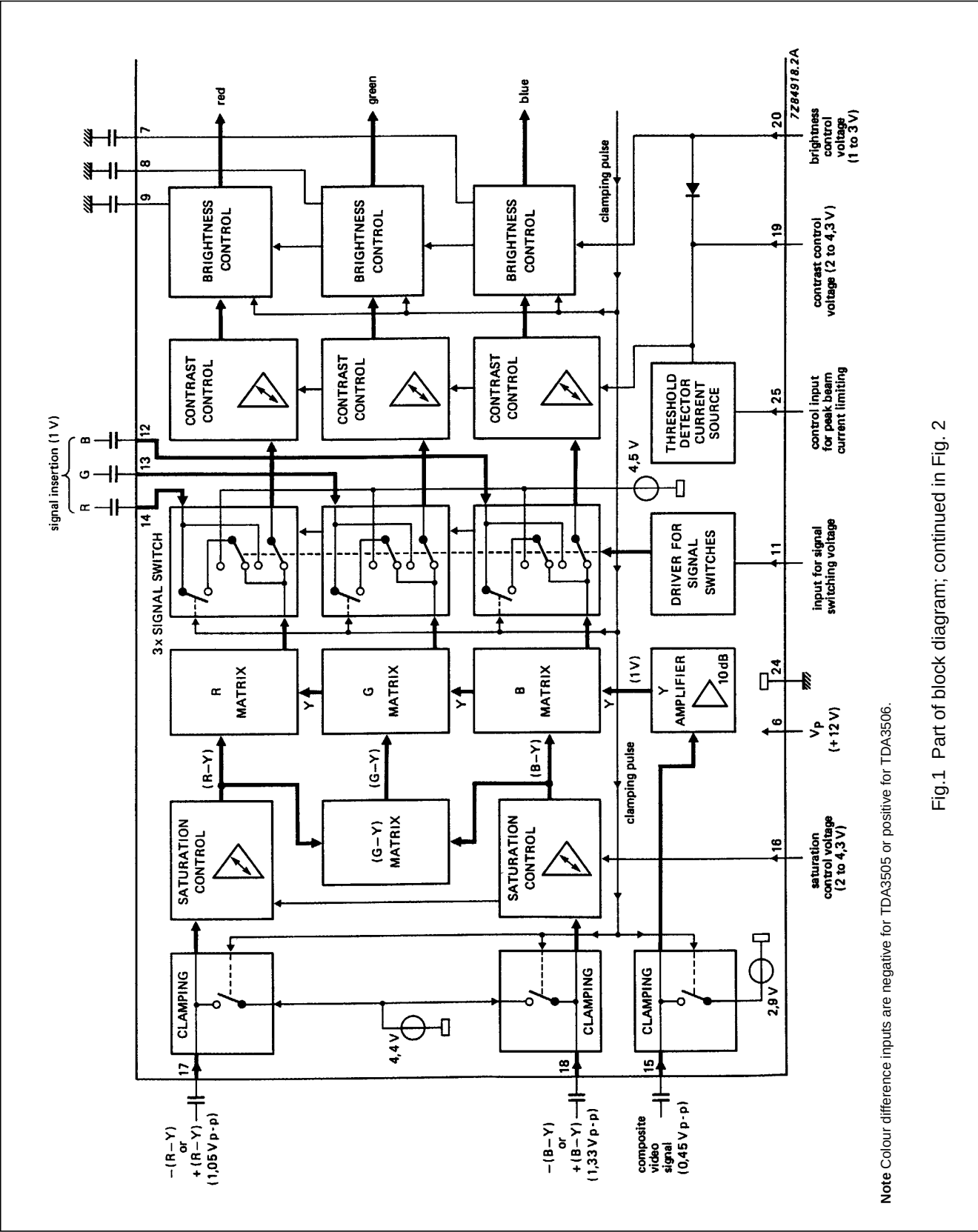


Fig.1 Part of block diagram; continued in Fig. 2

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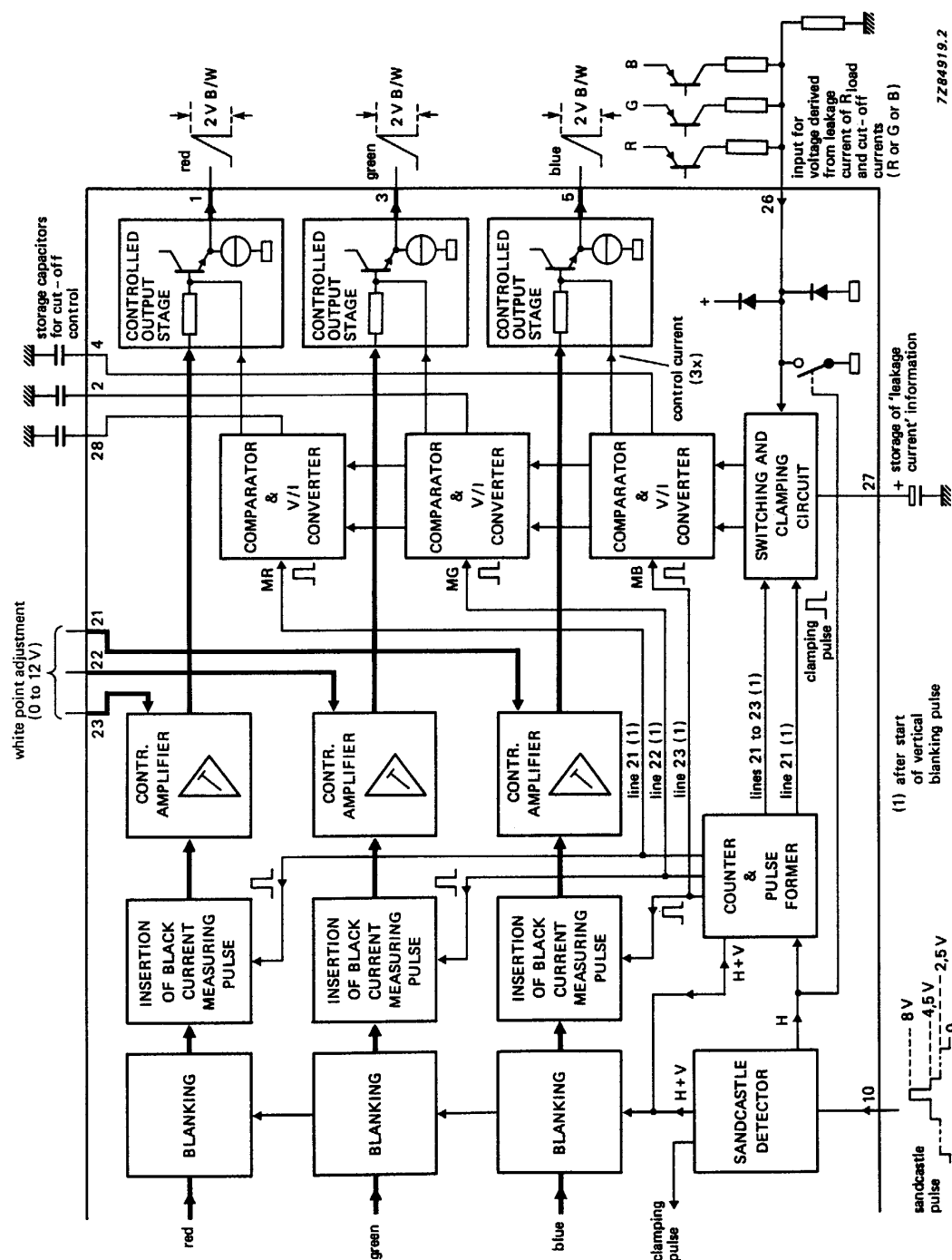


Fig.2 Part of block diagram; continued from Fig. 1

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PINNING

PIN	DESCRIPTION
1	red output
2	green storage capacitor for cut-off control
3	green output
4	blue storage capacitor for cut-off control
5	blue output
6	positive supply voltage (+ 12 V)
7	blue storage for brightness
8	green storage for brightness
9	red storage for brightness
10	sandcastle pulse input
11	fast switch for RGB inputs
12	blue input (external signal)
13	green input (external signal)
14	red input (external signal)
15	luminance input
16	saturation control input
17	colour difference input – (R-Y) or + (R-Y) respectively
18	colour difference input – (B-Y) or + (B-Y) respectively
19	contrast control input
20	brightness control input
21	white point adjustment, blue
22	white point adjustment, green
23	white point adjustment, red
24	ground (0 V)
25	control input for peak beam current limiting
26	automatic cut-off control input
27	storage capacitor for leakage current
28	red storage capacitor for cut-off control

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage (pin 6)	$V_P = V_{6-24}$	—	13,2	V
Voltage ranges				
at pins 10, 21, 22, 23, 25, 26	V_{n-24}	0	V_P	V
at pin 11	V_{11-24}	−0,5	3,0	V
at pins 16, 19, 20	$V_{16, 19, 20-24}$	0	$0,5V_P$	V
at pins 1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 15, 17, 18, 27, 28	no external DC voltage			
Currents				
at pins 1, 3, 5	$-I_{1, 3, 5}$	—	3	mA
at pin 19	I_{19}	—	10	mA
at pin 20	I_{20}	—	5	mA
at pin 25	$-I_{25}$	—	5	mA
Total power dissipation	P_{tot}	—	1,7	W
Storage temperature range	T_{stg}	−25	+150	°C
Operating ambient temperature range	T_{amb}	0	+70	°C

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CHARACTERISTICS

$V_P = V_{6-24} = 12,0 \text{ V}$; $V_{12, 13, 14(p-p)} = 1,0 \text{ V}$; $V_{15-24(p-p)} = 0,45 \text{ V}$; $V_{17-24(p-p)} = 1,05 \text{ V}$; $V_{18-24(p-p)} = 1,33 \text{ V}$; $T_{amb} = 25^\circ\text{C}$; measured in Fig.3; nominal settings of brightness, contrast, saturation and white point adjustment; all voltages are referred to pin 24; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply (pin 6)						
Supply voltage		$V_P = V_6$	10,8	12,0	13,2	V
Supply current		I_P	—	95	125 ⁽¹⁾	mA
Colour difference inputs (pins 17, 18)						
(R-Y) input signal (pin 17) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{17(p-p)}$	—	1,05	1,48	V
(B-Y) input signal (pin 18) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	$V_{18(p-p)}$	—	1,33	1,88	V
Input current during scanning		$I_{17, 18}$	—	—	1,0	μA
Input resistance		$R_{17, 18-24}$	1,0	—	—	M Ω
Internal DC voltage due to clamping	note 2	$V_{17, 18}$	3,8	4,4	4,8	V
Saturation control (pin 16)						
Control voltage for maximum saturation	note 2	V_{16}	4,0	4,2	4,4	V
Control voltage for nominal saturation	6 dB below max. note 2	V_{16}	2,9	3,1	3,3	V
Control voltage for -26 dB saturation referred to maximum	note 2	V_{16}	1,9	2,1	2,3	V
Minimum saturation	$V_{16} = 1,8 \text{ V}$	d	46	50	—	dB
Input current		I_{16}	—	—	20	μA
(G-Y) matrix						
Matrixed according to the equation $V_{(G-Y)} = -0,51 V_{(R-Y)} - 0,19 V_{(B-Y)}$						

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Luminance input (pin 15)						
Composite video input signal (peak-to-peak value)		$V_{15(p-p)}$	—	450	630	mV
Input resistance		R_{15-24}	100	—	—	k Ω
Input capacitance		C_{15-24}	—	—	5	pF
Input current during scanning		I_{15}	—	—	1	μ A
Linearity	nominal settings	m	0,85	—	—	
Internal DC voltage due to clamping	note 2	V_{15}	2,5	2,9	3,3	V
RGB channels						
<i>Signal switching input (pin 11)</i>						
Normal state; no insertion		V_{11}	0	—	0,4	V
Level for insertion-on		V_{11}	0,9	—	3,0	V
Input capacitance		C_{11-24}	—	—	10	pF
Input current	$V_{11} = 0$ to 3 V	I_{11}	−100	—	+450	μ A
<i>Signal insertion</i> (pins 12, 13, 14)						
External RGB input signals (black-to-white value)		$V_{12, 13, 14}$	—	1,0	1,4	V
Input current during scanning		$I_{12, 13, 14}$	—	—	1,0	μ A
Internal DC voltage due to clamping	notes 2, 3	$V_{12, 13, 14}$	4,0	4,5	5,0	V
Contrast control (pin 19)	note 2					
Control voltage for maximum contrast		V_{19}	4,0	4,2	4,4	V
Control voltage for nominal contrast	3 dB below max.	V_{19}	3,4	3,6	3,8	V
Control voltage for −10 dB below max.		V_{19}	2,6	2,8	3,0	V
Minimum contrast referred to max.	$V_{19} = 2$ V	d	18	21	29	dB
Input current	$V_{25} > 6$ V	I_{19}	—	—	2	μ A
Difference between RGB channels	contrast −10 dB below max.		—	—	0,6	dB

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Peak beam current limiting (pin 25)						
Internal DC bias voltage	note 2	V_{25}	5,3	5,5	5,7	V
Input resistance		R_{25-24}	—	10	—	k Ω
Input current at contrast control input	$V_{25} = 4,5$ V	I_{19}	10	20	34	mA
Brightness code (pin 20)	note 2					
Control voltage range		V_{20}	1	—	3	V
Input current		$-I_{20}$	—	—	10	μ A
Change of black level in the control range related to the luminance signal (black/white)	$\Delta V_{20} = 1$ V		—	± 50	—	%
Tracking			95	—	—	%
Internal signal limiting (RGB)						
Signal limiting referred to nominal luminance and nominal black level						
black			—	—25	—	%
white			115	120	125	%
White point adjustment (pins 21, 22, 23)	note 2					
AC voltage gain	note 4					
$V_{21, 22, 23} = 5,5$ V		G_v	—	100	—	%
$V_{21, 22, 23} = 0$ V		G_v	—35	—40	—	%
$V_{21, 22, 23} = 12$ V		G_v	+35	+40	—	%
Input resistance		$R_{21,22,23-24}$	—	20	—	k Ω

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
RGB outputs (emitter follower) (pins 1, 3, 5)						
Output voltage; black-to-white positive		$V_{1, 3, 5}$	1,5	2,0	2,5	V
Black level without automatic cut-off control	note 2; $V_{28,2,4} = 10 \text{ V}$	$V_{1, 3, 5}$	6,1	6,9	7,7	V
Difference in black level between RGB channels due to variation of contrast control		$\Delta V_{1, 3, 5}$	—	—	10	mV
Cut-off control range	note 2	$V_{1, 3, 5}$	4,0	4,6	—	V
Internal current source		$I_{1, 3, 5}$	2,0	3,0	—	mA
Automatic cut-off control (pin 26)	notes 2, 5					
Input voltage range		V_{26}	0	—	6,5	V
Voltage difference between cut-off current measurement (note 6) and leakage current measurement (note 7)		V_{26}	0,5	0,64	0,72	V
<i>Input pin 26 switches to ground during horizontal flyback</i>						
Gain data	at nominal brightness, contrast, saturation and white point settings					
Voltage gain with respect to luminance input (pin 15)		$G_{1,3,5-15}$	14	16	18	dB
Frequency response of luminance path	0 to 5 MHz	$d_{1,3,5-15}$	—	—	3	dB
Voltage gain with respect to colour difference inputs (pins 17 and 18)		G_{5-18} G_{1-17}	3	6	9	dB
Frequency response of colour difference paths	0 to 2 MHz	d_{5-18} d_{1-17}	—	—	3	dB

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage gain with respect to inserted signals		G_{1-14} G_{3-13} G_{5-12}	4	6	8	dB
Frequency response of inserted signal paths	0 to 10 MHz	d_{1-14} d_{3-13} d_{5-12}	—	—	3	dB
Rise and fall times of RGB output signals (pins 1, 3, 5)		t_r, t_f	—	40	—	ns
Difference in transit times between R, G and B channels		$\Delta t_{1, 3, 5}$	—	0	15	ns
Delay time between signal switching and signal insertion		t_d	−25	—	+25	ns
Difference in gain between normal mode and signal insertion mode		$\Delta G_{1,3,5}$	—	—	10	%
Sandcastle pulse detector (pin 10)	note 8					
Levels for separating the following pulses:						
horizontal and vertical blanking pulses	note 9	V_{10}	1,0	1,5	2,0	V
required pulses (H+V)		V_{10}	2,1	2,5	2,9	V
horizontal pulses		V_{10}	3,0	3,5	4,0	V
required pulses (H)		V_{10}	4,1	4,5	5,0	V
clamping pulses	note 10	V_{10}	6,5	7,0	7,5	V
required pulses		V_{10}	7,6	—	12,0	V
no keying		V_{10}	—	—	1,0	V
Input current		$-I_{10}$	—	—	110	μA

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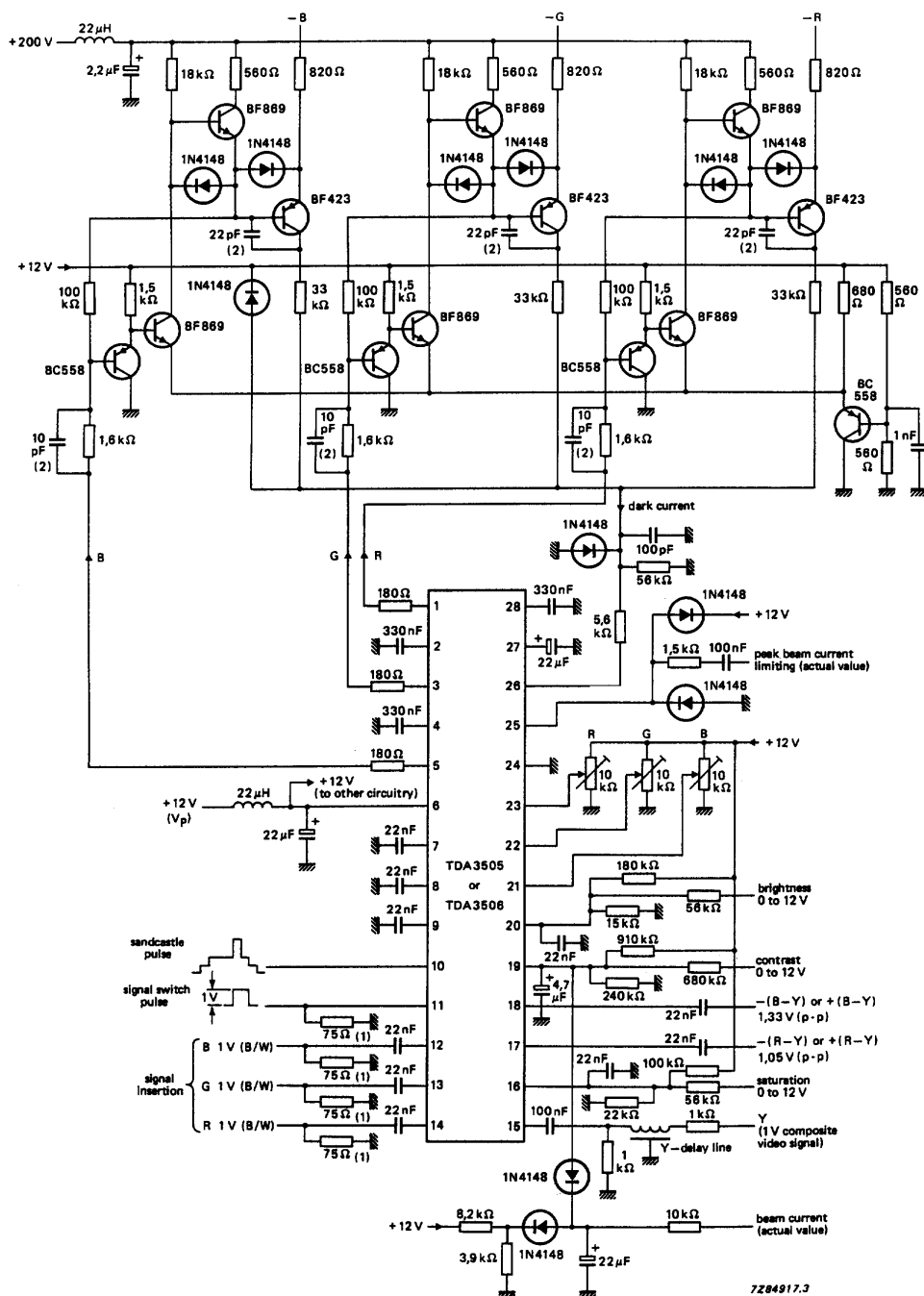
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Notes

1. < 110 mA after warm-up.
2. Values are proportional to the supply voltage.
3. When $V_{11-24} < 0,4$ V during clamping time - the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.
When $V_{11-24} > 0,9$ V during clamping time - the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
4. When pins 21, 22 and 23 are not connected, an internal bias voltage of 5,5 V is supplied.
5. Automatic cut-off control measurement occurs in the following lines after start of the vertical blanking pulse:
line 20: measurement of leakage current (R + G + B)
line 21: measurement of red cut-off current
line 22: measurement of green cut-off current
line 23: measurement of blue cut-off current
6. Black level of the measured channel is nominal; the other two channels are blanked to ultra-black.
7. All three channels blanked to ultra-black.
The cut-off control cycle occurs when the vertical blanking part of the sandcastle pulse contains more than 3 line pulses.
The internal blanking continues until the end of the last measured line.
The vertical blanking pulse is not allowed to contain more than 34 line pulses, otherwise another control cycle begins.
8. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
9. Blanked to ultra-black (–25%).
10. Pulse duration $\geq 3,5$ μ s.

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- (1) When supplied via a 75 Ω line.
(2) Capacitor value depends on circuit layout.

Fig.3 Typical application circuit diagram using TDA3505 or TDA3506; colour difference inputs are negative for TDA3505 or positive for TDA3506.

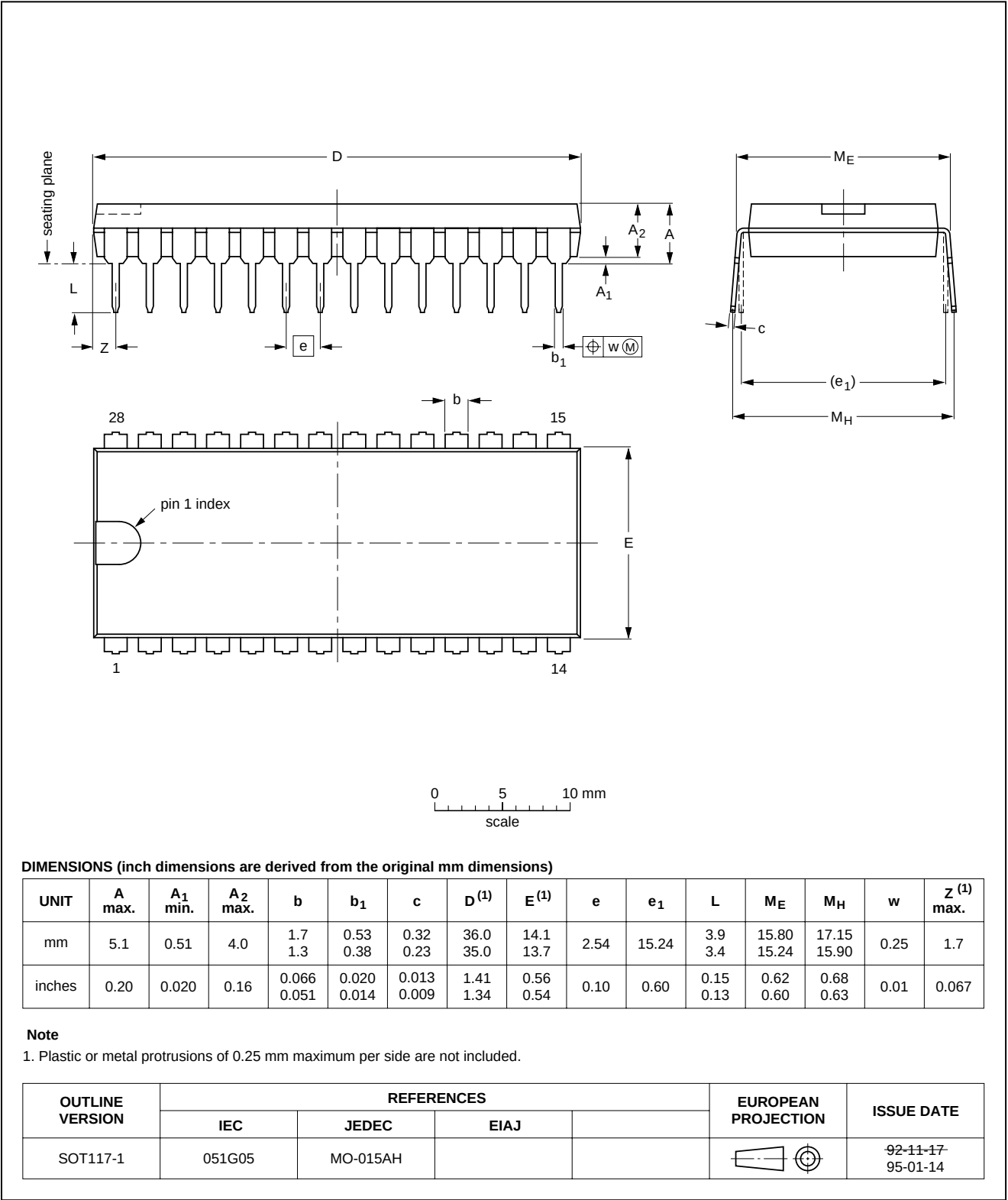
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PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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