

DATA SHEET

TDA8763

**10-bit high-speed low-power ADC
with internal reference regulator**

Product specification
Supersedes data of 1997 Feb 10
File under Integrated Circuits, IC02

1999 Jan 06

10-bit high-speed low-power ADC with internal reference regulator

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FEATURES

- 10-bit resolution
- Sampling rate up to 50 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 4.43 MHz full-scale input at $f_{\text{clk}} = 40$ MHz)
- No missing codes guaranteed
- In-Range (IR) CMOS output
- Levels TTL and CMOS compatible digital inputs
- 3 to 5 V CMOS digital outputs
- Low-level AC clock input signal allowed
- Internal reference voltage regulator
- Power dissipation only 235 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- $\Sigma\Delta$ modulators
- Medical imaging.

GENERAL DESCRIPTION

The TDA8763 is a 10-bit high-speed low-power Analog-to-Digital Converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL and CMOS compatible, although a low-level sine wave clock input signal is allowed.

The device includes an internal voltage reference regulator. If the application requires that the reference is driven via external sources the recommendation is to use the TDA8763A.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8763M/3	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1	30
TDA8763M/4	SSOP28		SOT341-1	40
TDA8763M/5	SSOP28		SOT341-1	50

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	30	35	mA
I_{CCD}	digital supply current		–	16	21	mA
I_{CCO}	output stages supply current	$f_{clk} = 40$ MHz; ramp input	–	1	2	mA
INL	integral non-linearity	$f_{clk} = 40$ MHz; ramp input	–	± 0.8	± 2.0	LSB
DNL	differential non-linearity	$f_{clk} = 40$ MHz; ramp input	–	± 0.5	± 0.9	LSB
$f_{clk(max)}$	maximum clock frequency					
	TDA8763M/3		30	–	–	MHz
	TDA8763M/4		40	–	–	MHz
	TDA8763M/5		50	–	–	MHz
P_{tot}	total power dissipation	$f_{clk} = 40$ MHz; ramp input	–	235	305	mW

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BLOCK DIAGRAM

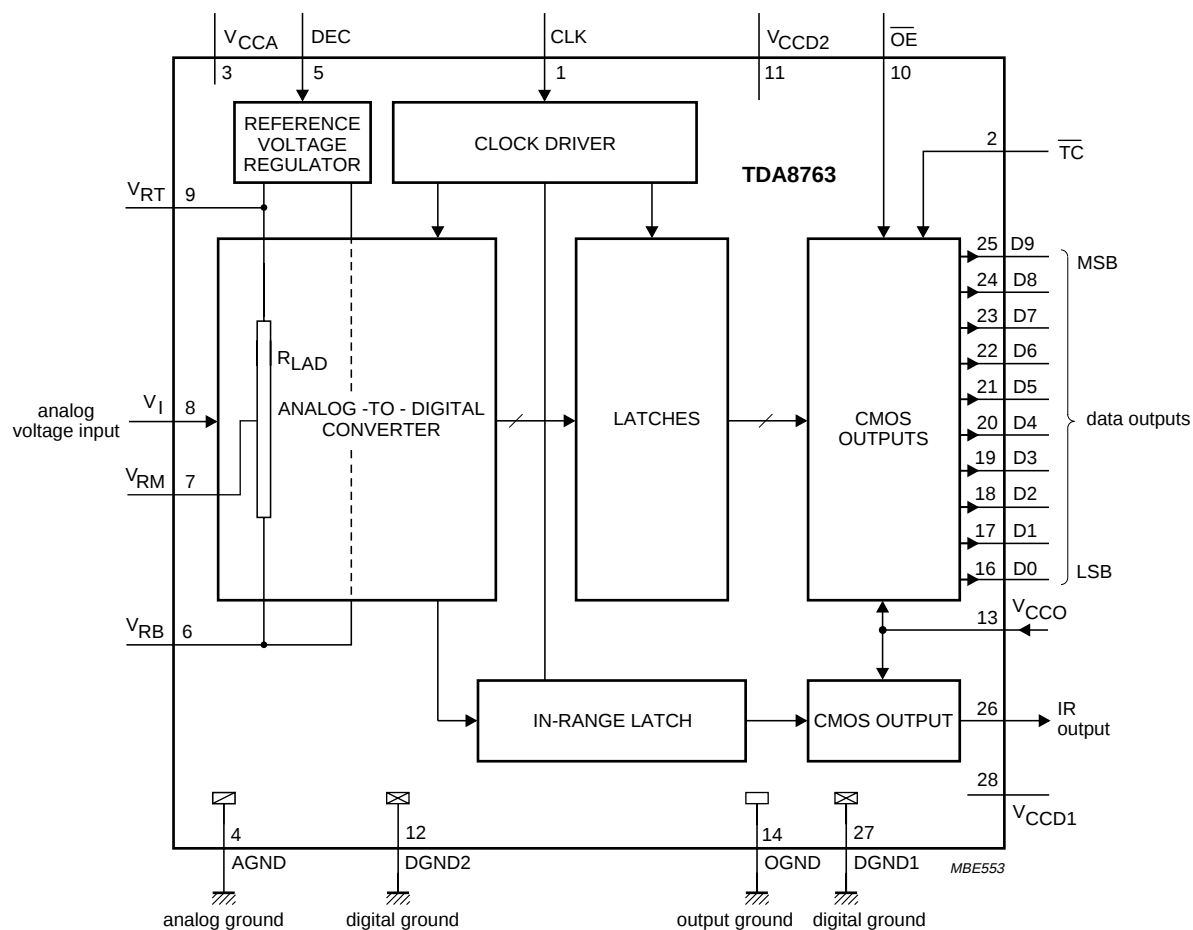


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V _{CCA}	3	analog supply voltage (+5 V)
AGND	4	analog ground
DEC	5	decoupling input
V _{RB}	6	reference voltage BOTTOM input
V _{RM}	7	reference voltage MIDDLE input
V _I	8	analog input voltage
V _{RT}	9	reference voltage TOP input
$\overline{OE}$	10	output enable input (CMOS level input, active LOW)
V _{CCD2}	11	digital supply voltage 2 (+5 V)
DGND2	12	digital ground 2
V _{CCO}	13	supply voltage for output stages (3 to 5 V)
OGND	14	output ground
n.c.	15	not connected
D0	16	data output; bit 0 (LSB)
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (MSB)
IR	26	in range data output
DGND1	27	digital ground 1
V _{CCD1}	28	digital supply voltage 1 (+5 V)

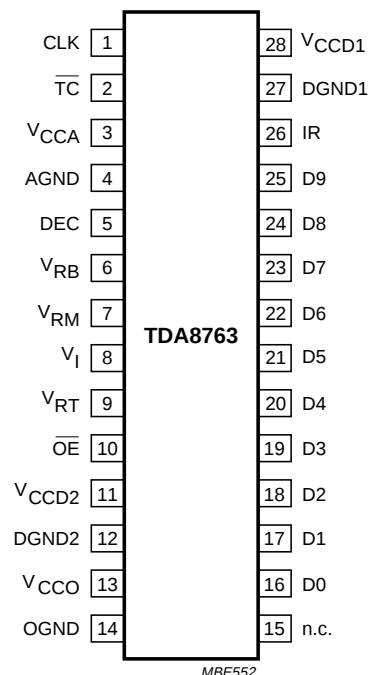


Fig.2 Pin configuration.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	−0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	−0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	$V_{CCA} - V_{CCD}$		−1.0	+1.0	V
	$V_{CCA} - V_{CCO}$		−1.0	+4.0	V
	$V_{CCD} - V_{CCO}$		−1.0	+4.0	V
V_I	input voltage	referenced to AGND	−0.3	+7.0	V
$V_{i(sw)(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	−	V_{CCD}	V
I_O	output current		−	10	mA
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
T_j	junction temperature		−	150	°C

Note

1. The supply voltages V_{CCA} , V_{CCD} and V_{CCO} may have any value between −0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	110	K/W

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CHARACTERISTICS

$V_{CCA} = V_3$ to $V_4 = 4.75$ to 5.25 V; $V_{CCD} = V_{11}$ to V_{12} and V_{28} to $V_{27} = 4.75$ to 5.25 V; $V_{CCO} = V_{13}$ to $V_{14} = 3.0$ to 5.25 V; AGND and DGND shorted together; $T_{amb} = 0$ to $+70$ °C; typical values measured at $V_{CCA} = V_{CCD} = 5$ V and $V_{CCO} = 3.3$ V; $C_L = 15$ pF and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD1}	digital supply voltage 1		4.75	5.0	5.25	V
V_{CCD2}	digital supply voltage 2		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		3.0	3.3	5.25	V
ΔV_{CC}	supply voltage difference					
	$V_{CCA} - V_{CCD}$		-0.20	–	+0.20	V
	$V_{CCA} - V_{CCO}$		-0.20	–	+2.25	V
	$V_{CCD} - V_{CCO}$		-0.20	–	+2.25	V
I_{CCA}	analog supply current		–	30	35	mA
I_{CCD}	digital supply current		–	16	21	mA
I_{CCO}	output stages supply current	$f_{clk} = 40$ MHz; ramp input	–	1	2	mA
Inputs						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{clk} = 0.8$ V	-1	0	+1	μA
I_{IH}	HIGH-level input current	$V_{clk} = 2$ V	–	2	10	μA
Z_i	input impedance	$f_{clk} = 40$ MHz	–	2	–	kΩ
C_i	input capacitance		–	2	–	pF
INPUTS $\overline{OE}$ AND $\overline{TC}$ (REFERENCED TO DGND); see Table 2						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.8$ V	-1	–	–	μA
I_{IH}	HIGH-level input current	$V_{IH} = 2$ V	–	–	1	μA
V_i (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
I_{IL}	LOW-level input current	$V_i = V_{RB} = 1.3$ V	–	0	–	μA
I_{IH}	HIGH-level input current	$V_i = V_{RT} = 3.67$ V	–	35	–	μA
Z_i	input impedance	$f_i = 4.43$ MHz	–	8	–	kΩ
C_i	input capacitance		–	5	–	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder using the internal voltage regulator; see Table 1						
V_{RB}	reference voltage BOTTOM		1.1	1.3	1.5	V
V_{RT}	reference voltage TOP		3.4	3.6	3.8	V
V_{diff}	differential reference voltage $V_{RT} - V_{RB}$		2.25	2.3	2.35	V
I_{ref}	reference current		–	9.39	–	mA
R_{lad}	resistor ladder		–	245	–	Ω
TC_{Rlad}	temperature coefficient of the resistor ladder		–	1860	–	ppm
			–	456	–	m Ω /K
$V_{offset(B)}$	offset voltage BOTTOM	note 2	–	175	–	mV
$V_{offset(T)}$	offset voltage TOP	note 2	–	175	–	mV
$V_{i(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.90	1.95	2.00	V
Outputs						
DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW-level output voltage	$I_{OL} = 1 \text{ mA}$	0	–	0.5	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -1 \text{ mA}$	$V_{CCO} - 0.5$	–	V_{CCO}	V
I_{OZ}	output current in 3-state mode	$0.5 \text{ V} < V_o < V_{CCO}$	–20	–	+20	μA
Switching characteristics						
CLOCK INPUT CLK; see Fig.4; note 1						
$f_{clk(max)}$	maximum clock frequency					
	TDA8763M/3		30	–	–	MHz
	TDA8763M/4		40	–	–	MHz
	TDA8763M/5		50	–	–	MHz
t_{CPH}	clock pulse width HIGH	full effective bandwidth	8.5	–	–	ns
t_{CPL}	clock pulse width LOW	full effective bandwidth	5.5	–	–	ns
Analog signal processing						
LINEARITY						
INL	integral non-linearity	$f_{clk} = 40 \text{ MHz}$; ramp input	–	± 0.8	± 2.0	LSB
DNL	differential non-linearity	$f_{clk} = 40 \text{ MHz}$; ramp input	–	± 0.5	± 0.9	LSB
E_{offset}	offset error	middle code	–	± 1	–	LSB
E_G	gain error (from device to device) using internal reference voltage	note 4	–	± 3	–	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BANDWIDTH ($f_{\text{clk}} = 40 \text{ MHz}$)						
B	analog bandwidth	full-scale sine wave; note 5	–	15	–	MHz
		75% full-scale sine wave; note 5	–	20	–	MHz
		small signal at mid-scale; $V_I = \pm 10 \text{ LSB}$ at code 512; note 5	–	350	–	MHz
t_{stLH}	analog input settling time LOW-to-HIGH	full-scale square wave; see Fig.6; note 6	–	1.5	3.0	ns
t_{stHL}	analog input settling time HIGH-to-LOW	full-scale square wave; see Fig.6; note 6	–	1.5	3.0	ns
HARMONICS ($f_{\text{clk}} = 40 \text{ MHz}$); see Figs 7 and 8						
$H_{\text{fund(FS)}}$	fundamental harmonics (full-scale)	$f_i = 4.43 \text{ MHz}$	–	–	0	dB
$H_{\text{all(FS)}}$	harmonics (full-scale); all components	$f_i = 4.43 \text{ MHz}$				
	second harmonics		–	–70	–63	dB
	third harmonics		–	–72	–63	dB
THD	total harmonic distortion	$f_i = 4.43 \text{ MHz}$	–	–61	–	dB
SIGNAL-TO-NOISE RATIO; see Figs 7 and 8; note 7						
SNR_{FS}	signal-to-noise ratio (full-scale)	without harmonics; $f_{\text{clk}} = 40 \text{ MHz}$; $f_i = 4.43 \text{ MHz}$	55	58	–	dB
EFFECTIVE BITS; see Figs 7 and 8; note 7						
EB	effective bits	TDA8763M/3; $f_{\text{clk}} = 30 \text{ MHz}$				
		$f_i = 4.43 \text{ MHz}$	–	9.4	–	bits
		$f_i = 7.5 \text{ MHz}$	–	9.1	–	bits
		TDA8763M/4; $f_{\text{clk}} = 40 \text{ MHz}$				
		$f_i = 4.43 \text{ MHz}$	–	9.3	–	bits
		$f_i = 7.5 \text{ MHz}$	–	9.0	–	bits
		$f_i = 10 \text{ MHz}$	–	8.9	–	bits
		$f_i = 15 \text{ MHz}$	–	8.1	–	bits
		TDA8763M/5; $f_{\text{clk}} = 50 \text{ MHz}$				
		$f_i = 4.43 \text{ MHz}$	–	9.3	–	bits
		$f_i = 7.5 \text{ MHz}$	–	8.9	–	bits
		$f_i = 10 \text{ MHz}$	–	8.8	–	bits
		$f_i = 15 \text{ MHz}$	–	8.0	–	bits

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TWO-TONE; note 8						
TTIR	two-tone intermodulation rejection	$f_{\text{clk}} = 40 \text{ MHz}$	–	–69	–	dB
BIT ERROR RATE						
BER	bit error rate	$f_{\text{clk}} = 50 \text{ MHz};$ $f_i = 4.43 \text{ MHz};$ $V_I = \pm 16 \text{ LSB at code 512}$	–	10^{-13}	–	times/ sample
DIFFERENTIAL GAIN; note 9						
G_{diff}	differential gain	$f_{\text{clk}} = 40 \text{ MHz};$ PAL modulated ramp	–	0.8	–	%
DIFFERENTIAL PHASE; note 9						
ϕ_{diff}	differential phase	$f_{\text{clk}} = 40 \text{ MHz};$ PAL modulated ramp	–	0.4	–	deg
Timing ($f_{\text{clk}} = 40 \text{ MHz}; C_L = 15 \text{ pF}$); see Fig.4; note 10						
t_{ds}	sampling delay time		–	3	–	ns
t_{h}	output hold time		4	–	–	ns
t_{d}	output delay time	$V_{\text{CCO}} = 4.75 \text{ V}$	–	10	13	ns
		$V_{\text{CCO}} = 3.15 \text{ V}$	–	12	15	ns
C_L	digital output load capacitance		–	–	15	pF
3-state output delay times; see Fig.5						
t_{dZH}	enable HIGH		–	5.5	8.5	ns
t_{dZL}	enable LOW		–	12	15	ns
t_{dHZ}	disable HIGH		–	19	24	ns
t_{dLZ}	disable LOW		–	12	15	ns

Notes

- In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.
- Analog input voltages producing code 0 up to and including code 1023:
 - $V_{\text{offset(B)}}$ (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM (V_{RB}) at $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$.
 - $V_{\text{offset(T)}}$ (voltage offset TOP) is the difference between reference voltage TOP (V_{RT}) and the analog input which produces data outputs equal to code 1023 at $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$.

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3. In order to ensure the optimum linearity performance of such converter architecture the lower and upper extremities of the converter reference resistor ladder (corresponding to output codes 0 and 1023 respectively) are connected to pins V_{RB} and V_{RT} via offset resistors R_{OB} and R_{OT} as shown in Fig.3.

a) The current flowing into the resistor ladder is $I_L = \frac{V_{RT} - V_{RB}}{R_{OB} + R_L + R_{OT}}$ and the full-scale input range at the converter,

$$\text{to cover code 0 to code 1023, is } V_I = R_L \times I_L = \frac{R_L}{R_{OB} + R_L + R_{OT}} \times (V_{RT} - V_{RB}) = 0.848 \times (V_{RT} - V_{RB})$$

b) Since R_L , R_{OB} and R_{OT} have similar behaviour with respect to process and temperature variation, the ratio

$\frac{R_L}{R_{OB} + R_L + R_{OT}}$ will be kept reasonably constant from device to device. Consequently variation of the output codes at a given input voltage depends mainly on the difference $V_{RT} - V_{RB}$ and its variation with temperature and supply voltage. When several ADCs are connected in parallel and fed with the same reference source, the matching between each of them is then optimized.

$$4. E_G = \frac{(V_{1023} - V_0) - V_{i(p-p)}}{V_{i(p-p)}} \times 100$$

5. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
6. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square wave signal) in order to sample the signal and obtain correct output data.
7. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8 K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio: $SINAD = EB \times 6.02 + 1.76$ dB.
8. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter.
9. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
10. Output data acquisition: the output data is available after the maximum delay time of $t_{d(max)}$. For 50 MHz version it is recommended to have the lowest possible output load.

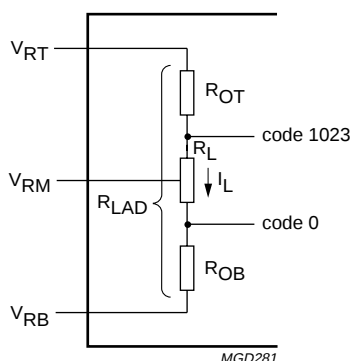


Fig.3 Explanation of note 3.

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Table 1 Output coding and input voltage (typical values; referenced to AGND)

STEP	$V_{i(p-p)}$	IR	BINARY OUTPUT BITS										TWOS COMPLEMENT OUTPUT BITS									
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
U/F	<1.455	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1.455	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1022	.	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
1023	3.405	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
O/F	>3.405	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1

Table 2 Mode selection

TC	OE	D9 to D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

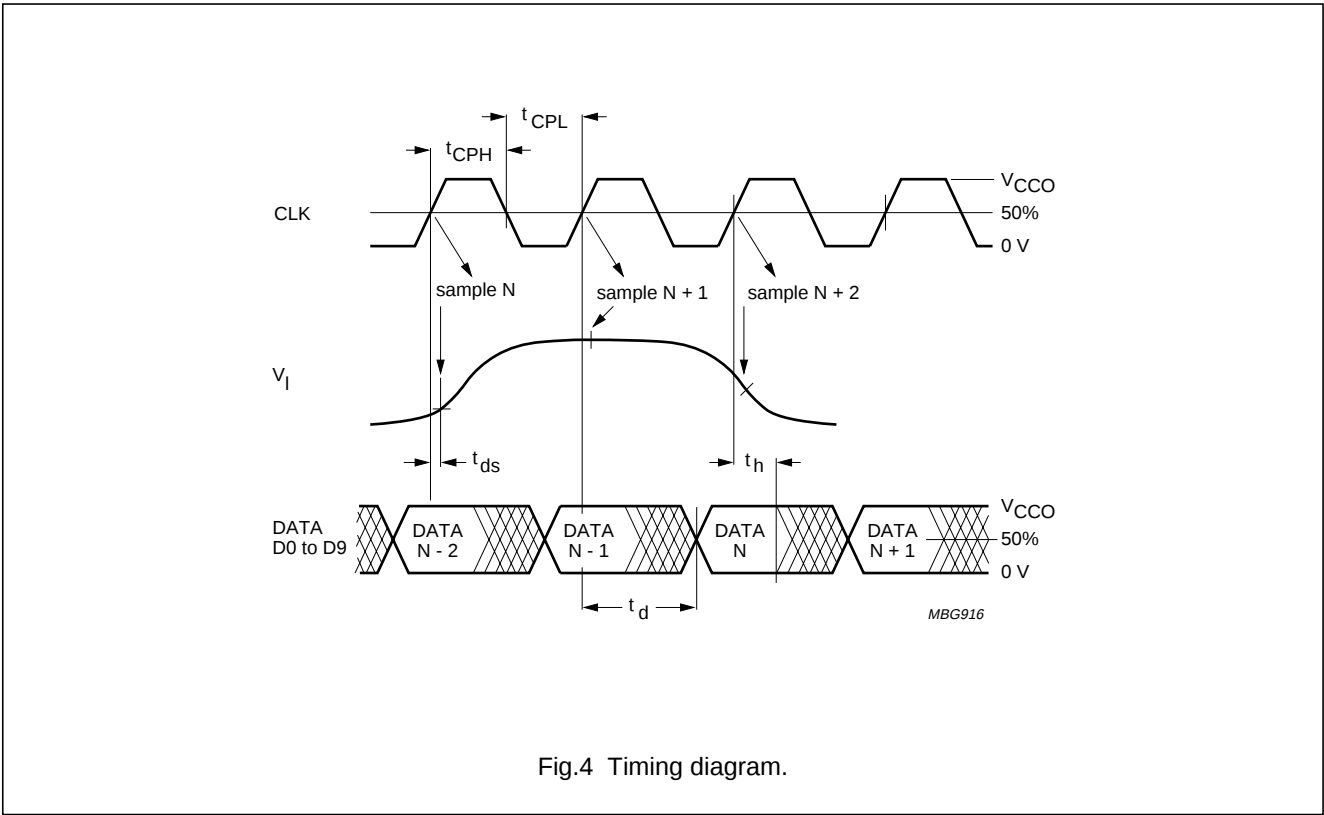
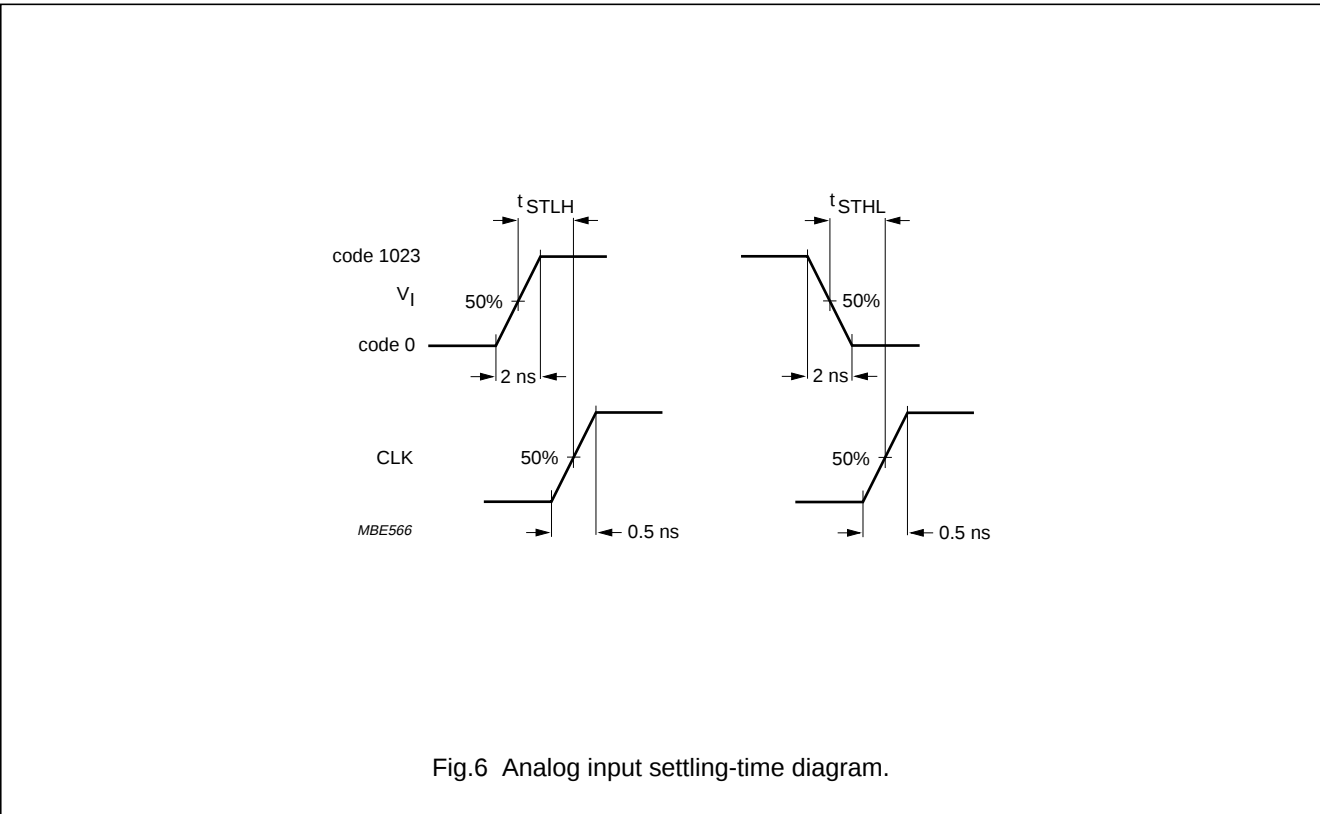
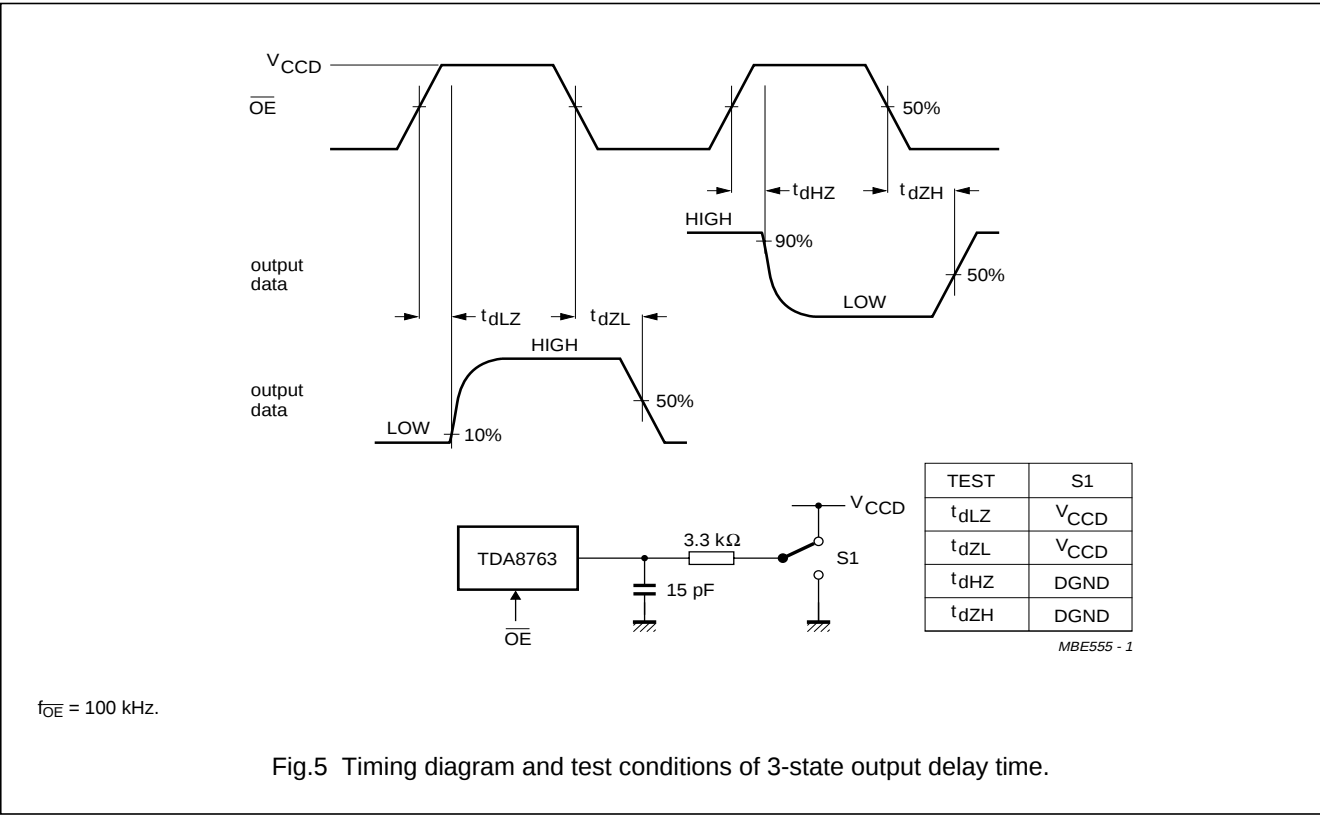


Fig.4 Timing diagram.

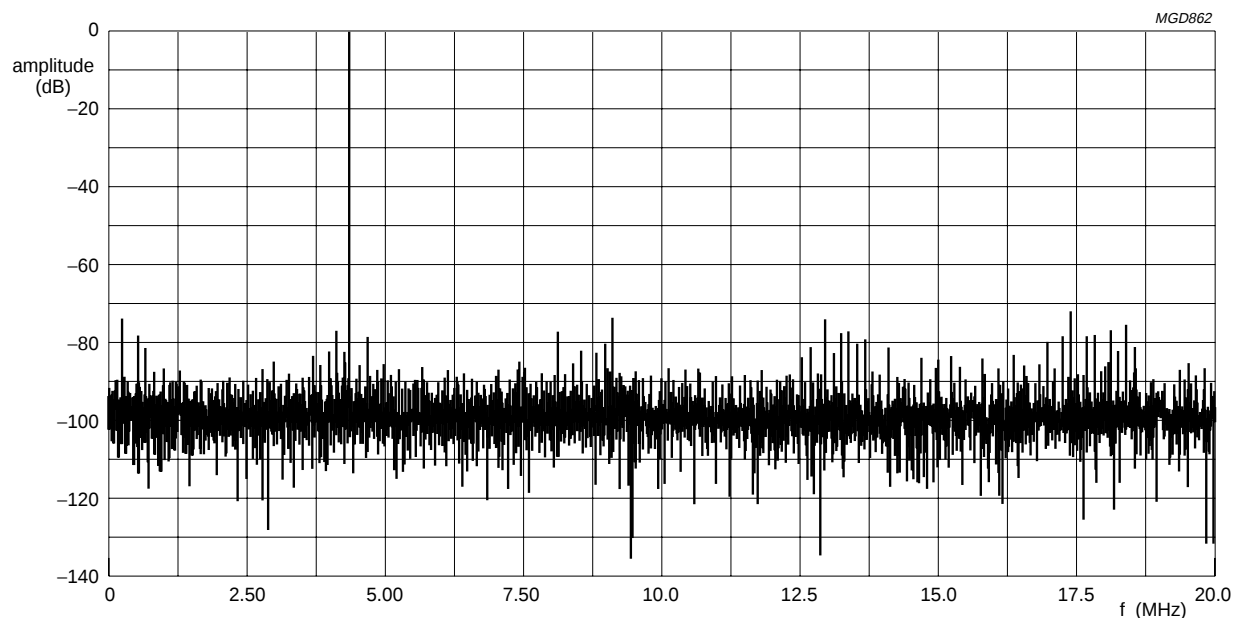
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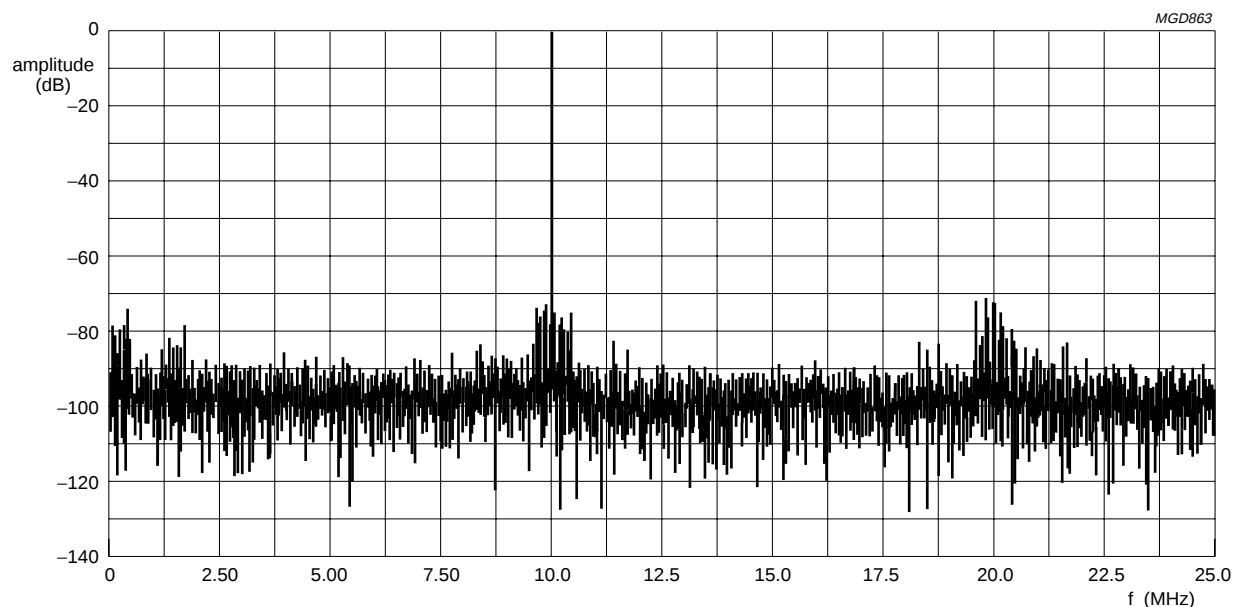
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Effective bits: 9.42; THD = -71.8 dB.
Harmonic levels (dB): 2nd = -83.19; 3rd = -78.09; 4th = -78.72; 5th = -78.33; 6th = -77.55.

Fig.7 Typical Fast Fourier Transform ($f_{\text{clk}} = 40 \text{ MHz}$; $f_i = 4.43 \text{ MHz}$).



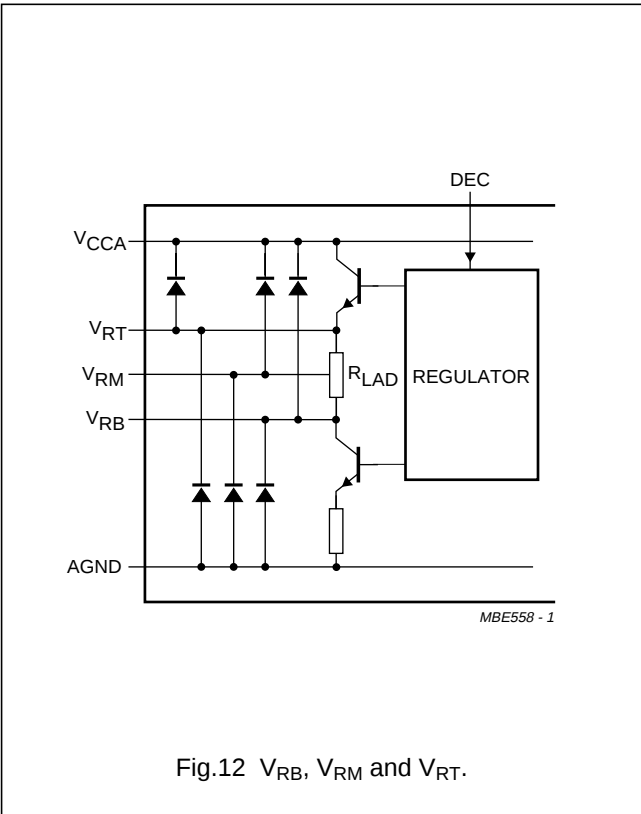
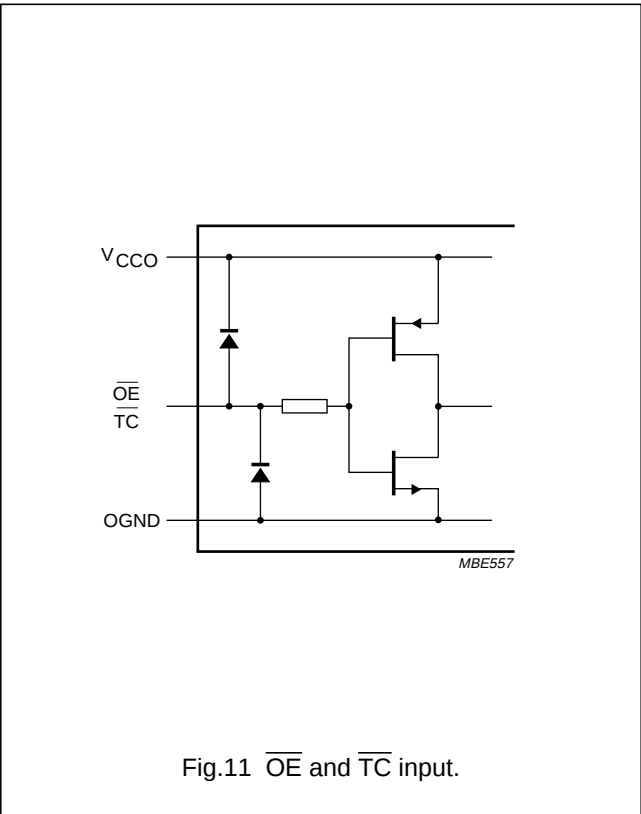
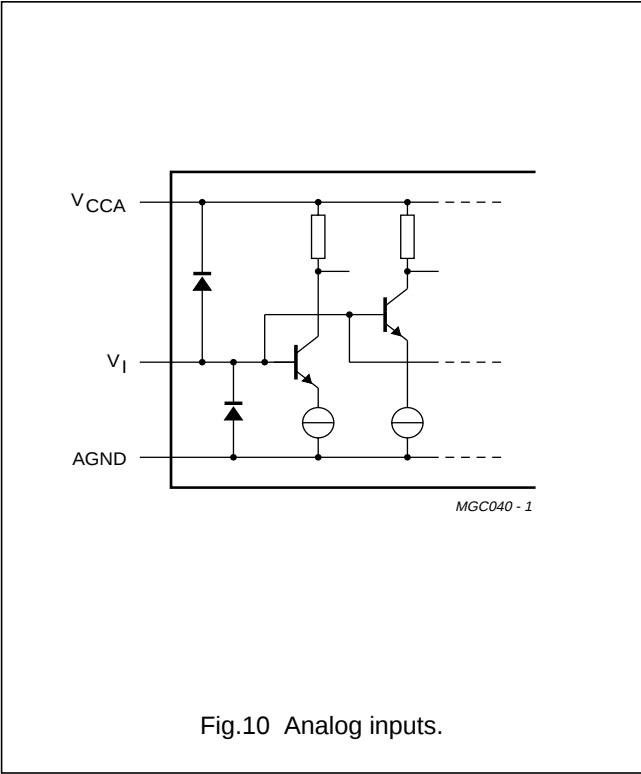
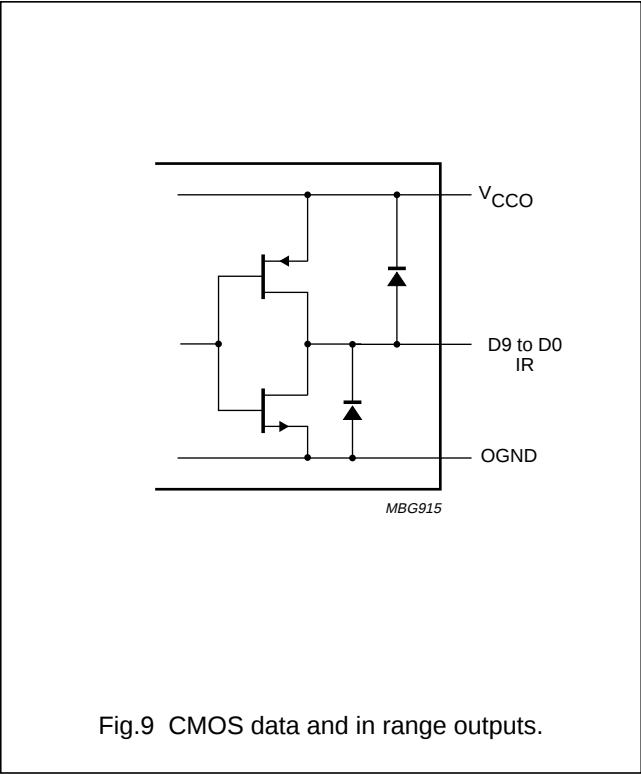
Effective bits: 8.91; THD = -62.96 dB.
Harmonic levels (dB): 2nd = -71.38; 3rd = -71.54; 4th = -74.14; 5th = -65.15; 6th = -77.16.

Fig.8 Typical Fast Fourier Transform ($f_{\text{clk}} = 50 \text{ MHz}$; $f_i = 10 \text{ MHz}$).

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INTERNAL PIN CONFIGURATIONS



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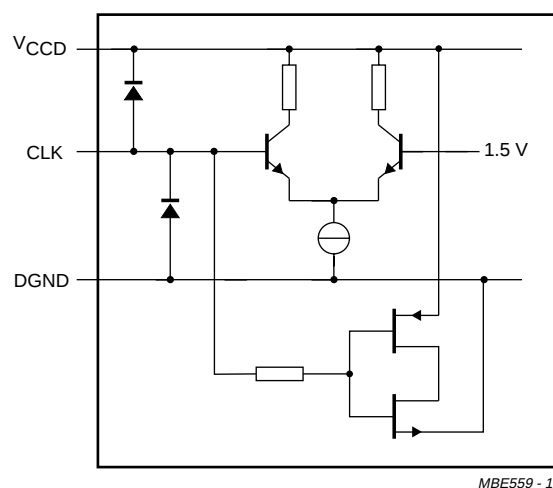
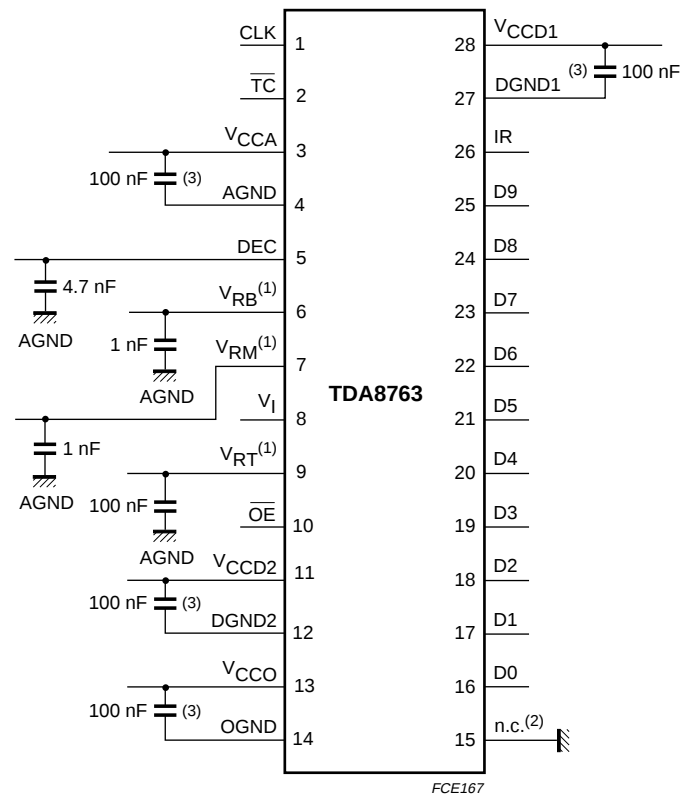
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Fig.13 CLK input.

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APPLICATION INFORMATION



The analog and digital supplies should be separated and well decoupled.

An application note is available and describes the design and the realization of a demonstration board that uses the version TDA8763M with an application environment.

- (1) V_{RB}, V_{RM} and V_{RT} are decoupled to AGND.
- (2) Pin 15 may be connected to DGND in order to prevent noise influence.
- (3) Decoupling capacitor for supplies: **must be placed close to the device.**

Fig.14 Application diagram.

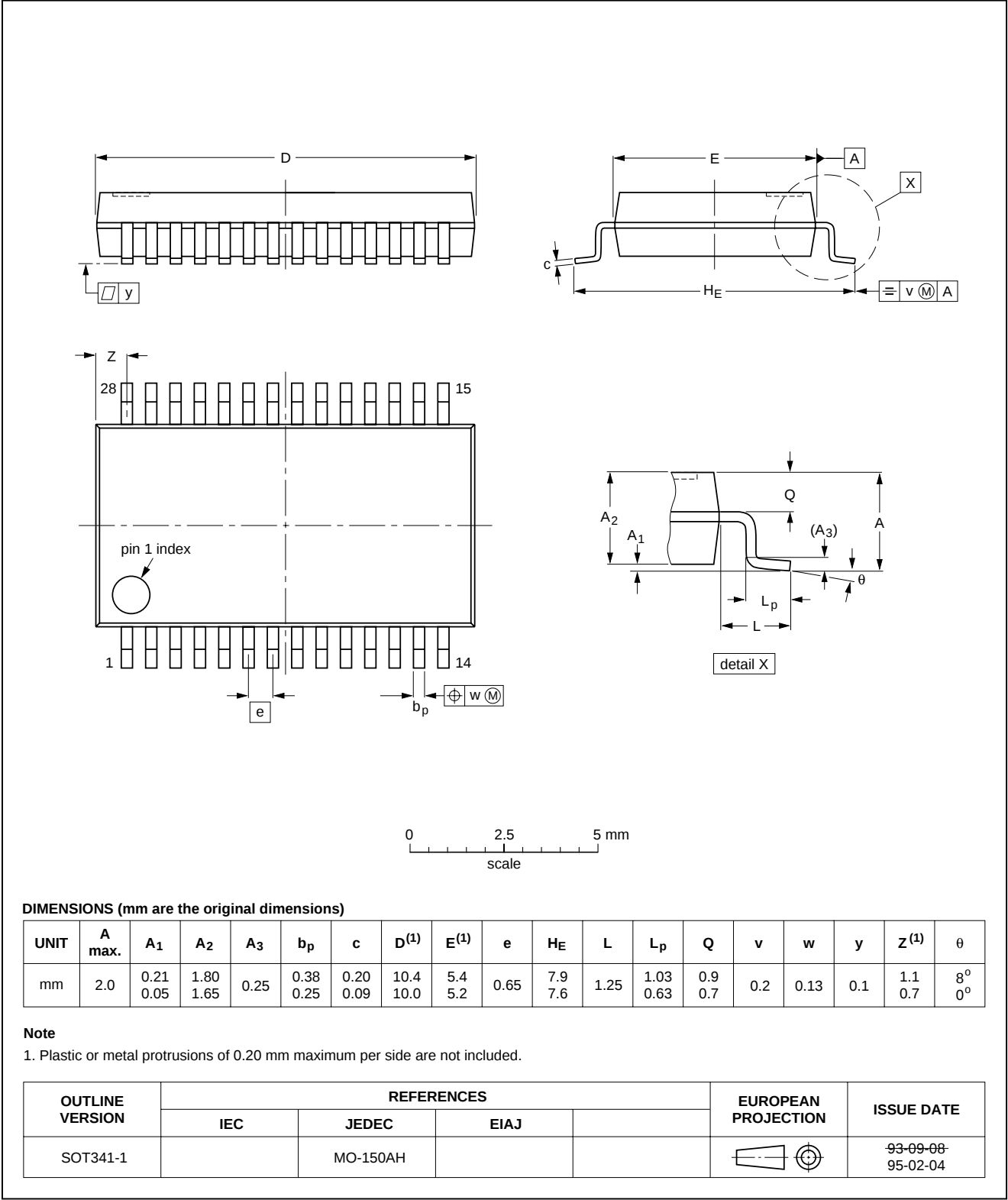
10-bit high-speed low-power ADC with
internal reference regulator

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PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm

SOT341-1



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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

545004/750/04/pp24

Date of release: 1999 Jan 06

Document order number: 9397 750 04692

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