

DATA SHEET

TDA8786; TDA8786A 10-bit analog-to-digital interface for CCD cameras

Product specification
Supersedes data of 1997 May 20
File under Integrated Circuits, IC02

1997 Nov 17

10-bit analog-to-digital interface for CCD cameras

TDA8786; TDA8786A

FEATURES

- Correlated Double Sampling (CDS), AGC, soft clipper, pre-blanking, 10-bit ADC and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- AGC gain from 3.5 to 33.5 dB (in 0.1 dB steps)
- Programmable soft clipper for white compression (starting at 40% of the input signal)
- Standby mode available for each block for power saving applications (19 mW)
- 6 dB fixed gain analog output for analog iris control
- 8-bit and 10-bit DAC included for analog settings
- Low power consumption of only 475 mW (typ.)
- 5 V operation and 2.5 to 5 V operation for the digital outputs
- CDS control pulse: TDA8786 = HIGH; TDA8786A = LOW
- TTL compatible inputs, TTL and CMOS compatible outputs.

GENERAL DESCRIPTION

The TDA8786; TDA8786A is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC, a soft clipper circuit and a low power 10-bit Analog-to-Digital Converter (ADC) together with its reference voltage regulator.

The AGC and soft clipper circuits are controlled by on-chip DACs via a serial interface.

A 10-bit DAC controls the ADC input clamp level.

A pre-blanking function is also included.

An additional DAC is provided for additional system controls; its output voltage range is 1.4 V (p-p) which is available at pin OFDOUT.

APPLICATIONS

- CCD camera systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{CCA}	analog supply voltage		4.5	4.75	5.5	V
V _{CCD}	digital supply voltage		4.5	4.75	5.5	V
V _{CCO}	digital outputs supply voltage		2.5	2.6	5.5	V
I _{CCA}	analog supply current		–	83	–	mA
I _{CCD}	digital supply current		–	16	–	mA
I _{CCO}	digital outputs supply current	f _{CLK} = 18 MHz; C _L = 20 pF; ramp input	–	1	–	mA
ADC _{res}	ADC resolution		–	10	–	bits
V _{i(CDS)(p-p)}	CDS input voltage (peak-to-peak value)		–	400	1200	mV
G _{CDS}	CDS output amplifier gain		–	6	–	dB
f _{CLK(max)}	maximum clock frequency		18	–	–	MHz
AGC _{dyn}	AGC dynamic range		–	30	–	dB
N _{tot(rms)}	total noise from CDS input to ADC output (RMS value)	gain = 3.5 dB	–	0.5	–	LSB
P _{tot}	total power consumption		–	475	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8786G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA8786AG			

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BLOCK DIAGRAM

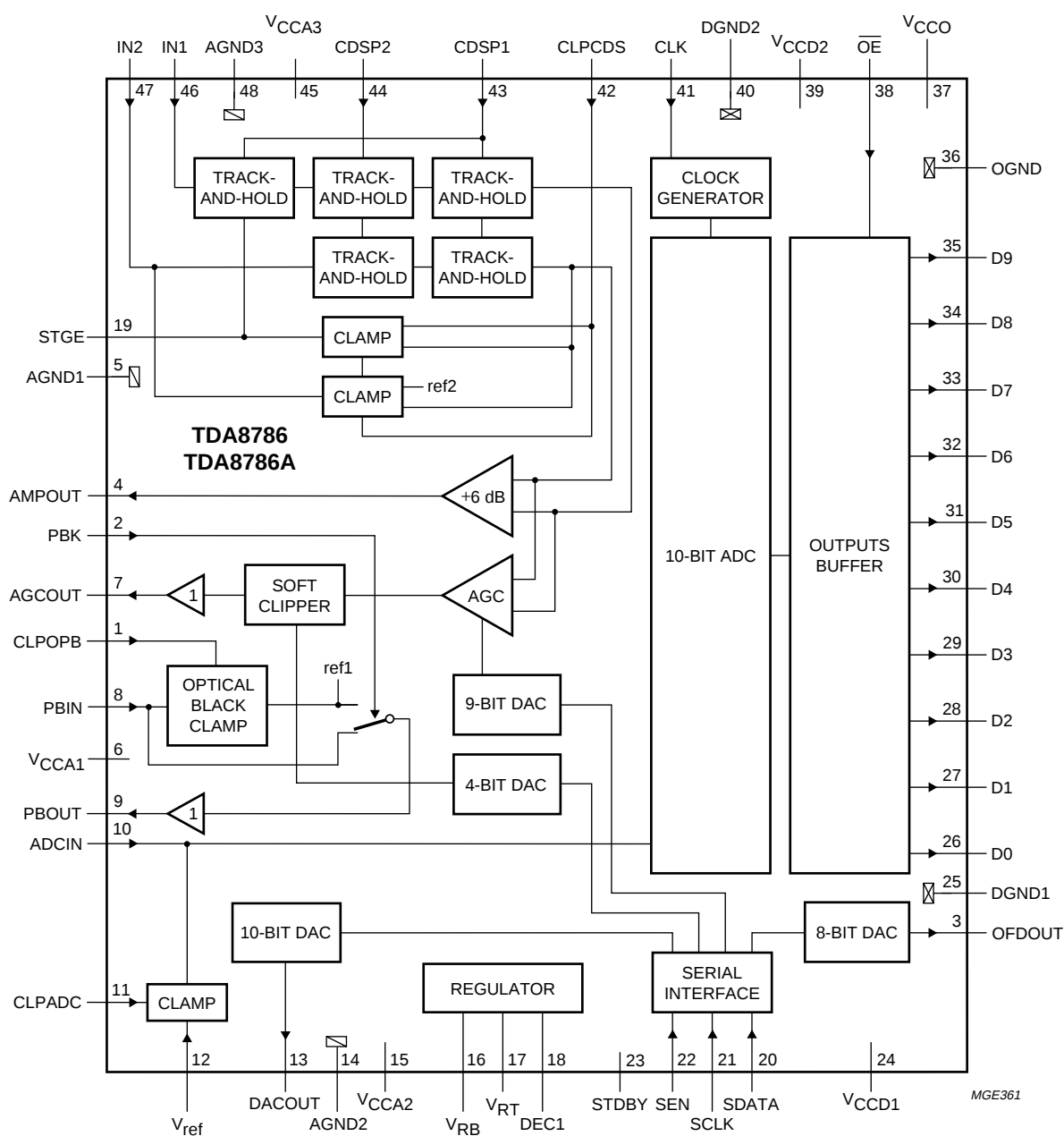


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
CLPOPB	1	optical black clamp control pulse input (active HIGH for TDA8786, active LOW for TDA8786A)
PBK	2	pre-blanking control pulse input; if PBK is HIGH (LOW) the signal is replaced by the optical black level for TDA8786 (TDA8786A)
OFDOUT	3	analog output of the additional 8-bit control DAC (controlled via the serial interface)
AMPOUT	4	CDS amplifier output (fixed gain = +6 dB)
AGND1	5	analog ground 1
V _{CCA1}	6	analog supply voltage 1
AGCOUT	7	AGC and soft clipper amplifier signal output
PBIN	8	optical black clamp and pre-blanking block signal input (from AGCOUT via a capacitor)
PBOUT	9	optical black clamp and pre-blanking block signal output
ADCIN	10	ADC analog signal input (from PBOUT or AGCOUT via a capacitor)
CLPADC	11	clamp control input for ADC analog input signal clamp (active HIGH for TDA8786 and active LOW for TDA8786A)
V _{ref}	12	ADC input clamp reference voltage (normally connected to pin VRB or DACOUT)
DACOUT	13	DAC output for ADC clamp level
AGND2	14	analog ground 2
V _{CCA2}	15	analog supply voltage 2
V _{RB}	16	ADC reference voltage (BOTTOM) code 0
V _{RT}	17	ADC reference voltage (TOP) code 1023
DEC1	18	decoupling 1 (decoupled to ground via a capacitor)
STGE	19	CDS offset storage
SDATA	20	serial data input for the 4 control DACs (9-bit DAC for AGC gain, 4-bit DAC for soft clipper; additional 8-bit DAC for OFD output voltage; 10-bit DAC for ADC clamp level and the stand-by mode per block; see Table 1)
SCLK	21	serial clock input for the control DACs and their serial interface; see Table 1
SEN	22	enable input for the serial interface shift register (active when SEN = logic 0); see Table 1
STDBY	23	stand-by control pin (active HIGH); all the output bits are logic 0 when stand-by is enabled
V _{CCD1}	24	digital supply voltage 1
DGND1	25	digital ground 1
D0	26	ADC digital output 0 (LSB)
D1	27	ADC digital output 1
D2	28	ADC digital output 2
D3	29	ADC digital output 3
D4	30	ADC digital output 4
D5	31	ADC digital output 5
D6	32	ADC digital output 6
D7	33	ADC digital output 7
D8	34	ADC digital output 8
D9	35	ADC digital output 9 (MSB)
OGND	36	digital output ground

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SYMBOL	PIN	DESCRIPTION
V _{CCO}	37	digital output supply voltage
OE	38	output enable (LOW: digital outputs active; HIGH: digital outputs high impedance)
V _{CCD2}	39	digital supply voltage 2
DGND2	40	digital ground 2
CLK	41	ADC clock input
CLPCDS	42	CDS clamp control input (active HIGH for TDA8786; active LOW for TDA8786A)
CDSP1	43	CDS control pulse input 1 (active HIGH for TDA8786; active LOW for TDA8786A)
CDSP2	44	CDS control pulse input 2 (active HIGH for TDA8786; active LOW for TDA8786A)
V _{CCA3}	45	analog supply voltage 3
IN1	46	input signal 1 from CCD (usually black channel)
IN2	47	input signal 2 from CCD (usually video channel)
AGND3	48	analog ground 3

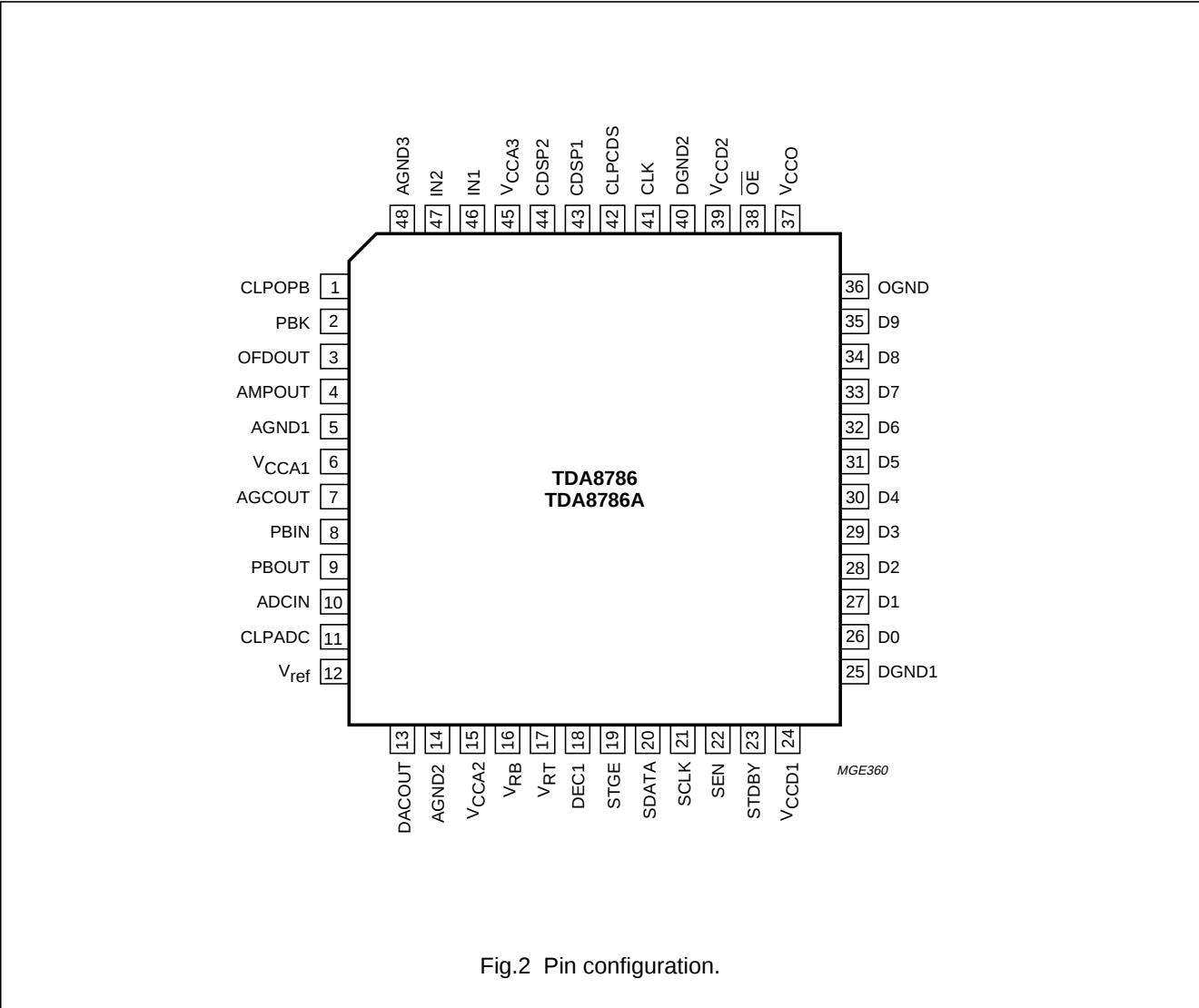


Fig.2 Pin configuration.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	-0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	-0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	-0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD} between V_{CCA} and V_{CCO} between V_{CCD} and V_{CCO}		-1.0 -1.0 -1.0	+1.0 +4.0 +4.0	V V V
V_i	input voltage	referenced to V_{SSA}	-0.3	+7.0	V
$V_{CLK(p-p)}$	AC input voltage for switching (peak-to peak-value)	referenced to V_{SSD}	–	V_{CCD}	V
I_o	output current		–	10	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		-20	+75	°C
T_j	junction temperature		–	150	°C

Note

- The supply voltages V_{CCA} , V_{CCD} and V_{CCO} may have any value between -0.3 and +7.0 V provided that the supply voltage difference ΔV_{CC} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	76	K/W

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CHARACTERISTICS

$V_{CCA} = V_{CCD} = 4.75\text{ V}$; $V_{CCO} = 2.6\text{ V}$; $f_{CLK} = 18\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	4.75	5.5	V
V_{CCD}	digital supply voltage		4.5	4.75	5.5	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	5.5	V
I_{CCA}	analog supply current		–	83	–	mA
I_{CCD}	digital supply current		–	16	–	mA
I_{CCO}	digital outputs supply current	$C_L = 20\text{ pF}$ on all data outputs; ramp input	–	1	–	mA
Digital inputs						
CLOCK INPUT: CLK (REFERENCED TO DGND)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{CLK} = 0.8\text{ V}$	–1	–	+1	μA
I_{IH}	HIGH-level input current	$V_{CLK} = 2.0\text{ V}$	–	–	20	μA
Z_i	input impedance	$f_{CLK} = 18\text{ MHz}$	–	2	–	$\text{k}\Omega$
C_i	input capacitance	$f_{CLK} = 18\text{ MHz}$	–	2	–	pF
INPUTS: CDSP1 AND CDSP2						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.2	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.6\text{ V}$	–	–100	–	μA
I_{IH}	HIGH-level input current	$V_{IH} = 2.2\text{ V}$	–	0	–	μA
INPUTS: SEN, STDBY, CLPCDS, CLPOPB, PBK AND CLPADC						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.2	–	V_{CCD}	V
I_i	input current		–2	–	+2	μA
INPUTS: SEN, SDATA AND SCLK (see Fig.14)						
t_{su1}	SEN set-up time compared to SCLK rising edge		–	4	–	ns
t_{su2}	SDATA set-up time compared to SCLK rising edge		–	4	–	ns
t_{su3}	SEN set-up time compared to SCLK falling edge		–	4	–	ns
t_{hd3}	SEN hold time compared to SCLK rising edge		–	4	–	ns
t_{hd4}	SDATA hold time compared to SCLK rising edge		–	4	–	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Correlated Double Sampling; CDS						
$V_{i(CDS)(p-p)}$	CDS input amplitude (peak-to-peak value)		–	400	1200	mV
$I_{STGE,IN1,IN2}$	input current pins 19, 46 and 47		–2	–	+2	μA
$t_{CDS(min)}$	CDS control pulses minimum active time (HIGH for TDA8786, LOW for TDA8786A)	$f_{i(CDS1,2)} = f_{CLK(pix)}$ $V_{i(CDS)(p-p)} = 1200$ mV black-to-white transition in one pixel (± 1 LSB typ.)	12	–	–	ns
t_{hd1}	hold time IN1 compared to control pulse CDSP1	see Fig.15	–	1	–	ns
t_{hd2}	hold time of IN2 compared to control pulse CDSP2	see Fig.15	–	–0.5	–	ns
Amplifier outputs						
G_{AMPOUT}	output amplifier gain		–	6	–	dB
Z_{AMPOUT}	output amplifier impedance		–	300	–	Ω
$V_{AMPOUT(p-p)}$	output amplifier dynamic voltage level (peak-to-peak value)		–	2.4	–	V
$V_{AMPOUT(bl)}$	output amplifier black level voltage		–	1.1	–	V
$V_{AGCOUT(p-p)}$	AGC output amplifier dynamic voltage level (peak-to-peak value)		–	1800	–	mV
V_{AGCOUT}	AGC output amplifier black level voltage		–	1.1	–	V
Z_{AGCOUT}	AGC output amplifier output impedance	at 10 kHz	–	5	–	Ω
I_{AGCOUT}	AGC output static drive current	static	–	–	1	mA
$V_{OPB(p-p)}$	optical black clamp and blanking block output dynamic voltage (peak-to-peak value)		–	1.8	–	V
V_{OPB}	optical black clamp and blanking block output black level voltage		–	1.4	–	V
Z_{OPB}	optical black clamp and blanking block output impedance	at 10 kHz	–	–	5	Ω
I_{OPB}	OPB output current drive	static	–	–	1	mA
I_{PBIN}	input current pin 8		–2	–	+2	μA
$G_{AGC(min)}$	minimum gain of AGC circuit	AGC DAC input code = 00 (9-bit control)	–	3.5	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G _{AGC(max)}	maximum gain of AGC circuit	AGC DAC input code = ≥319 (9-bit control)	–	33.5	–	dB
V _{AGCOUT}	AGC output amplifier black level voltage		–	1.1	–	V
V _{inflex(p-p)}	voltage at soft clipper inflexion point (peak-to-peak value)	soft clipper 4-bit control DAC input code = 00	–	40% V _{AGCOUT(p-p)}	–	V
		soft clipper 4-bit control DAC input code = 15	–	100% V _{AGCOUT(p-p)}	–	V
CR _{sc}	soft clipper compression ratio	V _{i(sc)} < V _{inflex}	–	1.0	–	
		V _{i(sc)} > V _{inflex}	–	0.66	–	
CLAMPS						
g _{mADC}	ADC clamps transconductance	at clamp level	–	60	–	mS
g _{mPBK}	PBK clamp transconductance	at clamp level	–	60	–	mS
g _{mCDS}	CDS clamps transconductance	at clamp level	–	5.5	–	mS
V _{PBIN(clamp)}	clamp voltage at PBIN input		–	1.4	–	V
Analog-to-Digital Converter; ADC						
f _{CLK(max)}	maximum clock frequency		18	–	–	MHz
t _{CPH}	clock pulse width HIGH		15	–	–	ns
t _{CPL}	clock pulse width LOW		15	–	–	ns
SR _{CLK}	clock input slew rate (rising and falling edge)	10 to 90%	0.5	–	–	V/ns
V _{i(ADC)(p-p)}	ADC input voltage level (peak-to-peak value)		–	1.8	–	V
V _{RB}	ADC reference voltage output code 0		–	1.4	–	V
V _{RT}	ADC reference voltage output code 1023		–	3.2	–	V
I _{ADCIN}	input current pin 10		–2	–	+2	μA
ILE	integral linearity error	f _{CLK} = 18 MHz; ramp input	–	±1.0	±2.0	LSB
DLE	differential linearity error	f _{CLK} = 18 MHz; ramp input	–	±0.4	±0.75	LSB
t _{d(s)}	sampling delay time		–	–	5	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Total chain timing (CDS + ADC + SOFT CLIPPER + PRE BLANKING + ADC)						
t_d	time delay between CDSP1 and CLK	50% at rising edges of CLK and CDSP1: transition full-scale code 0 to code 1023; $V_{i(CDS)(p-p)} = 1200 \text{ mV}$	–	40	–	ns
$N_{(rms)}$	noise (RMS value)	gain = 3.5 dB	–	0.5	–	LSB
Digital-to-Analog Converters (OFDOUT DAC)						
$V_{OFDOUT(p-p)}$	additional 8-bit control DAC (OFD) output voltage (peak-to-peak value)		–	1.4	–	V
$V_{OFDOUT(0)}$	DC output voltage for code 0		–	2.0	–	V
$V_{OFDOUT(255)}$	DC output voltage for code 255		–	3.4	–	V
Z_{OFDOUT}	additional 8-bit control DAC (OFD) output impedance		–	2000	–	Ω
I_{OFDOUT}	OFD output current drive	static	–	–	50	μA
ADC clamp control DAC (see Fig.5)						
$V_{DACOUT(p-p)}$	ADC clamp 10-bit control DAC output voltage (peak-to-peak value)		–	0.9	–	V
V_{DACOUT}	DC output voltage	code 0	–	1.4	–	V
		code 1023	–	2.3	–	V
Z_{DACOUT}	ADC clamp control DAC output impedance		–	–	250	Ω
I_{DACOUT}	DAC output current drive	static	–	–	50	μA
OFE_{LOOP}	maximum offset error of DAC + ADC clamp loop	code 0	–	± 5	–	LSB
		code 1023	–	± 5	–	LSB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs (f _{CLK} = 18 MHz; C _L = 20 pF)						
V _{OH}	HIGH-level output voltage	I _{OH} = −1 mA	V _{CCO} − 0.5	−	V _{CCO}	V
V _{OL}	LOW-level output voltage	I _{OL} = 1 mA	0	−	0.5	V
I _{OZ}	output current in 3-state mode	0.5 V < V _o < V _{CCO}	−20	−	+20	μA
t _{o(h)}	output hold time		5	−	−	ns
t _{o(d)}	output delay	C _i = 20 pF; V _{CCO} = 4.75 V	−	12	15	ns
		C _i = 20 pF; V _{CCO} = 3.15 V	−	17	20	ns
		C _i = 20 pF; V _{CCO} = 2.7 V	−	21	24	ns
Serial interface						
f _{SCLK(max)}	maximum frequency of serial interface		5	−	−	MHz

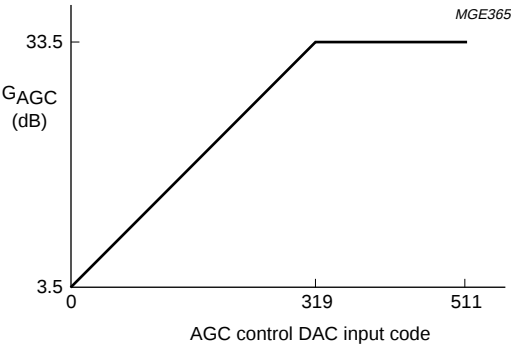
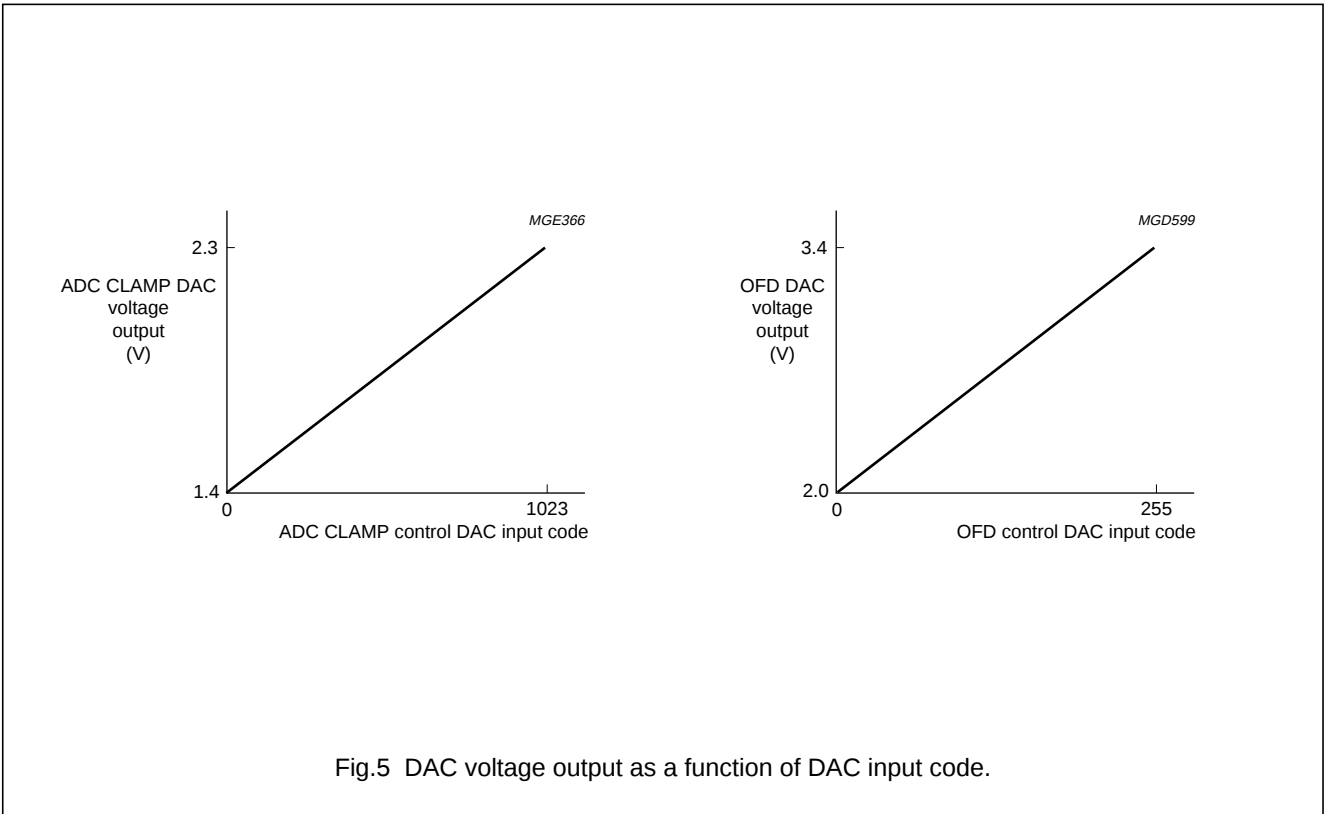
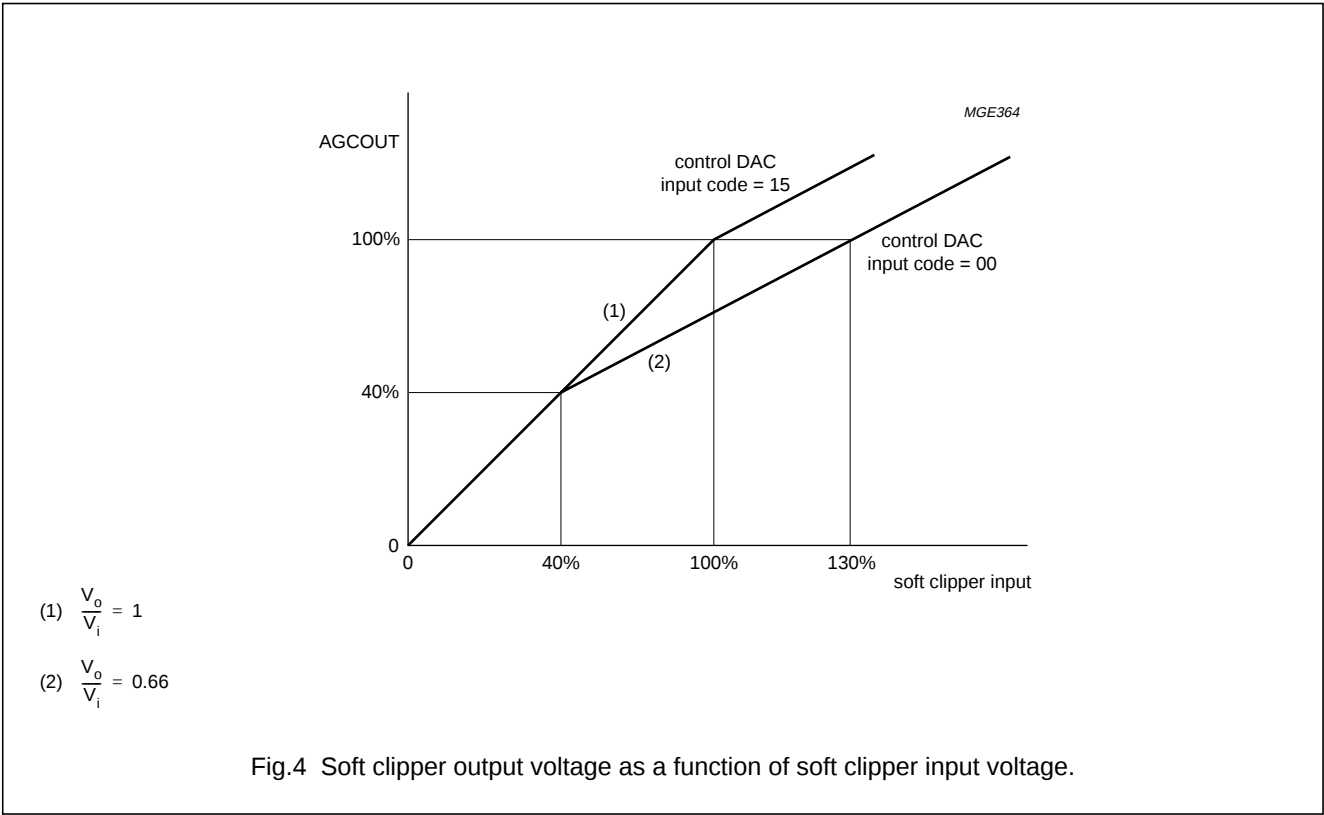


Fig.3 AGC gain as a function of DAC input code.

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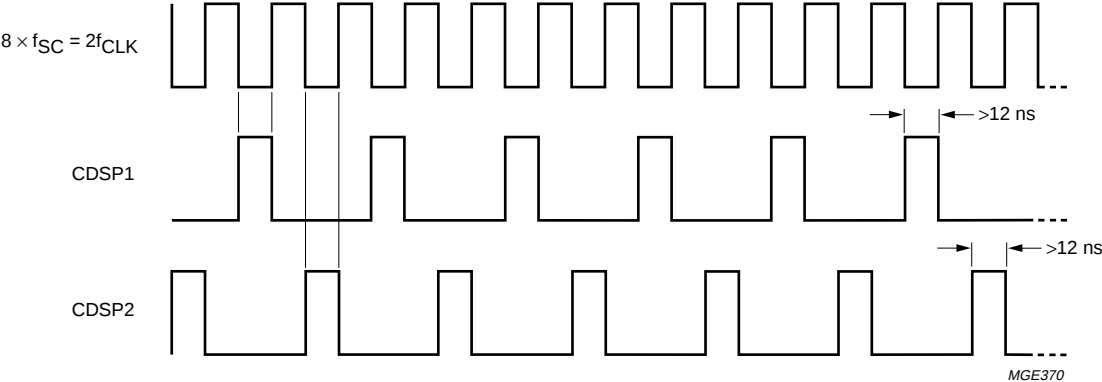


Fig.6 CCD high band control signal timing (TDA8786).

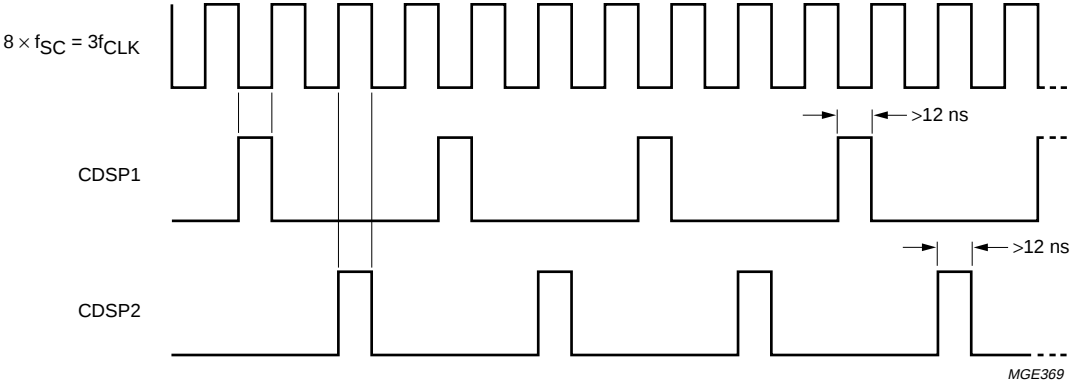


Fig.7 CCD normal band control signal timing (TDA8786).

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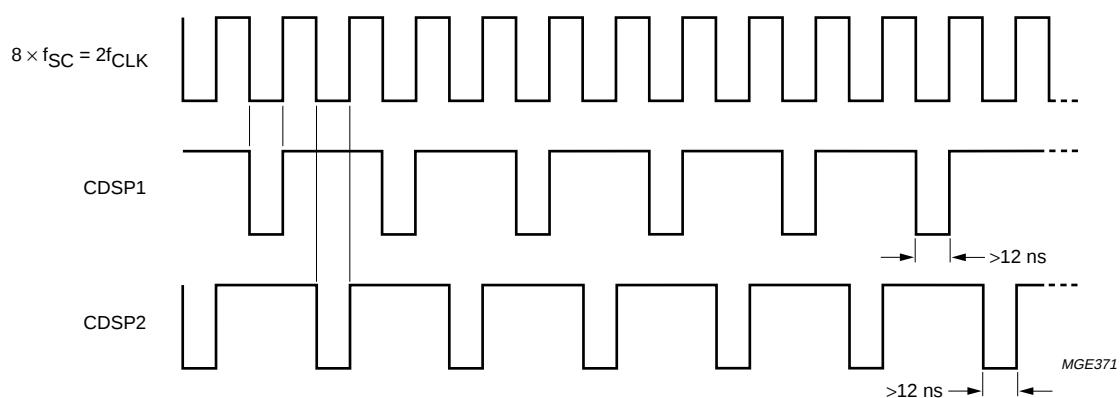


Fig.8 CCD high band control signal timing (TDA8786A).

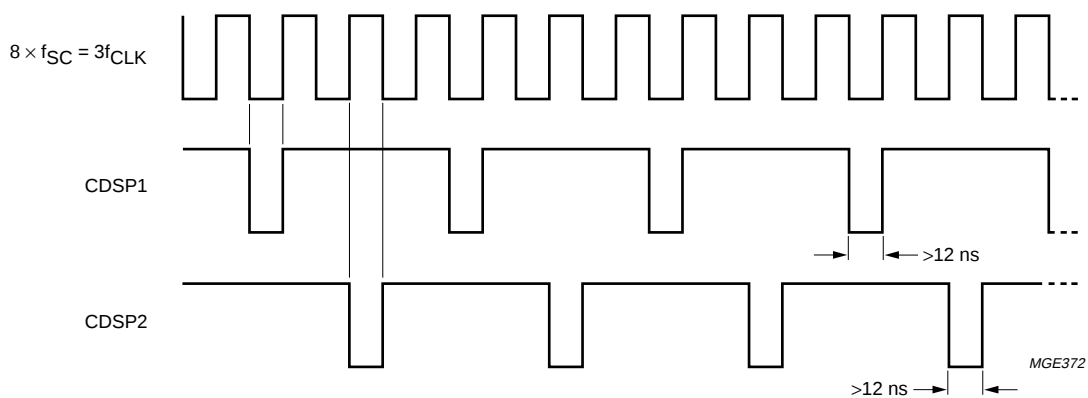
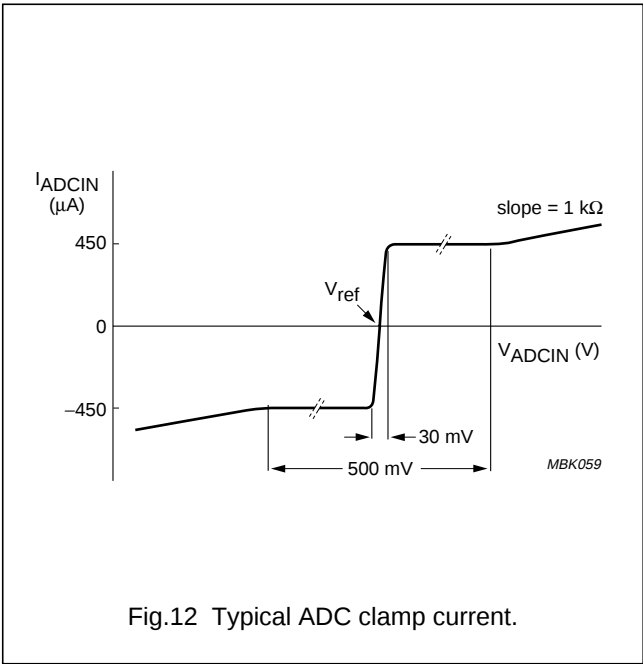
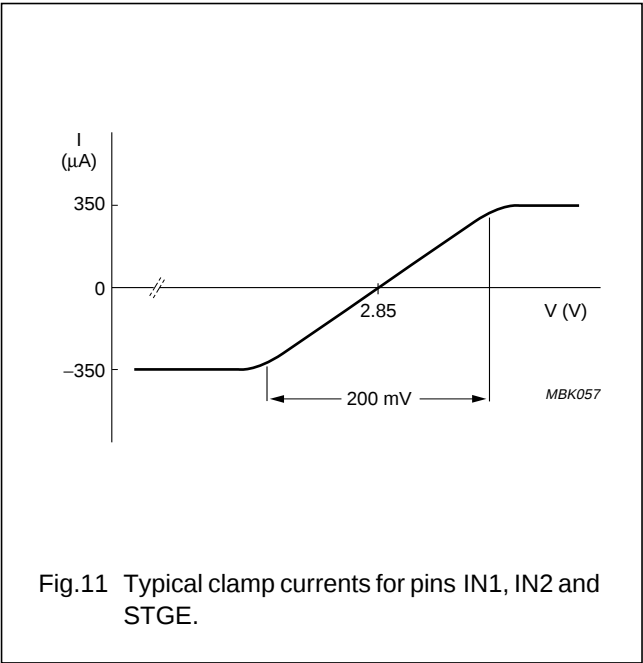
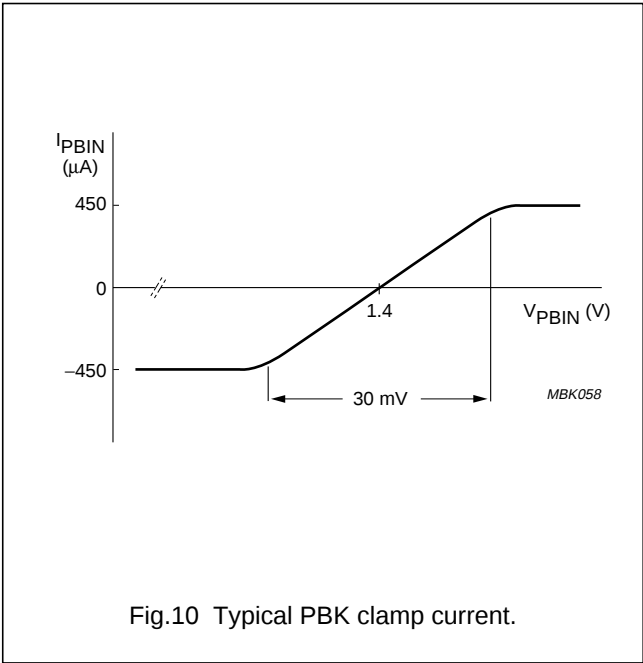


Fig.9 CCD normal band control signal timing (TDA8786A).

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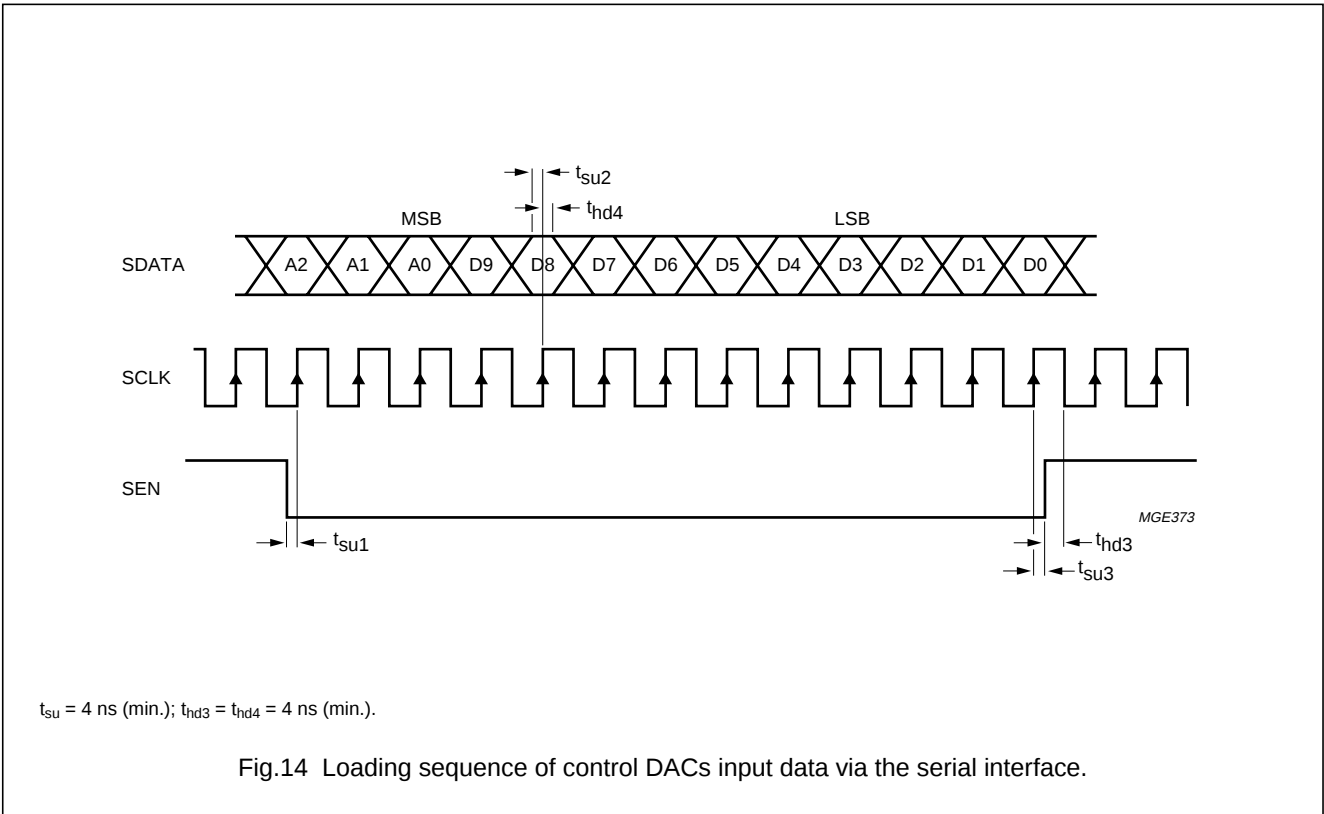
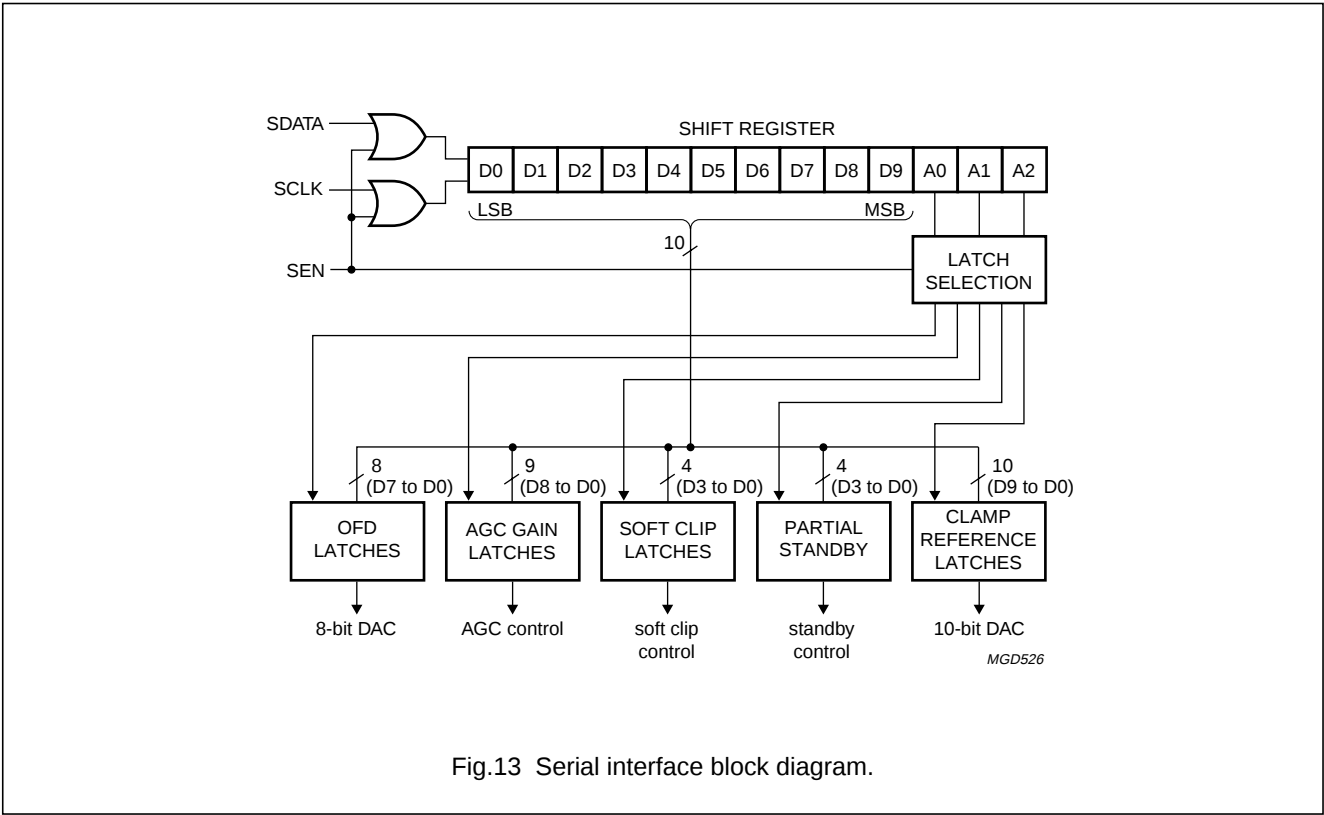


ADC clamping

When pin CLPADC is HIGH (TDA8786) (LOW for TDA8786A), the ADC input is clamped to voltage level V_{ref} . V_{ref} should normally be connected to V_{RB} (ADC reference voltage code 0) or to DACOUT (10-bit DAC output). The DAC is controlled via the serial interface, its output covers the lower half of the ADC input range.

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Table 1 Serial interface programming (see note 1)

ADDRESS BITS			DATA BITS D9 to D0
A2	A1	A0	
0	0	0	OFDOUT output control (D7 to D0).
0	0	1	Soft clipper control. Only the 4 LSBs (D3 to D0) are used. Bits D9 to D4 should be set to logic 0.
0	1	0	AGC gain control (D8 to D0).
0	1	1	Partial standby controls for power consumption optimization. Only the 4 LSBs (D3 to D0) are used. Bits D9 to D4 should be set to logic 0: D0 = 1: CDS + AGC + soft clipper block in standby; $I_{CCA} + I_{CCD} = 48$ mA D1 = 1: optical black clamp + blanking block in standby; $I_{CCA} + I_{CCD} = 92$ mA D2 = 1: OFD DAC in standby; $I_{CCA} + I_{CCD} = 98$ mA D3 = 1: 6 dB amplifier (output on AMPOUT pin) in standby; $I_{CCA} + I_{CCD} = 98.5$ mA.
1	0	0	Clamp reference DAC (D9 to D0).

Note

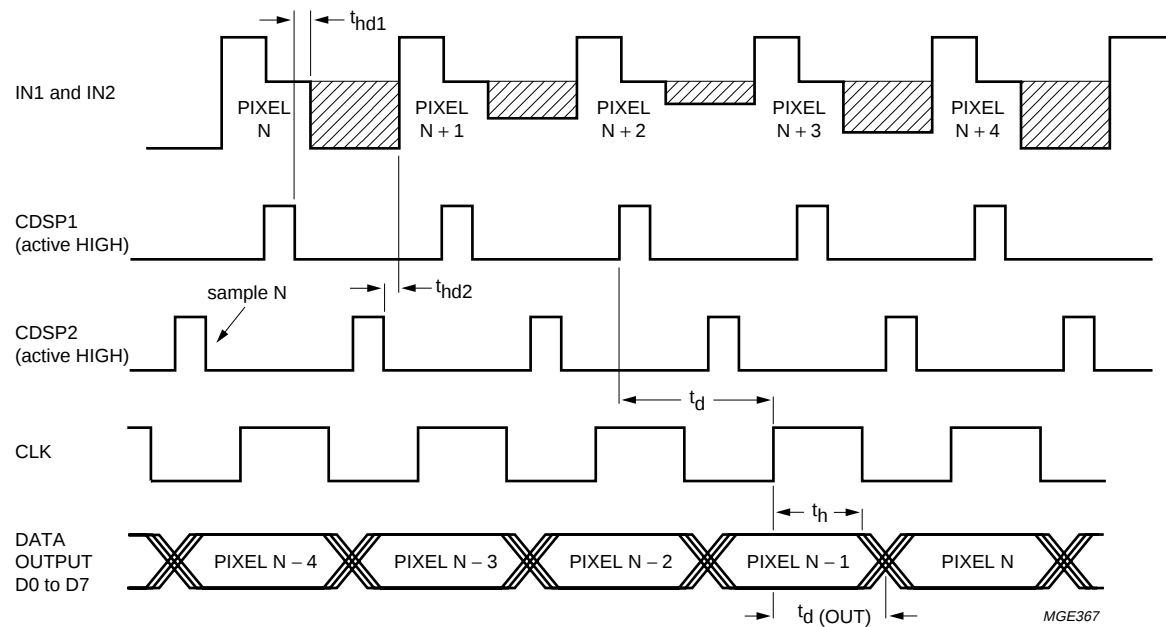
- At the end of each programming sequence (usually during the video vertical blanking), the soft clipper register must be reloaded (for example if the soft clipper is not used, code 15 must be entered in the soft clipper register at the end of each TDA8786(A) programming sequence).

Table 2 Standby selection

STDBY	D9 to D0	$I_{CCA} + I_{CCD}$
1	LOW	4 mA (typ.)
0	active	99 mA (typ.)

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The hatched areas represent active video.

Fig.15 Pixel frequency timing diagram.

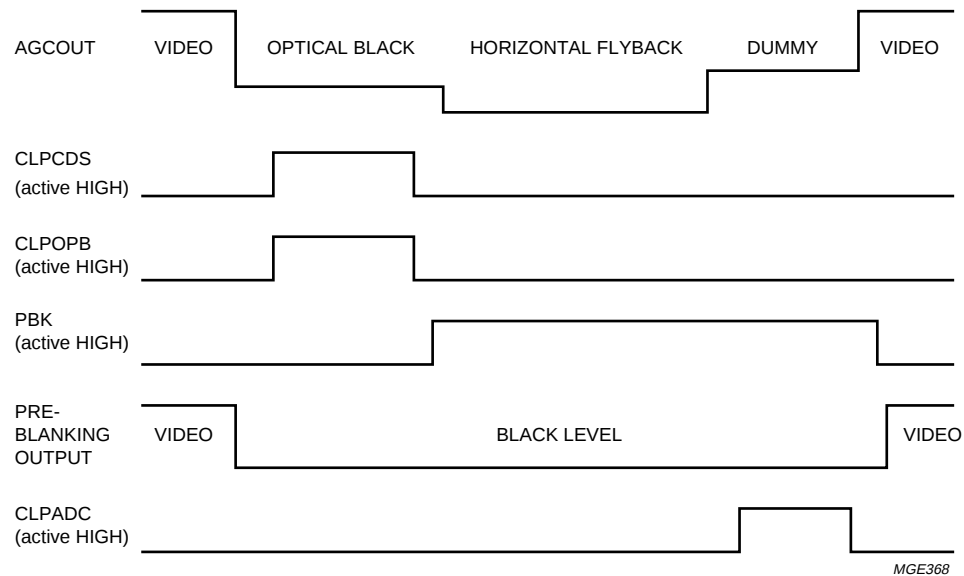


Fig.16 Line frequency timing diagram.

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APPLICATION INFORMATION

TDA8786 and SAA8110 can be used with Sharp CCDs. TDA8786A and SAA8110 can be used with Sony CCDs. Table 3 gives as an example some references of ICs which may be used with Philips TDA8786(A)/SAA8110. This overview is not restrictive, both devices are compatible with other CCD/V-driver/PPG combinations including the more recent ones.

Table 3 Possible components for the application of Figs 17 and 18

CCD TYPE	COMPONENT TYPE	NTSC		PAL	
		MEDIUM RESOLUTION	HIGH RESOLUTION	MEDIUM RESOLUTION	HIGH RESOLUTION
Sony CCDs	CCD	LZ2313H5	LZ2353A	LZ2323H5	LZ2363
	V-driver	LR36683N			
	timing generator	LZ95G55	LZ95G71	LZ95G55	LZ95G71
Sharp CCDs	CCD	ICX056AK	ICX068AK	ICX057AK	ICX069AK
	V-driver	CXD1250MN, CXD1267N			
	timing generator	CXD1257AR	CXD1265R	CXD1257AR	CXD1265R

Notes to the application diagram

1. In the configuration of Figs 17 and 18, the microcontroller reads and writes data from/to the DSP using the SNERT-bus (UART mode 0). Optional external control is available via the I²C-bus.
2. Free I/O pins of the microcontroller can be used to control PGG, or for other purposes.
3. 83Cxxx processing is synchronized by VD interruption. Depending on VD polarity, it can be necessary to invert VD.
4. A customized 83Cxxx is available for this application. Please contact your nearest Philips sales office.

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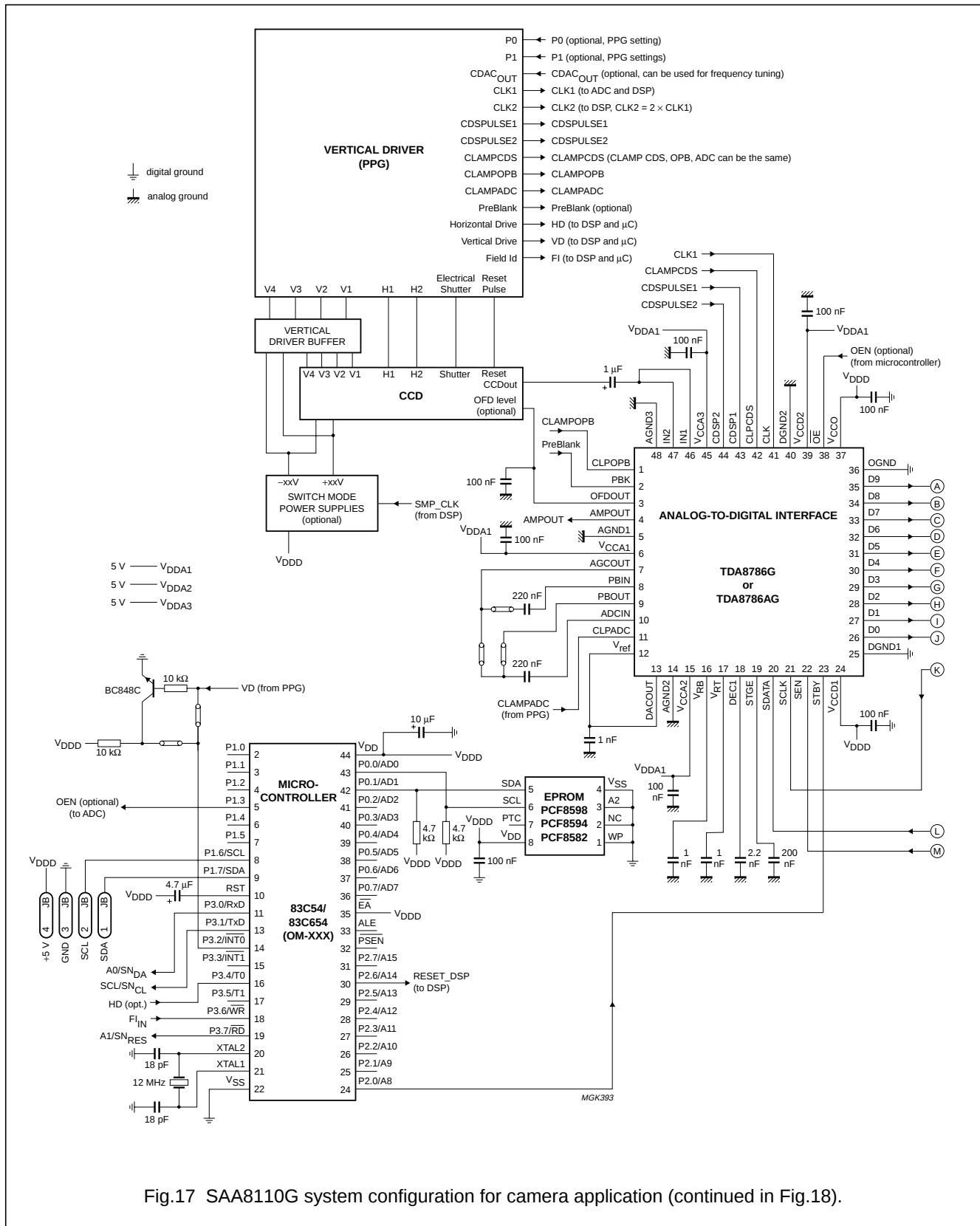
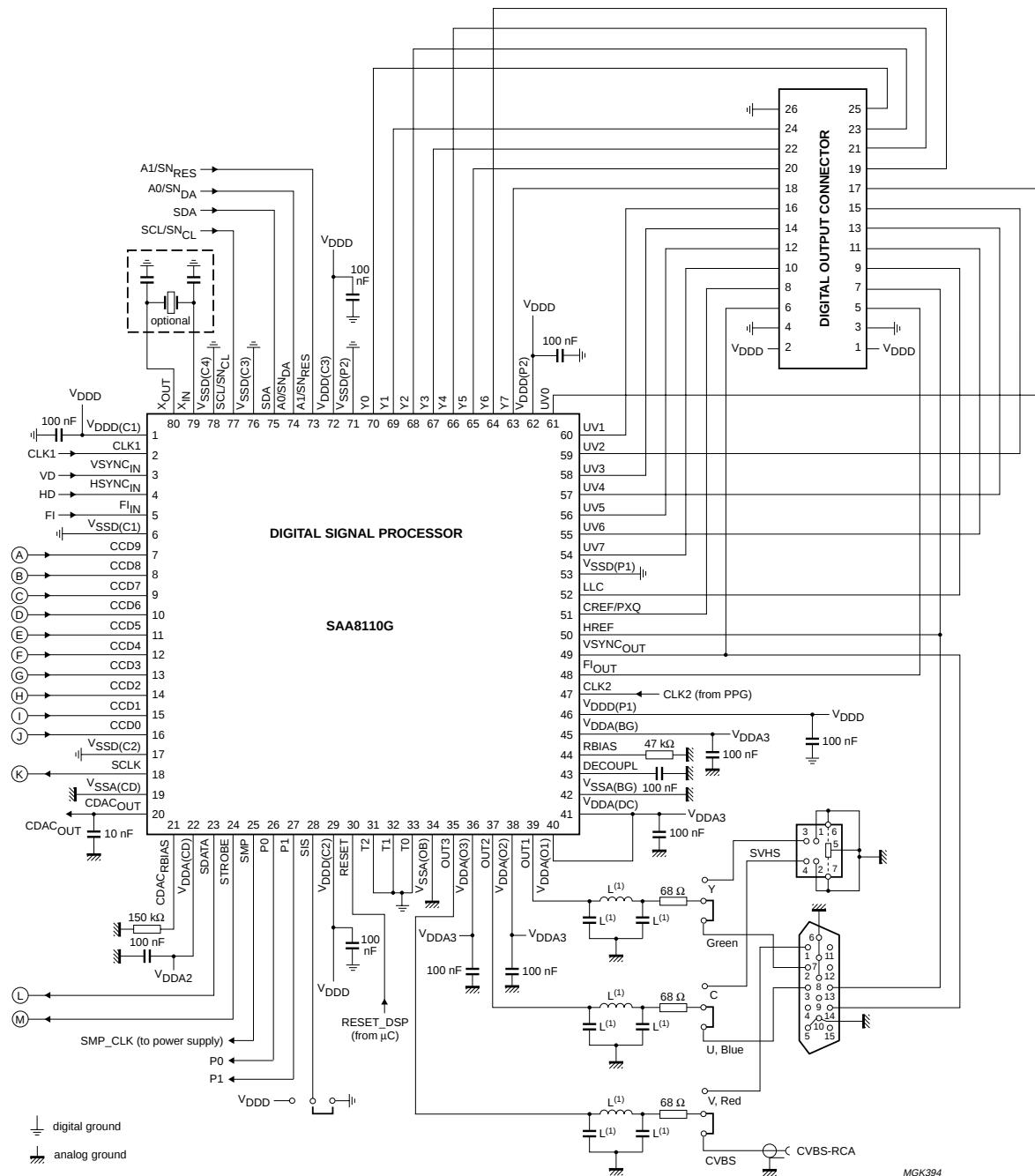


Fig.17 SAA8110G system configuration for camera application (continued in Fig.18).

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(1) Values depend on DSP output configuration.

Fig.18 SAA8110G system configuration for camera application (continued from Fig.17).

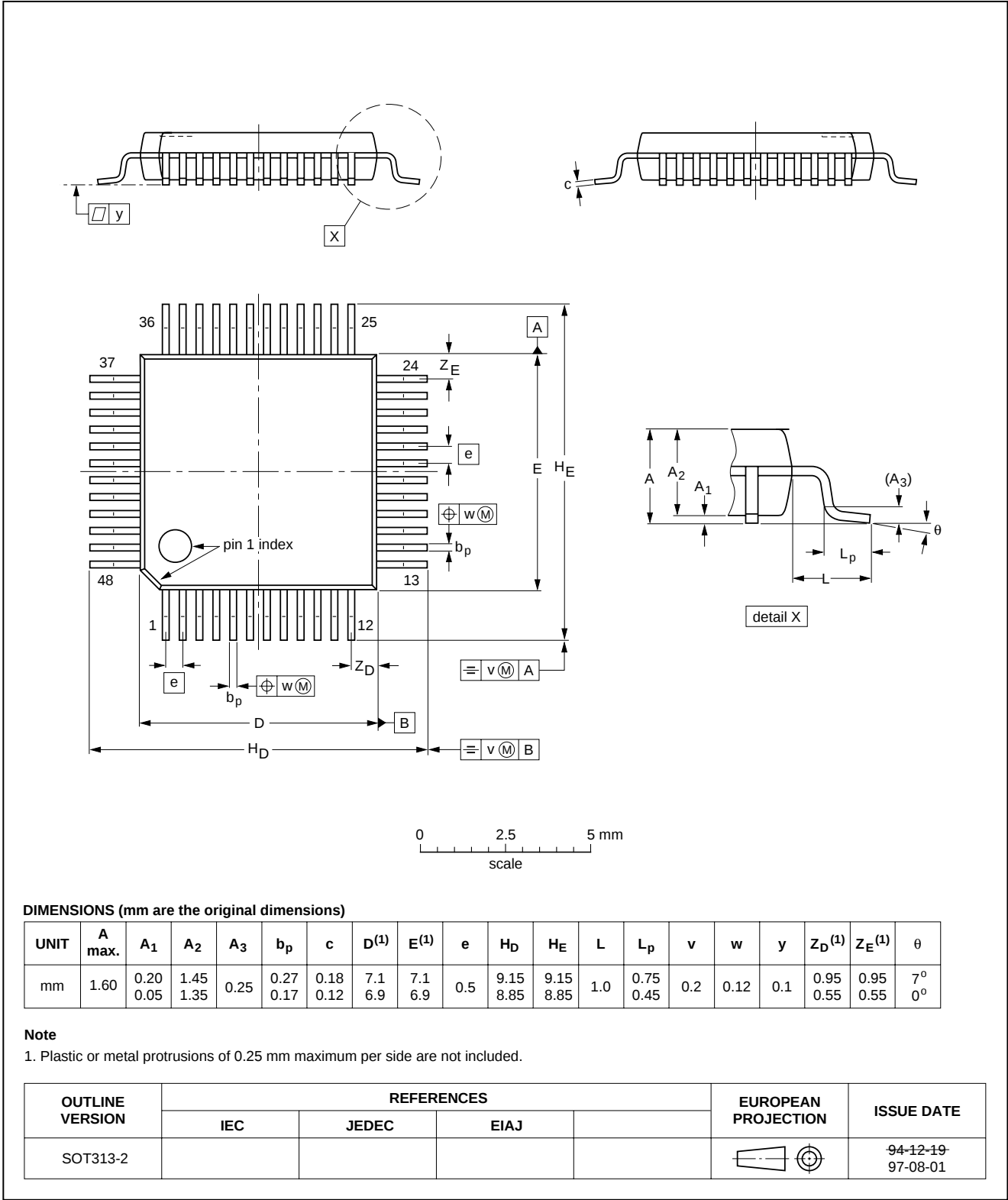
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PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2



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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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NOTES

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Printed in The Netherlands

547047/1200/03/pp28

Date of release: 1997 Nov 17

Document order number: 9397 750 02926

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