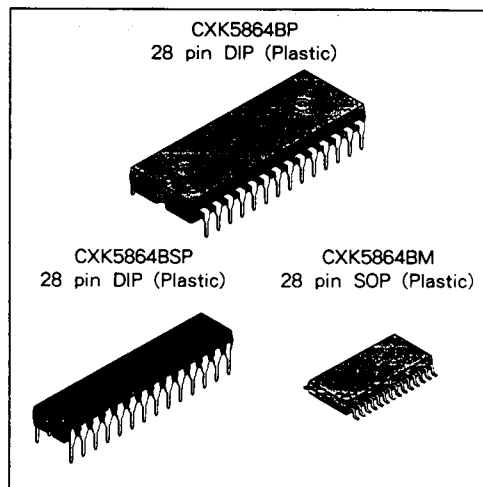


SONY**CXK5864BP/BSP/BM** -70L/10L/12L/
-70LL/10LL/12LL**8,192-word × 8-bit High Speed CMOS Static RAM** *Maintenance Only***Description**

CXK5864BP/BSP/BM are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8 bits and operates from a single 5V supply. These IC are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

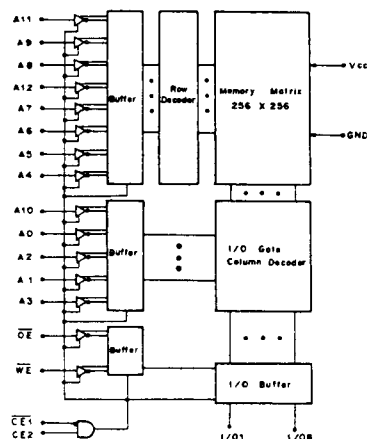
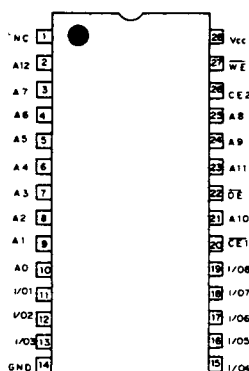
- Fast access time (Access time)
CXK5864BP/BSP/BM-70L, 70LL 70ns(Max.)
CXK5864BP/BSP/BM-10L, 10LL 100ns(Max.)
CXK5864BP/BSP/BM-12L, 12LL 120ns(Max.)
- Low power operation :
CXK5864BP/BSP/BM-70LL, 10LL, 12LL ;
Standby/Operation : 5 μ W (Typ.)/40mW (Typ.)
CXK5864BP/BSP/BM-70L, 10L, 12L ;
Standby/Operation : 10 μ W (Typ.)/40mW (Typ.)
- Single power supply 5V : +5V $\pm$ 10 %
- Fully static memory ... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs
- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

**Function**

8,192-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram**Pin Configuration**
(Top View)**Pin Description**

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK5864BP/BSP	1.0
		CXK5864BM	0.7
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics**• DC and operating characteristics**(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70°C)

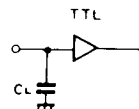
Item	Symbol	Test conditions	- 70L/10L/12L - 70LL/10LL/12LL			Unit
			Min.	Typ.*	Max.	
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	- 500	—	500	nA
Output leak current	I _{LO}	V _{I/O} = GND to V _{CC} CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	- 500	—	500	nA
Operating supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	8	15	mA
Average operating current	I _{CC2}	Min. cycle Duty = 100 %, I _{OUT} = 0mA	—	30	50	mA
Standby current	I _{SB1}	CE2 ≤ 0.2V or { CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	- L	—	2	60
			- LL	—	1	30
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL}	—	0.1	2	mA
Output high voltage	V _{OH}	I _{OH} = - 1.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C**Pin capacitance**(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.**AC characteristics****• AC test conditions** (V_{CC} = 5V ± 10 %, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 2.2V
Input pulse low level	V _{IL} = 0.8V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	10L/10LL/12L/12LL C _L * = 100pF, 1TTL
	70L/70LL C _L * = 30pF, 1TTL

* C_L includes scope and jig capacitances.

●Read cycle

Item	Symbol	- 70L/70LL		- 10L/10LL		- 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	100	—	120	ns
Chip enable access time ($\overline{\text{CE1}}$, CE2)	t _{CO1} t _{CO2}	—	70	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	50	—	60	ns
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} * t _{HZ2} *	0	30	0	35	0	45	ns
Output disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	30	0	35	0	45	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

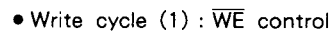
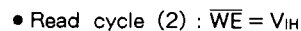
●Write cycle

Item	Symbol	- 70L/70LL		- 10L/10LL		- 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	60	—	80	—	85	—	ns
Chip enable to end of write	t _{CW}	60	—	80	—	85	—	ns
Data to write time overlap	t _{DW}	30	—	35	—	50	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	40	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	30	0	35	0	45	ns

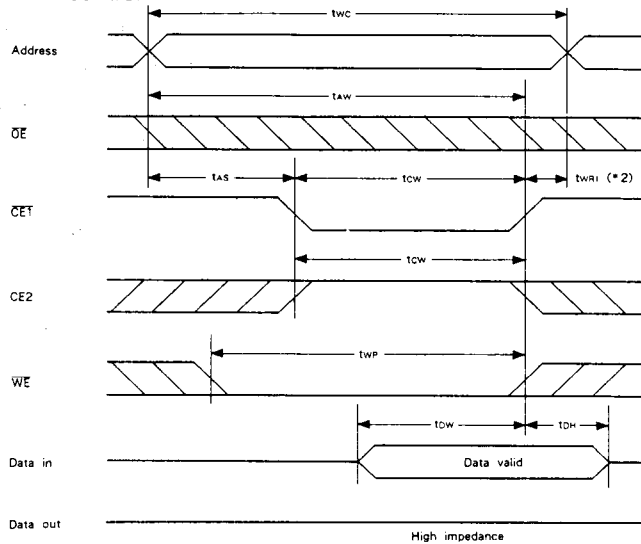
* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$

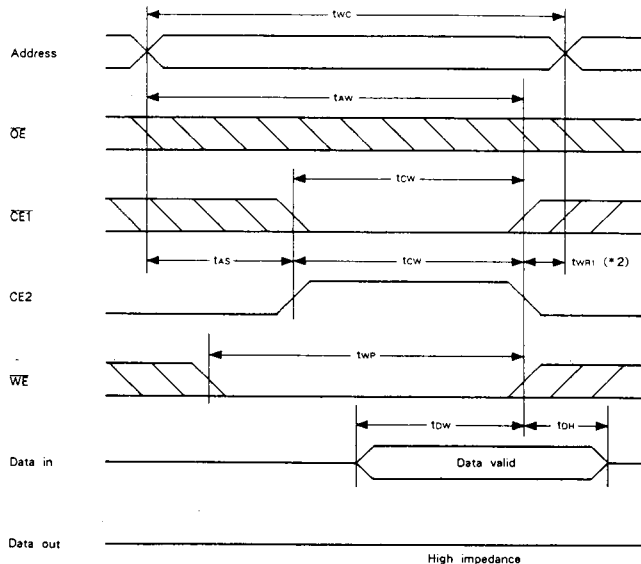
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note)

- *1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
- *2. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.
- *3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

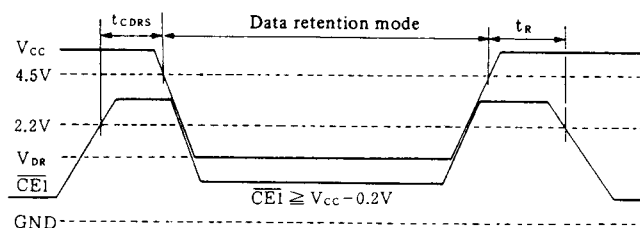
Data Retention Characteristics

(Ta = 0 to +70°C)

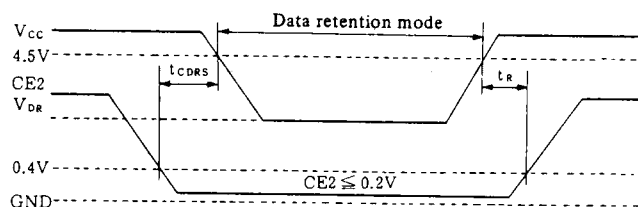
Item	Symbol	Test conditions		- 70L/10L/12L			- 70LL/10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	*1	Ta = 0°C to 70°C	—	1	35	—	0.5	15	μA
		V _{CC} = 3.0V	Ta = 0°C to 40°C	—	—	—	—	—	3	
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V, *1		—	2	60	—	1	30	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	t _{RC} *2	—	—	ns

* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ [$\overline{CE1}$ Control] or $CE2 \leq 0.2V$ [$CE2$ Control]* 2. t_{RC}: Read cycle time

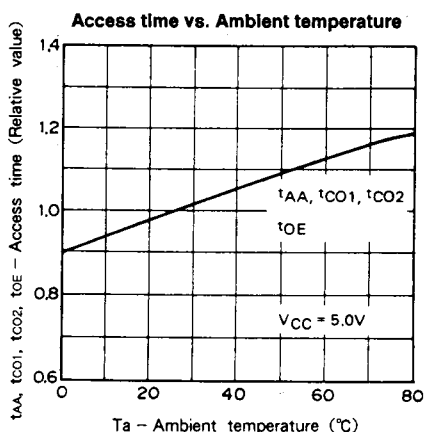
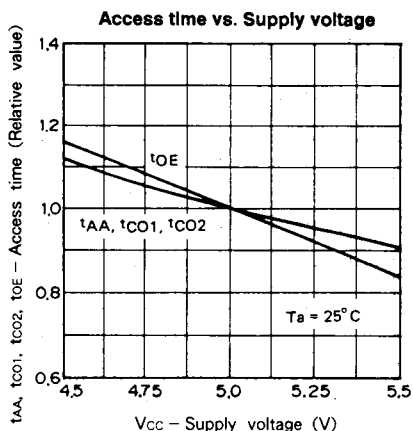
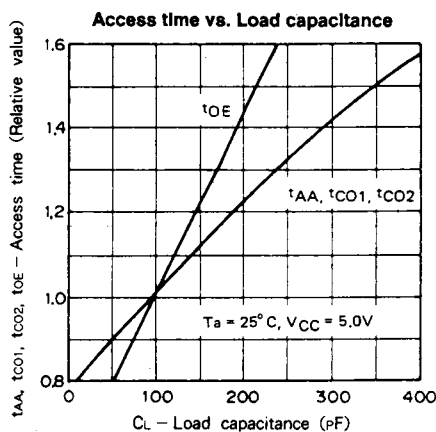
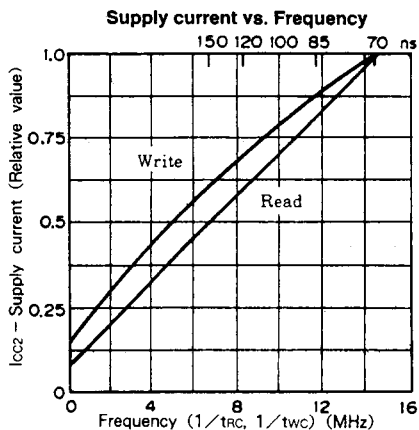
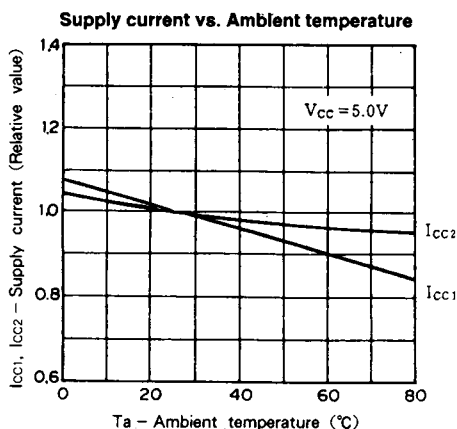
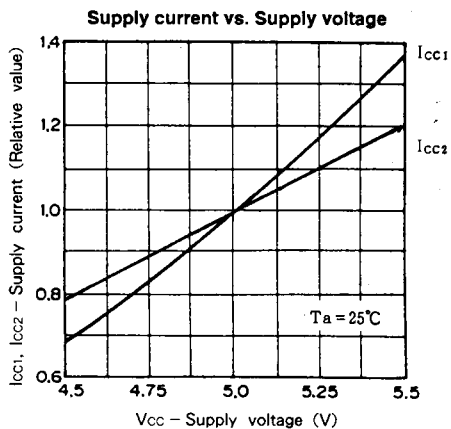
Data Retention Waveform

1. $\overline{CE1}$ control

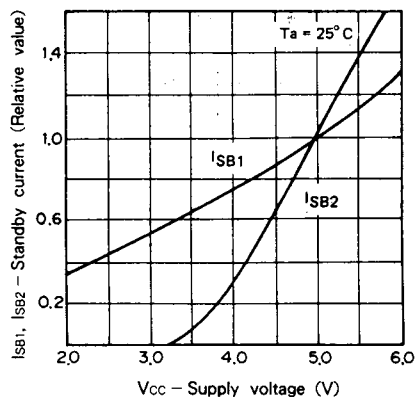
2. CE2 control



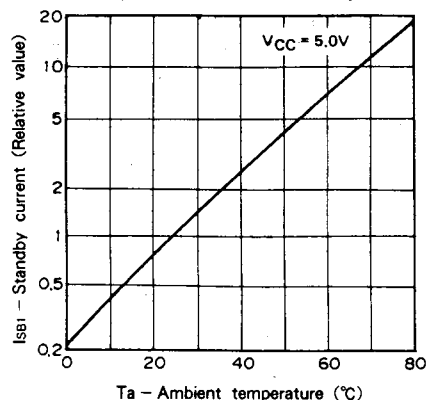
Example of Representative Characteristics



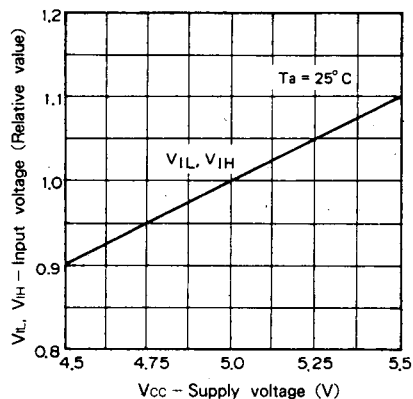
Standby current vs. Supply voltage



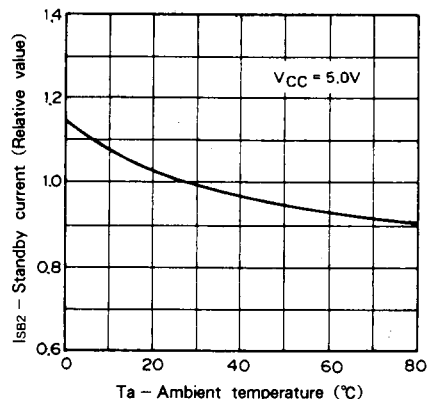
Standby current vs. Ambient temperature



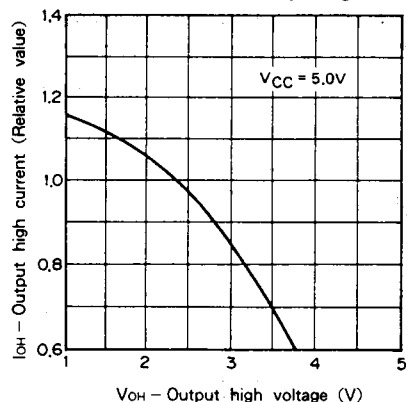
Input voltage level vs. Supply voltage



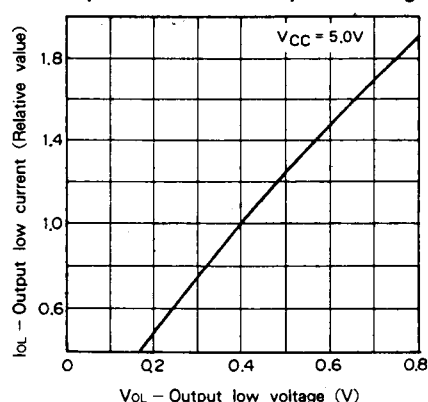
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

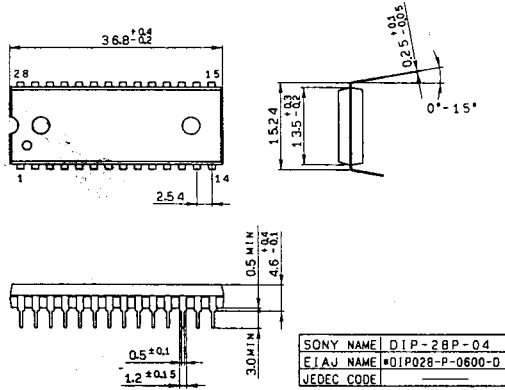


Output low current vs. Output low voltage

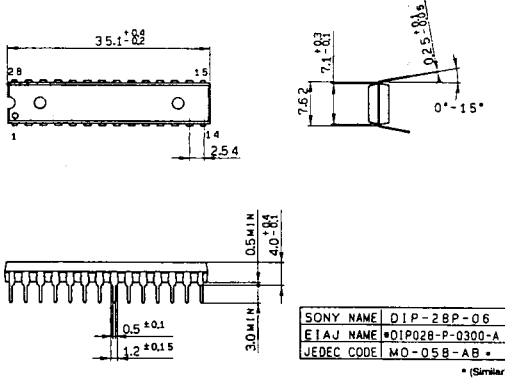


Package Outline Unit : mm

CXK5864BP 28 pin DIP (Plastic) 600mil 4.2g



CXK5864BSP 28 pin DIP (Plastic) 300mil 2.0g



CXK5864BM 28 pin SOP (Plastic) 450mil 0.7g

