RF2366

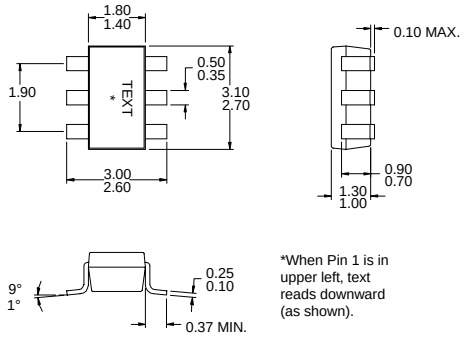
3V LOW NOISE AMPLIFIER/
3V PA DRIVER AMPLIFIER

Typical Applications

- CDMA PCS Bypass LNA
- CDMA PCS Bypass Driver Amplifier
- General Purpose Amplification
- Commercial and Consumer Systems

Product Description

The RF2366 is a switchable low noise amplifier with a very high dynamic range designed for digital cellular applications. The device functions as an outstanding front end low noise amplifier. When used as an LNA, the bias current can be set externally. When used as a PA driver, the IC can operate directly from a single cell Li-ion battery and includes a power down feature that can be used to completely turn off the device. The IC is featured in a standard SOT 6-lead plastic package.



All dimensions in mm.

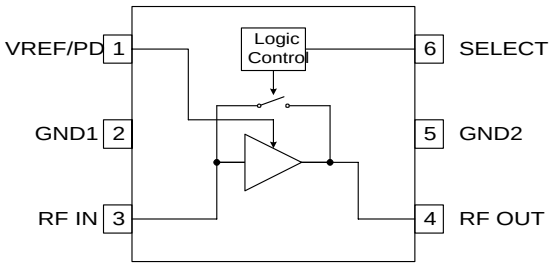
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: SOT 6-Lead

Features

- Low Noise and High Intercept Point
- Adjustable Bias Current
- Power Down Control
- Single 2.5V to 6.0V Power Supply
- 1000MHz to 2500MHz Operation
- Meets IS-98B Single-Tone and IMD



Functional Block Diagram

Ordering Information

RF2366	3V Low Noise Amplifier/ 3V PA Driver Amplifier)
RF2366 PCBA-PCS	Fully Assembled Evaluation Board (LNA)

RF Micro Devices, Inc.
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http://www.rfmd.com

Absolute Maximum Ratings

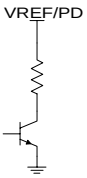
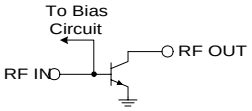
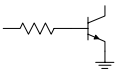
Parameter	Rating	Unit
Supply Voltage	-0.5 to +8.0	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

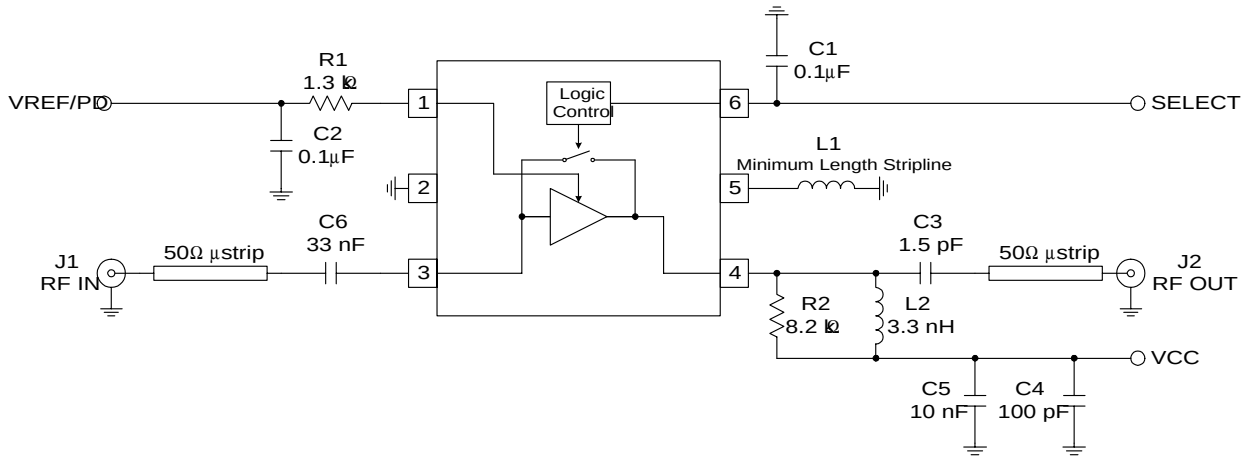
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T_{AMB}=25°C, V_{CC}=3.0V
PCS Low Noise Amplifier					RF=1930MHz to 1990MHz
Frequency Range		1930 to 1990		MHz	
HIGH GAIN MODE					Gain Select<0.8V, V_{PD}/V_{REF}=3V
Gain	10	12.5		dB	
Noise Figure		1.4	1.8	dB	
IIP3	9	14		dBm	
Current Drain		6.5		mA	
Input VSWR		1.8:1			
Output VSWR		1.6:1			
BYPASS MODE					Gain Select>1.8V, V_{PD}/V_{REF}=0V
Gain	-4.0	-2.5		dB	
IIP3		18.5		dBm	
Input VSWR		1.8:1	3:1		
Output VSWR		1.8:1	2.5:1		
Current Drain		0.85		mA	
PCS CDMA Driver					RF=1850MHz to 1910MHz
Frequency		1850 to 1910		MHz	
HIGH GAIN MODE					Gain Select<0.8V, V_{PD}/V_{REF}=3V
Gain		12		dB	
Noise Figure		1.6		dB	
Output Power	4			dBm	
ACPR1		-60		dBc/30kHz	P_{OUT}=+4dBm, ±1.25MHz offset
Input VSWR		1.9:1			
Output VSWR		1.6:1			
Current Drain		6.5		mA	
BYPASS MODE					Gain Select>1.8V, V_{PD}/V_{REF}=0V
Gain		-3		dB	
IIP3		17		dBm	
Input VSWR		2:1			
Output VSWR		1.5:1			
Current Drain		0.85		mA	
Power Supply					
Voltage (V_{CC})		3		V	
V_{SELECT} Low			0.8	V	High Gain mode. Select<0.8V, V_{PD}/V_{REF}=3V
V_{SELECT} High	1.8			V	Low Gain mode. Select>1.8V, V_{PD}/V_{REF}=0V
Power Down		10		µA	Gain Select<0.8V, V_{PD}/V_{REF}=0V, V_{CC}=0V

Bypass Possibility

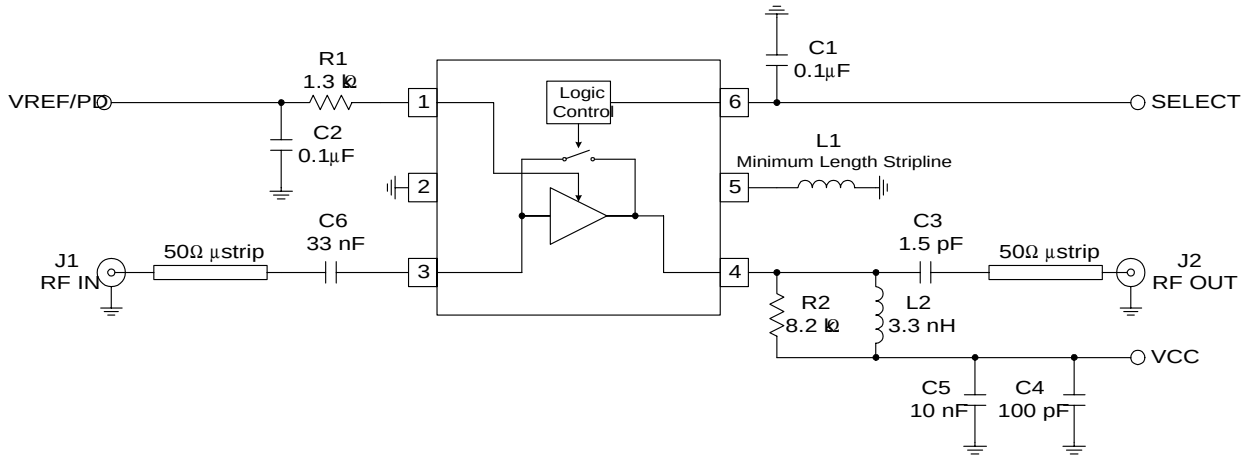
Gain Select	V_{PD}/V_{REF}	V_{CC}	Current	Comments
>1.8V	0V	3V	0.85mA	Recommended Bypass Mode
>1.8V	3V	3V	2mA	Alternative Bypass Mode

Pin	Function	Description	Interface Schematic
1	VREF/PD	For low noise amplifier applications, this pin is used to control the bias current. An external resistor can be used to set the bias current for any V_{PD} voltage.	
2	GND1	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
3	RF IN	RF input pin.	
4	RF OUT	Amplifier output pin. This pin is an open-collector output. It must be biased to V_{CC} through a choke or matching inductor. This pin is typically matched to 50Ω with a shunt bias/matching inductor and series blocking/matching capacitor. Refer to application schematics.	
5	GND2	LNA emittance inductance. Total inductance is comprised of package+bondwire+stripline (L1) on PCB.	
6	SELECT	This pin selects high gain and bypass. Select ≤ 0.8V, high gain. Select ≥ 1.8V, low gain.	

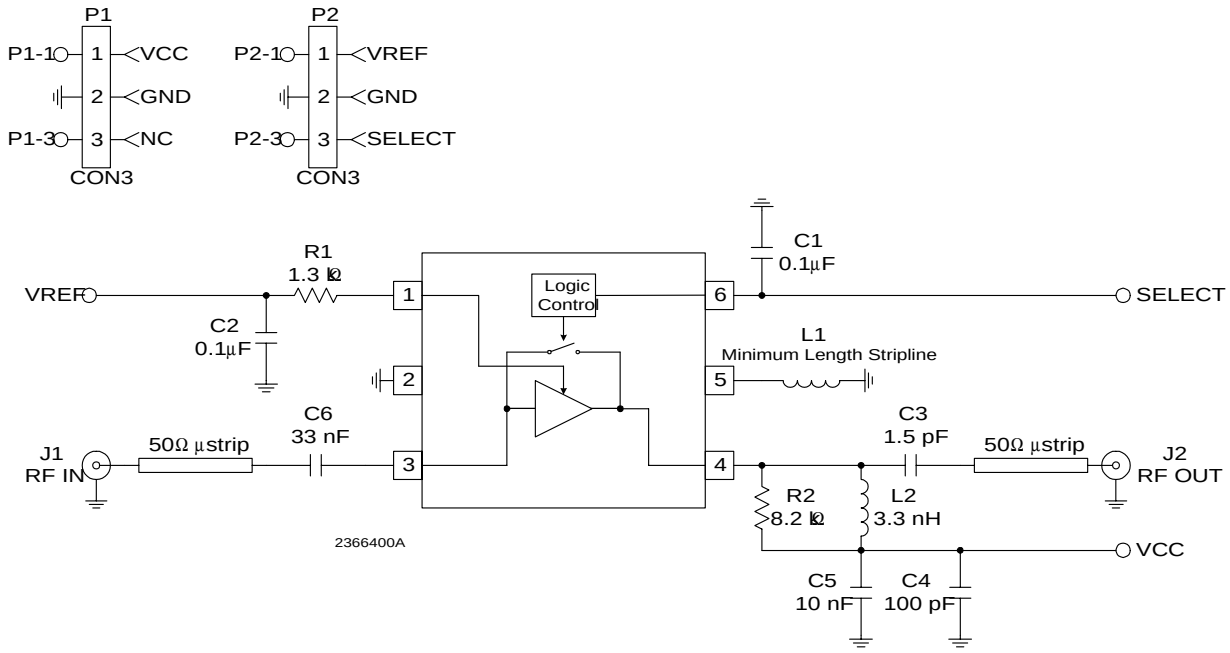
Application Schematic
PCS Low Noise Amplifier ~1950MHz



Application Schematic
PCS Driver Amplifier ~1880MHz



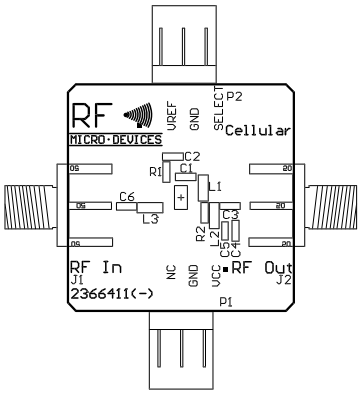
Evaluation Board Schematic - PCS LNA



Evaluation Board Layout - PCS
Board Size 1.0" x 1.0"

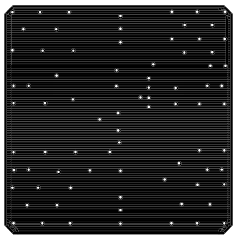
Board Thickness 0.031”, Board Material FR-4

Assembly

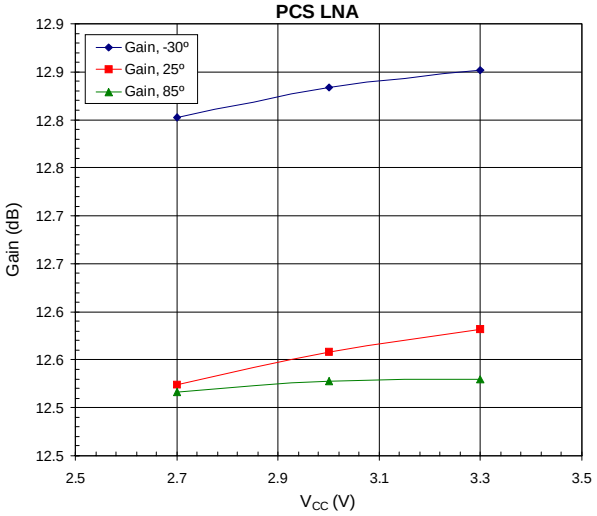


Top

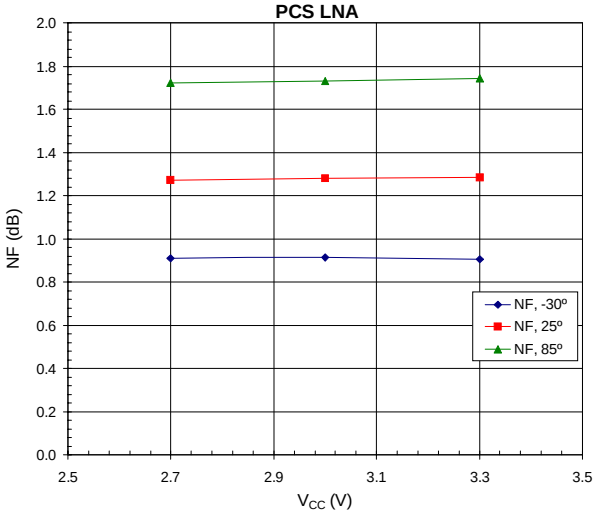
Back



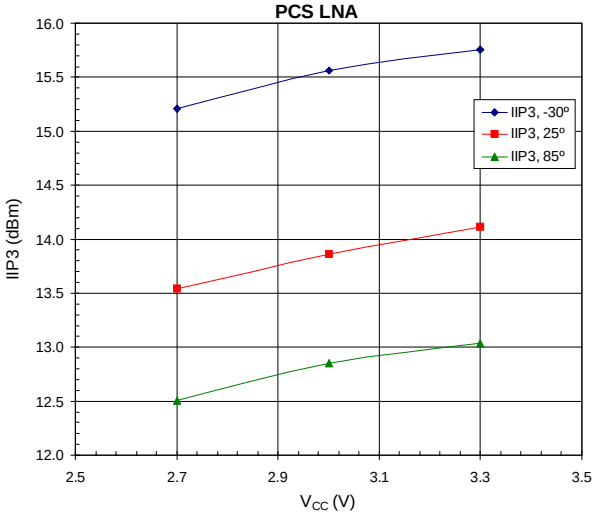
High Gain Mode Gain versus V_{CC}, PCS LNA



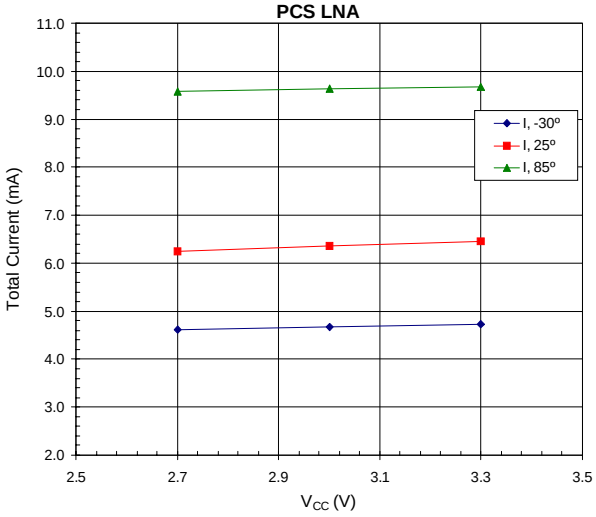
High Gain Mode NF versus V_{CC}, PCS LNA



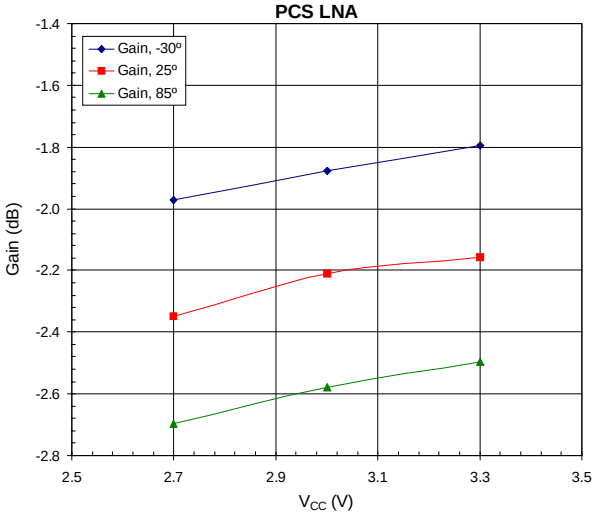
High Gain Mode IIP3 versus V_{CC}, PCS LNA



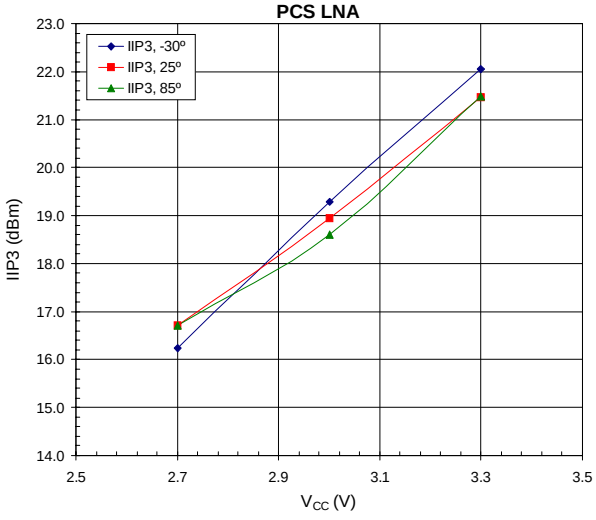
High Gain Mode Total Current versus V_{CC}, PCS LNA



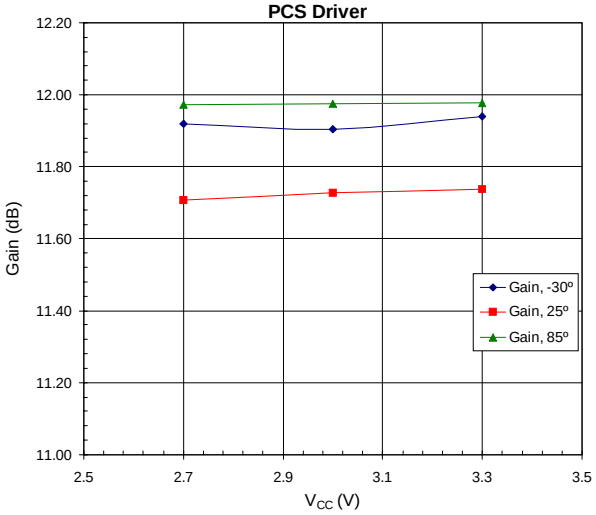
BYP Mode Gain versus V_{CC}, PCS LNA



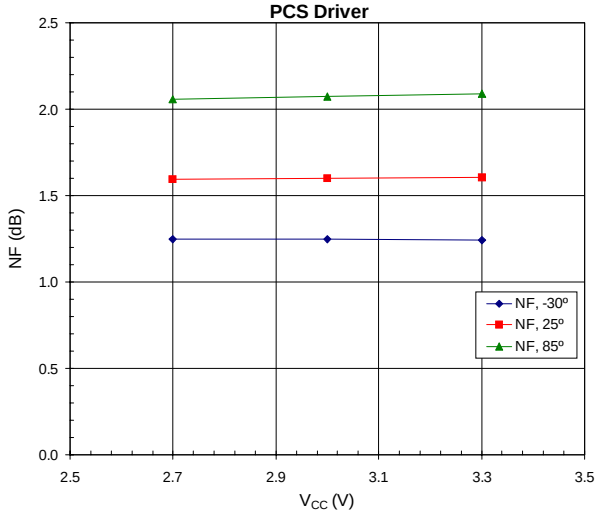
BYP Mode IIP3 versus V_{CC}, PCS LNA



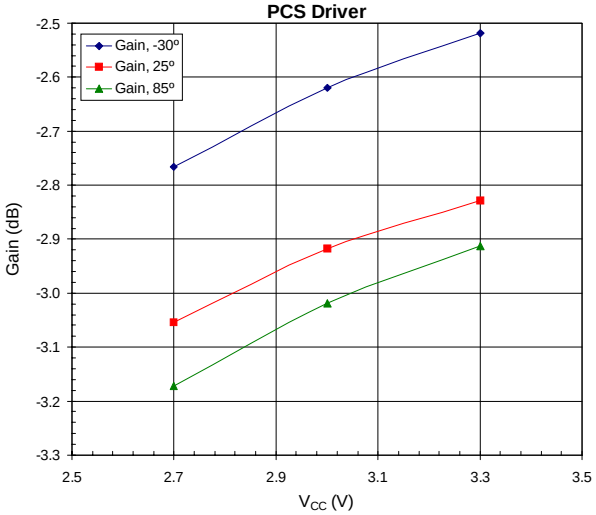
High Gain Mode Gain versus V_{CC}, PCS Driver



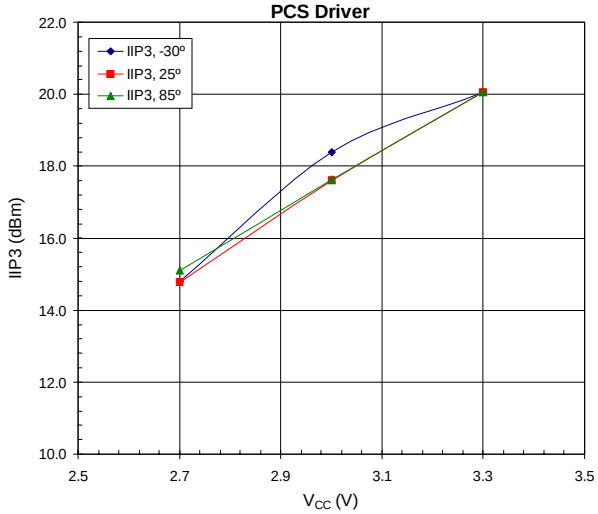
High Gain Mode NF versus V_{CC}, PCS Driver



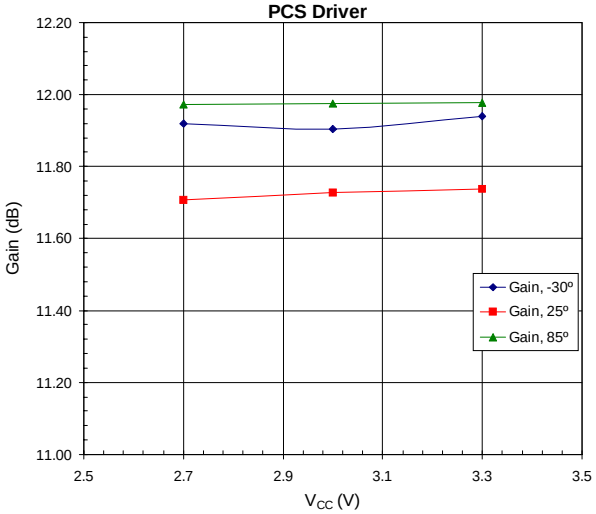
BYP Mode Gain versus V_{CC}, PCS Driver



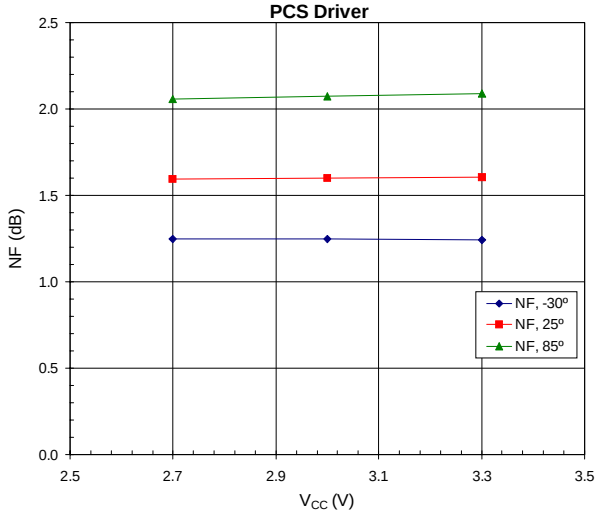
BYP Mode IIP3 versus V_{CC}, PCS Driver

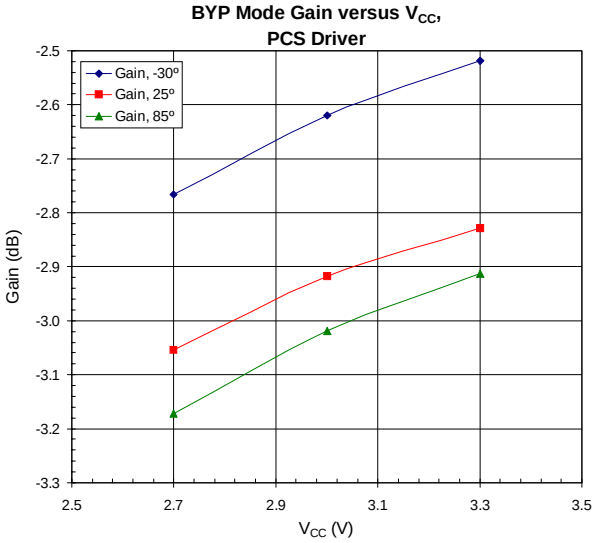


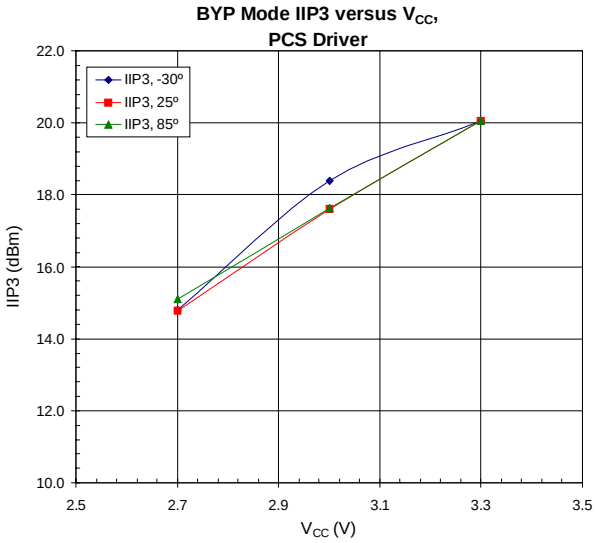
High Gain Mode Gain versus V_{CC}, PCS Driver



High Gain Mode NF versus V_{CC}, PCS Driver




BYP Mode Gain versus V_{CC}, PCS Driver
Gain, -30º
Gain, 25º
Gain, 85º
Gain (dB)
-2.5
-2.6
-2.7
-2.8
-2.9
-3.0
-3.1
-3.2
-3.3
2.5
2.7
2.9
3.1
3.3
3.5
V_{CC} (V)


BYP Mode IIP3 versus V_{CC}, PCS Driver
IIP3, -30º
IIP3, 25º
IIP3, 85º
IIP3 (dBm)
22.0
20.0
18.0
16.0
14.0
12.0
10.0
2.5
2.7
2.9
3.1
3.3
3.5
V_{CC} (V)