

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (L^2 - π -MOSV)

2SK2350

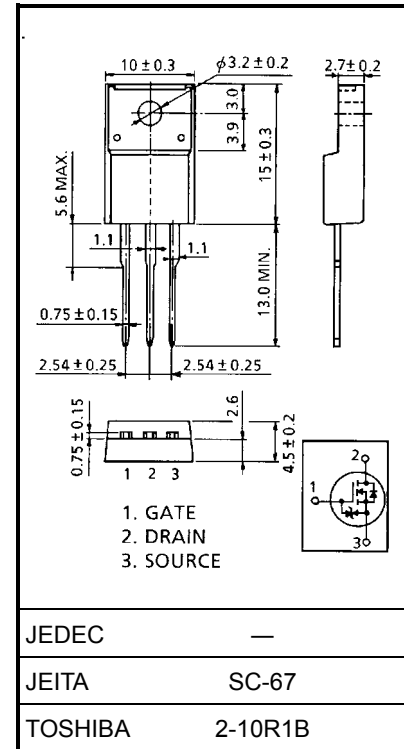
Switching Regulator, DC-DC Converter and Motor Drive Applications

Unit: mm

- 4 V gate drive
- Low drain-source ON resistance : $R_{DS(ON)} = 0.26 \Omega$ (typ.)
- High forward transfer admittance : $|Y_{fs}| = 8 S$ (typ.)
- Low leakage current : $I_{DSS} = 100 \mu A$ (max) ($V_{DS} = 200 V$)
- Enhancement-mode : $V_{th} = 1.5 \sim 3.5 V$ ($V_{DS} = 10 V$, $I_D = 1 mA$)

Maximum Ratings ($T_a = 25^\circ C$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	200	V
Drain-gate voltage ($R_{GS} = 20 k\Omega$)		V_{DGR}	200	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	8.5	A
	Pulse (Note 1)	I_{DP}	34	A
Drain power dissipation ($T_c = 25^\circ C$)		P_D	30	W
Single pulse avalanche energy (Note 2)		E_{AS}	110	mJ
Avalanche current		I_{AR}	8.5	A
Repetitive avalanche energy (Note 3)		E_{AR}	3	mJ
Channel temperature		T_{ch}	150	$^\circ C$
Storage temperature range		T_{stg}	$-55 \sim 150$	$^\circ C$



Weight: 1.9 g (typ.)

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	4.16	$^\circ C / W$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	62.5	$^\circ C / W$

Note 1: Please use devices on condition that the channel temperature is below $150^\circ C$.

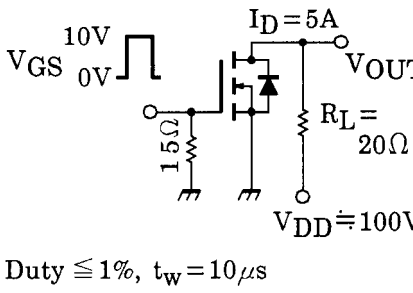
Note 2: $V_{DD} = 50 V$, $T_{ch} = 25^\circ C$ (initial), $L = 2.47 mH$, $R_G = 25 \Omega$, $I_{AR} = 8.5 A$

Note 3: Repetitive rating; Pulse width limited by maximum channel temperature.

This transistor is an electrostatic sensitive device.

Please handle with caution.

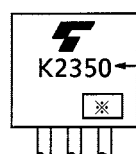
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 200 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	200	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	1.5	—	3.5	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	—	0.26	0.4	Ω
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 5 \text{ A}$	4	8	—	S
Input capacitance		C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	700	—	pF
Reverse transfer capacitance		C_{rss}		—	80	—	
Output capacitance		C_{oss}		—	270	—	
Switching time	Rise time	t_r		—	15	—	ns
	Turn-on time	t_{on}		—	25	—	
	Fall time	t_f		—	15	—	
	Turn-off time	t_{off}		—	70	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	$V_{DD} \approx 160 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	—	17	—	nC
Gate-source charge		Q_{gs}		—	10	—	
Gate-drain ("miller") charge		Q_{gd}		—	7	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	8.5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	34	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 10 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-2.0	V
Reverse recovery time	t_{rr}	$I_{DR} = 10 \text{ A}, V_{GS} = 0 \text{ V}$	—	155	—	ns
Reverse recovered charge	Q_{rr}	$dI_{DR} / dt = 100 \text{ A} / \mu\text{s}$	—	0.8	—	μC

Marking



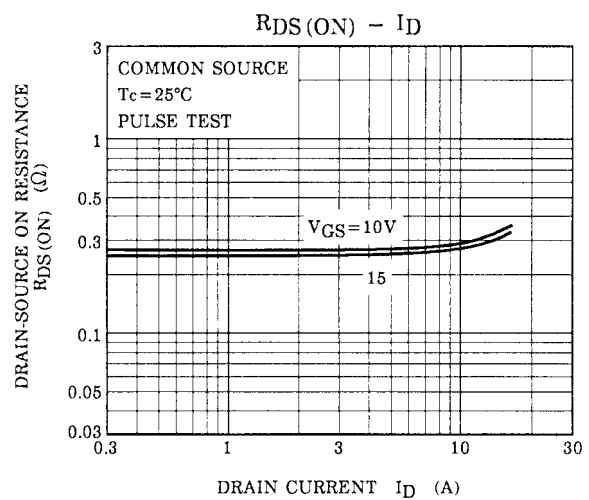
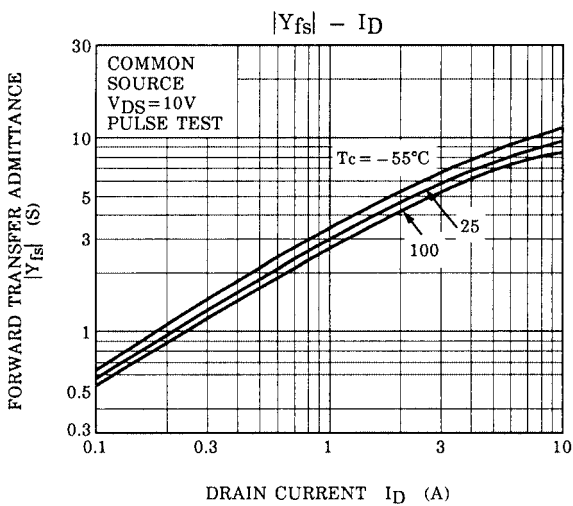
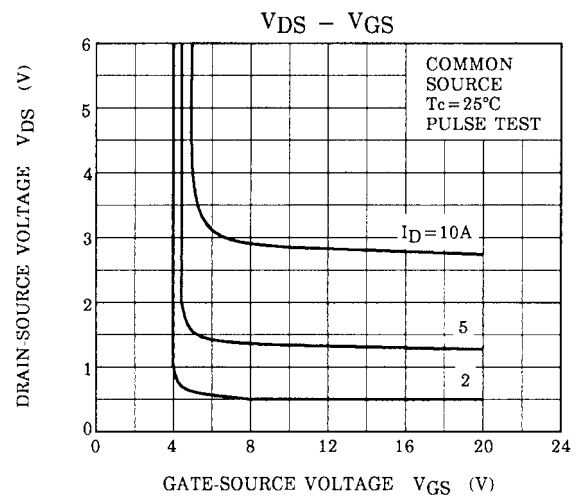
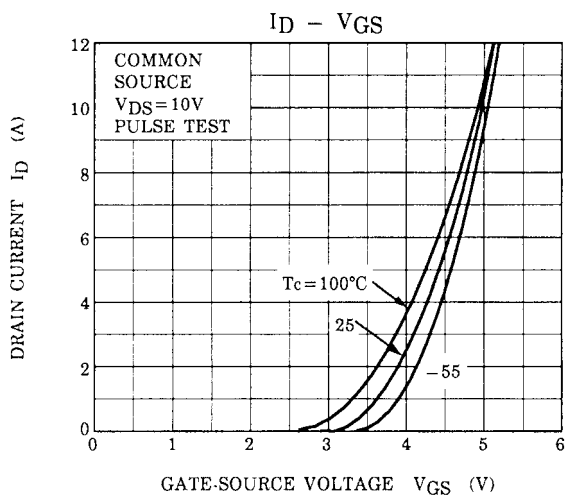
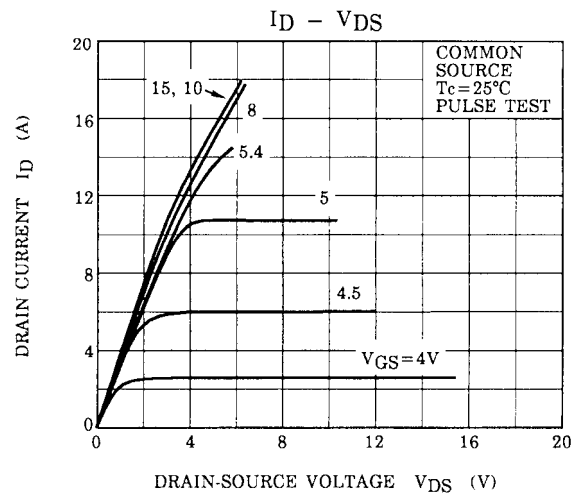
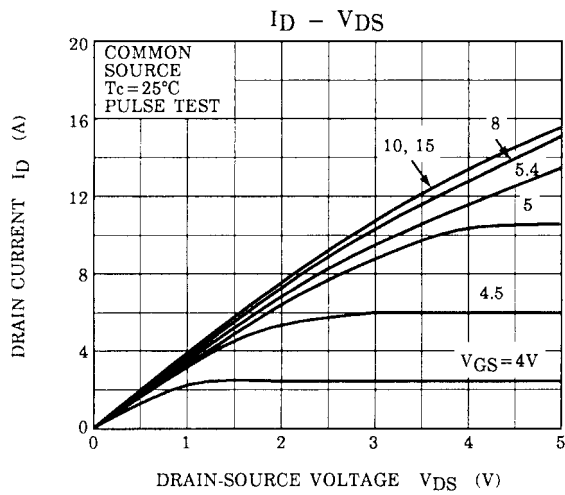
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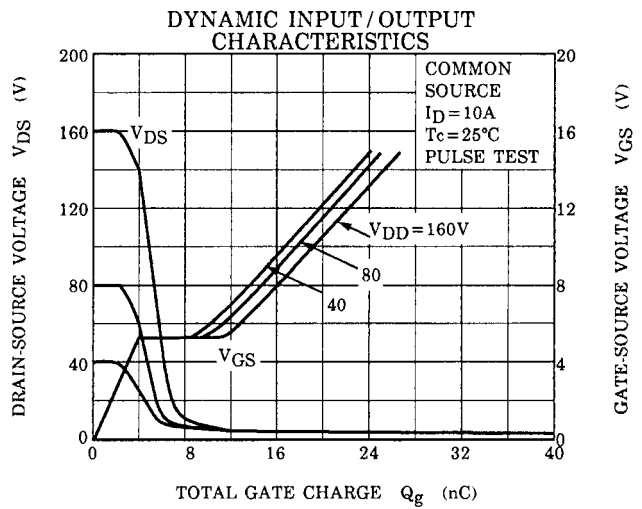
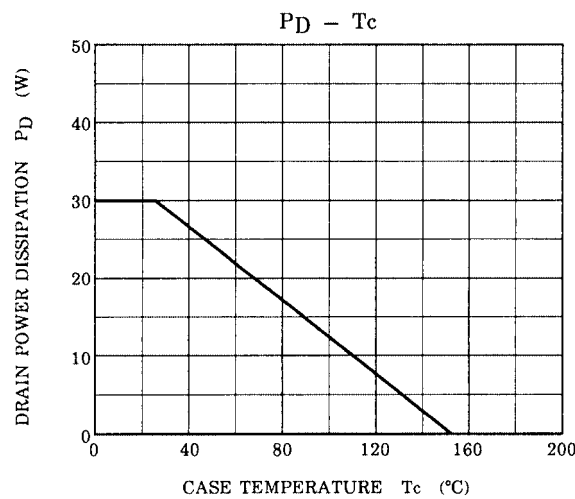
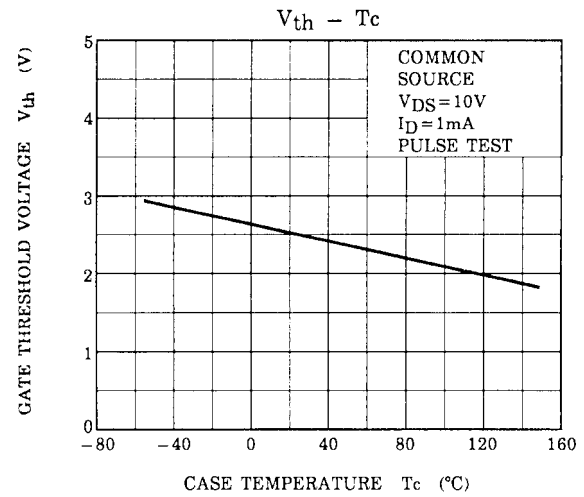
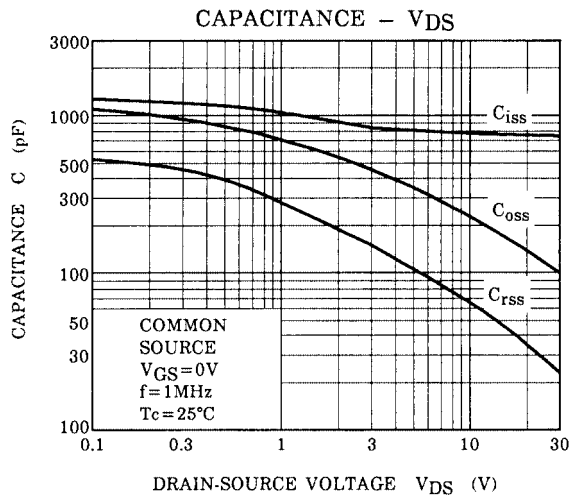
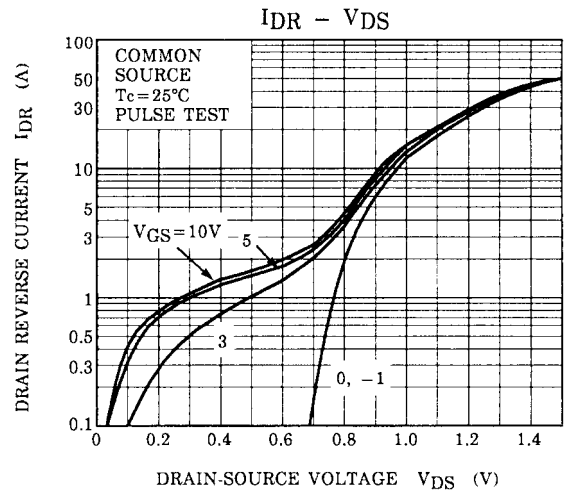
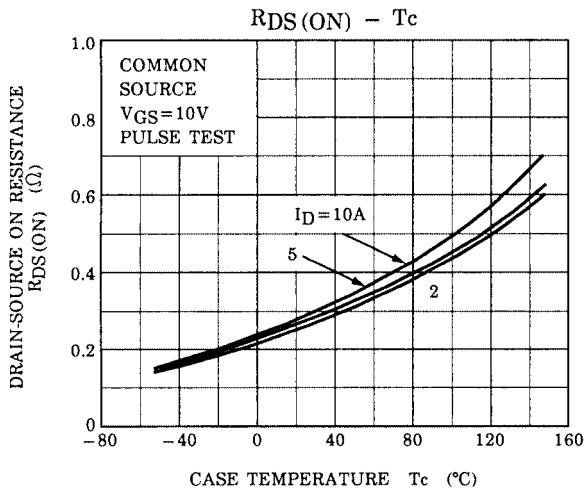
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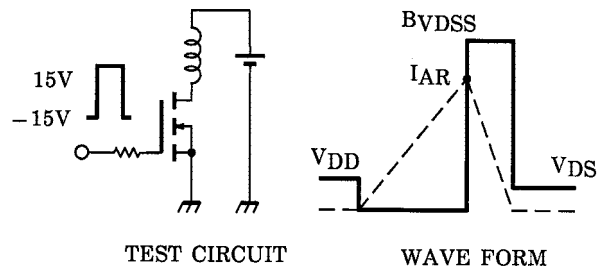
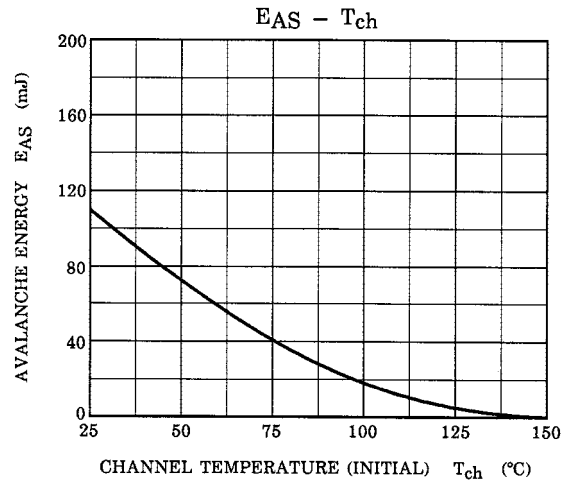
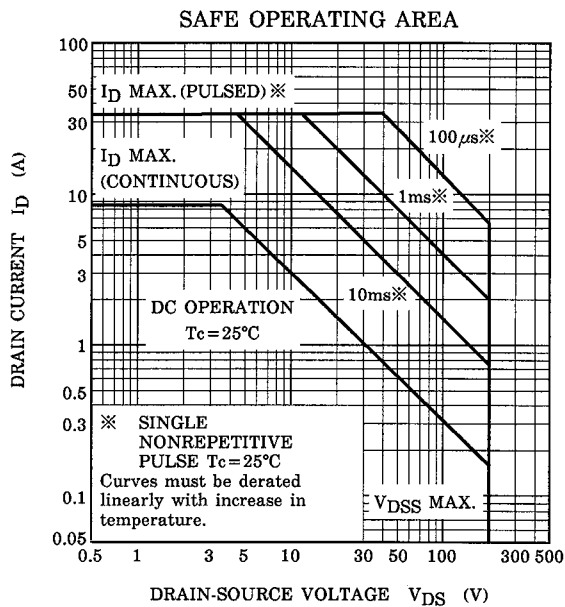
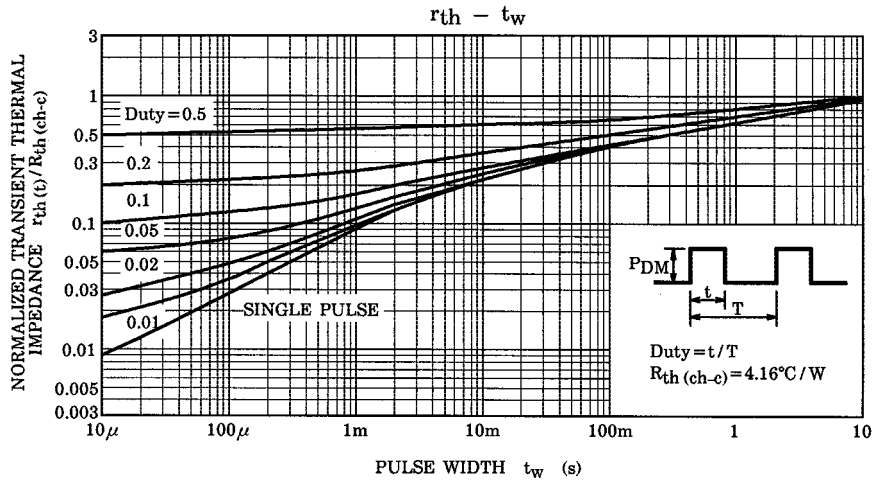


Month (Starting from Alphabet A)

Year (Last Number of the Christian Era)







$$R_G = 25 \, \Omega$$

$$V_{DD} = 50 \, V, L = 2.47 \, mH$$

$$E_{AS} = \frac{1}{2} \cdot I^2 \cdot \left(\frac{BVDSS}{BVDSS - V_{DD}} \right)$$

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