

6N137

Digital Logic Isolation

Tele-Communication

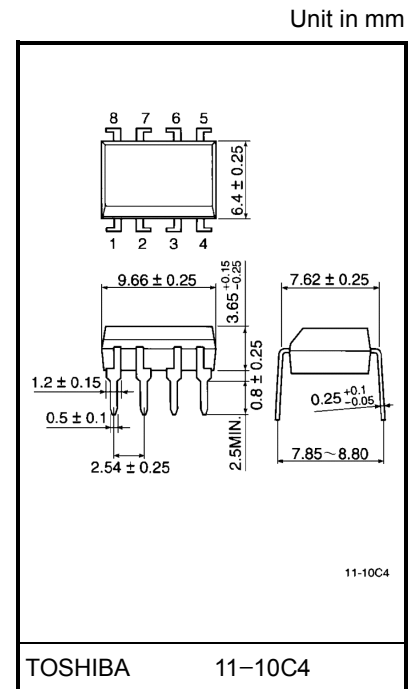
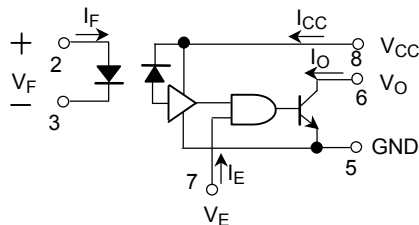
Analog Data Equipment Control

The TOSHIBA 6N137 consist of a high emitting diode and a one chip photo IC. This unit is 8-lead DIP package.

- LSTTL / TTL compatible: 5V Supply
- Ultra high speed: 10MBd
- Guaranteed performance over temperature: 0°C to 70°C
- High isolation voltage: 2500Vrms min.
- UL recognized: UL1577, file no. E67349

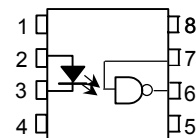
Truth Table

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H



Weight: 0.54g

Pin Configurations (top view)



- 1 : N.C.
- 2 : Anode
- 3 : Cathode
- 4 : N.C.
- 5 : GND
- 6 : Output(Open collector)
- 7 : Enable
- 8 : V_{CC}

Maximum Ratings

Characteristic		Symbol	Rating	Unit
LED	Forward current	I_F	20	mA
	Pulse forward current (Note 1)	I_{FP}	40	mA
	Reverse voltage	V_R	5	V
Detector	Output current	I_O	50	mA
	Output voltage	V_O	7	V
	Supply voltage (1 minute maximum)	V_{CC}	7	V
	Enable input voltage (not to exceed V_{CC} by more than 500mV)	V_{EH}	5.5	V
	Output collector power dissipation	P_O	85	mW
Operating temperature range		T_{opr}	0~70	°C
Storage temperature range		T_{stg}	-55~125	°C
Lead solder temperature (10 s) (Note 2)		T_{sol}	260	°C

(Note 1) 50% duty cycle, 1ms pulse width.

(Note 2) Soldering portion of lead: Up to 2mm from the body of the device.

Recommended Operating Conditions

Characteristic	Symbol	Min.	Max.	Unit
Input current, low level each channel	I_{FL}	0	250	μA
Input current, high level each channel	I_{FH}	7	20	mA
High level enable voltage	V_{EH}	2.0	V_{CC}	V
Low level enable voltage (output high)	V_{EL}	0	0.8	V
Supply voltage, output	V_{CC}	4.5	5.5	V
Fan out (TTL load)	N	—	8	—
Operating temperature	T_a	0	70	°C

Precaution

Please be careful of the followings.

A ceramic capacitor(0.1μF)should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

Electrical Characteristics
Over Recommended Temperature ($T_a = 0\sim 70^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	(**)Typ.	Max.	Unit
High level output current	I_{OH}	$V_{CC}=5.5\text{V}$, $V_O=5.5\text{V}$ $I_F=250\mu\text{A}$, $V_E = 2.0\text{V}$	—	1	250	μA
Low level output voltage	V_{OL}	$V_{CC}=5.5\text{V}$, $I_F=5\text{mA}$ $V_{EH}=2.0\text{V}$ $I_{OL}(\text{sinking})=13\text{mA}$	—	0.4	0.6	V
High level enable current	I_{EH}	$V_{CC}=5.5\text{V}$, $V_E=2.0\text{V}$	—	-1.0	—	mA
Low level enable current	I_{EL}	$V_{CC}=5.5\text{V}$, $V_E=0.5\text{V}$	—	-1.6	-2.0	mA
High level supply current	I_{CCH}	$V_{CC}=5.5\text{V}$, $I_F=0$, $V_E=0.5\text{V}$	—	7	15	mA
Low level supply current	I_{CCL}	$V_{CC}=5.5\text{V}$, $I_F=10\text{mA}$ $V_E=0.5\text{V}$	—	12	18	mA
Resistance (input-output) (Note 3)	R_{I-O}	$V_{I-O}=500\text{V}$, $T_a=25^\circ\text{C}$ R.H. $\leq 60\%$	—	10^{12}	—	Ω
Capacitance (input-output) (Note 3)	C_{I-O}	$f=1\text{MHz}$, $T_a=25^\circ\text{C}$	—	0.6	—	pF
Input forward voltage	V_F	$I_F=10\text{mA}$, $T_a=25^\circ\text{C}$	—	1.65	1.75	V
Input reverse breakdown voltage	BV_R	$I_R=10\mu\text{A}$, $T_a=25^\circ\text{C}$	5	—	—	V
Input capacitance	C_{IN}	$V_F=0$, $f=1\text{MHz}$	—	45	—	pF
Current transfer ratio	CTR	$I_F=5.0\text{mA}$, $R_L=100\Omega$	—	1000	—	%

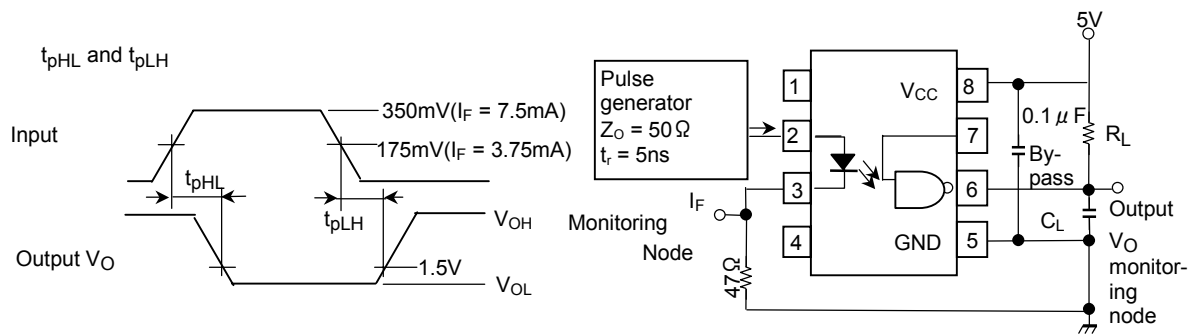
(**) All typical values are at $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$

(Note 3) Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Switching Characteristics ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$)

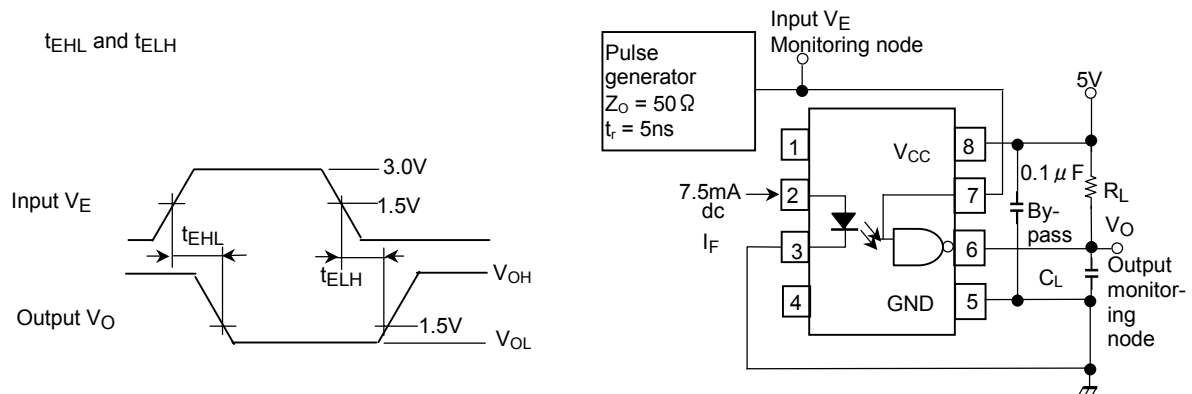
Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time to high output level	t_{pLH}	1	$R_L=350\Omega$, $C_L=15\text{pF}$ $I_F=7.5\text{mA}$	—	60	75	ns
Propagation delay time to low output level	t_{pHL}	1	$R_L=350\Omega$, $C_L=15\text{pF}$ $I_F=7.5\text{mA}$	—	60	75	ns
Output rise–fall time (10–90%)	t_r , t_f	—	$R_L=350\Omega$, $C_L=15\text{pF}$ $I_F=7.5\text{mA}$	—	30	—	ns
Propagation delay time of enable from V_{EH} to V_{EL}	t_{ELH}	2	$R_L=350\Omega$, $C_L=15\text{pF}$ $I_F=7.5\text{mA}$ $V_{EH}=3.0\text{V}$ $V_{EL}=0.5\text{V}$	—	25	—	ns
Propagation delay time of enable from V_{EL} to V_{EH}	t_{EHL}	2	$R_L=350\Omega$, $C_L=15\text{pF}$ $I_F=7.5\text{mA}$ $V_{EH}=3.0\text{V}$ $V_{EL}=0.5\text{V}$	—	25	—	ns
Common mode transient immunity at logic high output level	CM_H	3	$V_{CM}=10\text{V}$ $R_L=350\Omega$ $V_{O(\min.)}=2\text{V}$ $I_F=0\text{mA}$	—	200	—	V / μs
Common mode transient immunity at logic low output level	CM_L	3	$V_{CM}=10\text{V}$ $R_L=350\Omega$ $V_{O(\max.)}=0.8\text{V}$ $I_F=5\text{mA}$	—	–500	—	V / μs

Test Circuit 1.



- C_L is approximately 15pF which includes probe and stray wiring capacitance.

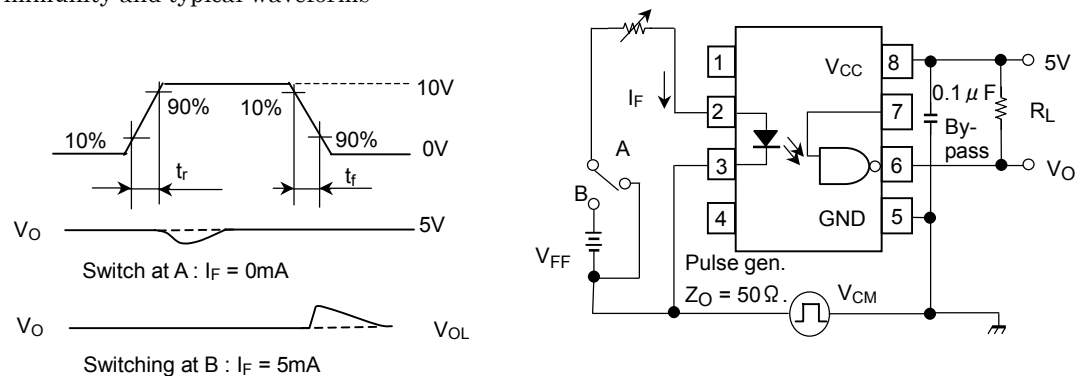
Test Circuit 2.

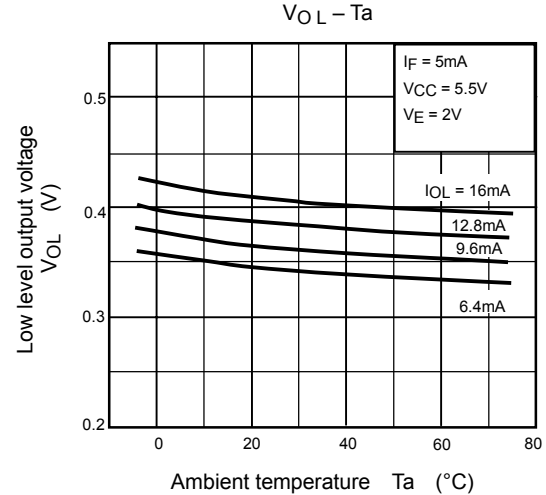
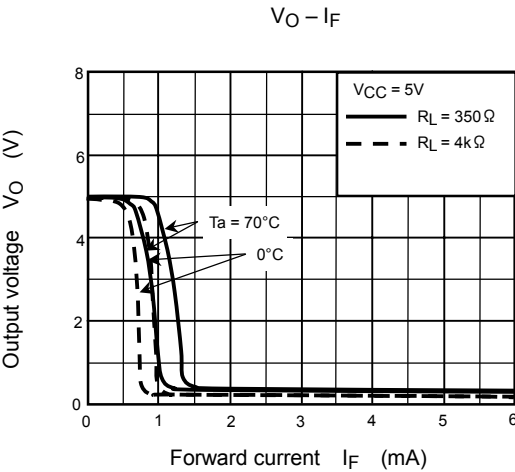
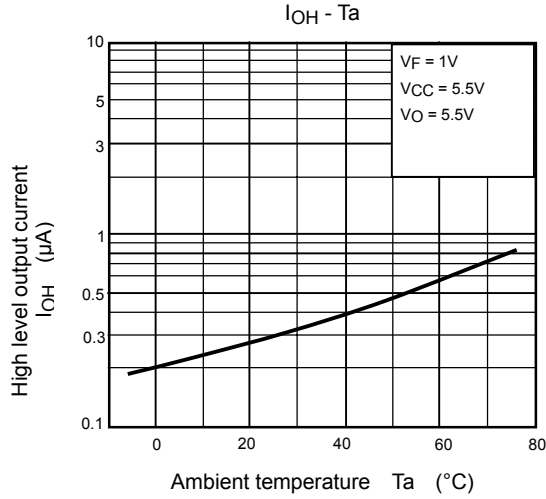
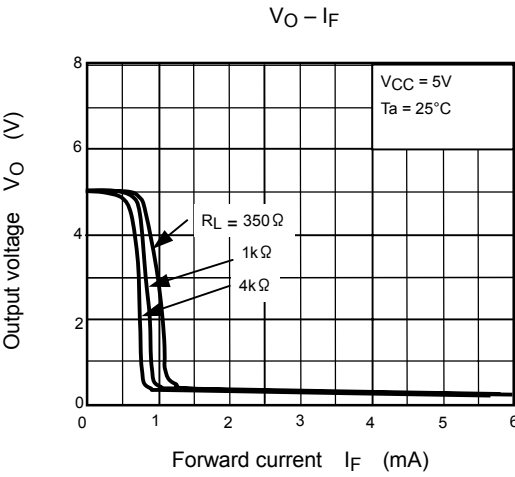
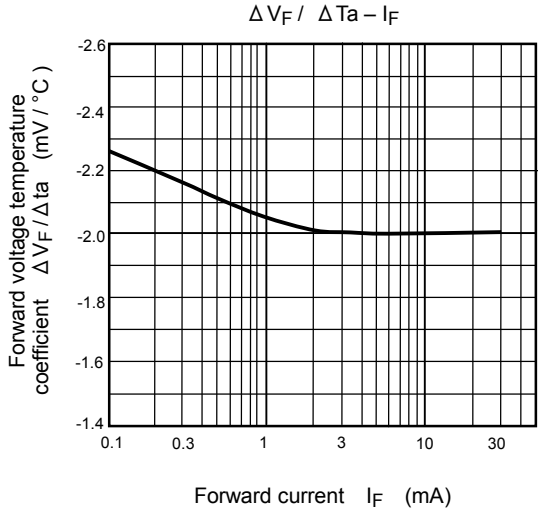
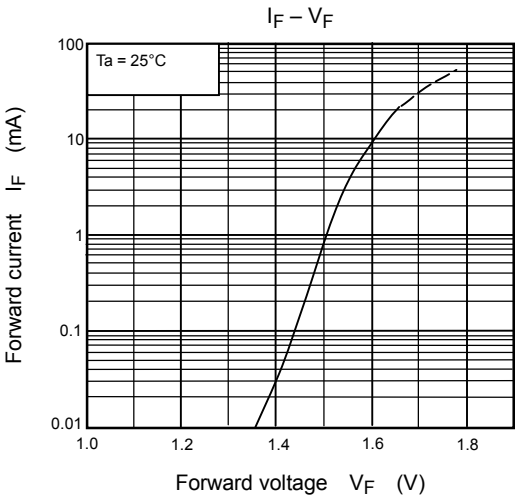


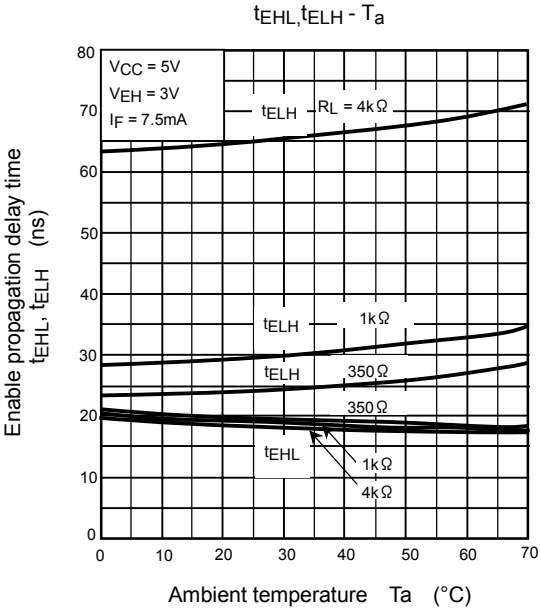
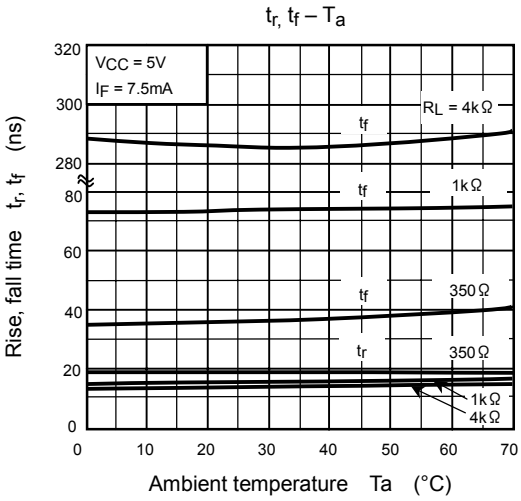
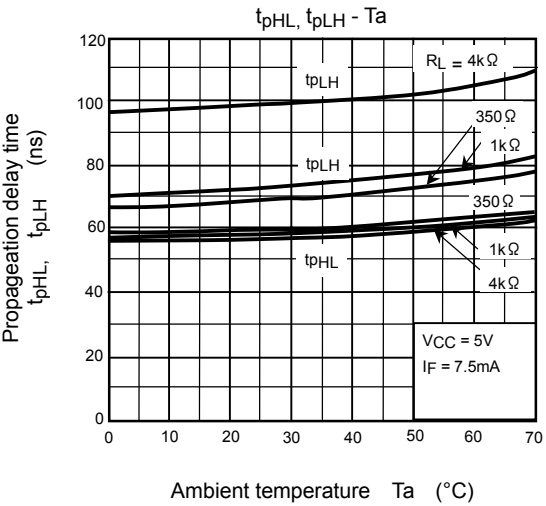
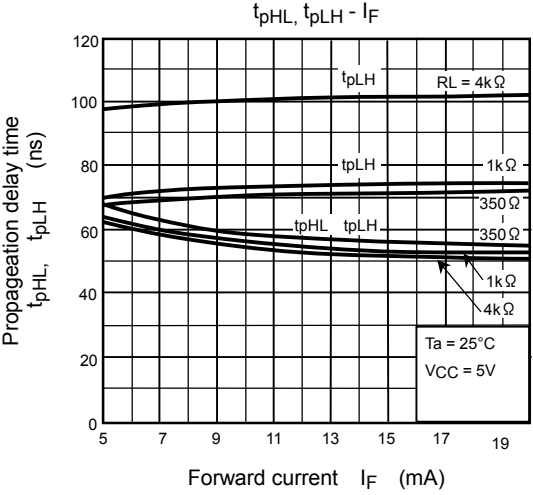
- C_L is approximately 15pF which includes prove and stray wiring capacitance.

Test Circuit 3.

Transient immunity and typical waveforms







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