

TOSHIBA MOS MEMORY PRODUCTS

4096 WORD x 1 BIT CMOS STATIC RAM

TC5504AP-2/-3, TC5504APL-2/-3

SILICON GATE CMOS

DESCRIPTION

The TC5504AP is a 4,096 bit high speed and low power static random access memory organized as 4,096 words by 1 bit using CMOS technology, and operates from a single 5-volt supply.

On chip latches are provided for addresses, data input and output, and read write control allowing efficient interfacing with microprocessor systems.

The TC5504AP is a fully CMOS RAM, therefore it is suited for use in low power applications where battery operation and battery back up for non-

volatility are required. Furthermore the TC5504APL guaranteed a standby current equal to or less than $1\mu\text{A}$ at 60°C ambient temperature.

The TC5504AP is guaranteed for data retention at a power supply as low as 2 volts. The TC5504AP is directly TTL compatible in all inputs and output.

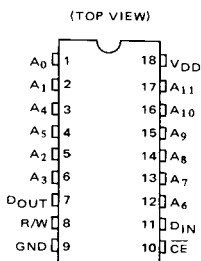
The TC5504AP is offered in both standard 18 pin plastic and cerdip packages, 0.3 inch in width.

FEATURES

- Standby Current
 $0.2\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
 $1.0\mu\text{A}$ (Max.) at $T_a = 60^\circ\text{C}$: TC5504APL
 $20\mu\text{A}$ (Max.) : TC5504AP
- Low Power Dissipation : 15mW (Typ.) operating
- Single 5V Power Supply : $5\text{V} \pm 10\%$
- Data Retention Supply Voltage : $2 \sim 5.5\text{V}$
- All Inputs and Output : Directly TTL Compatible

- Access Time
 200ns (Max.) : TC5504AP/APL-2
 300ns (Max.) : TC5504AP/APL-3
- Static Operation
- On Chip Address Register
- Three State Output
- Package
Plastic DIP : TC5504AP/APL

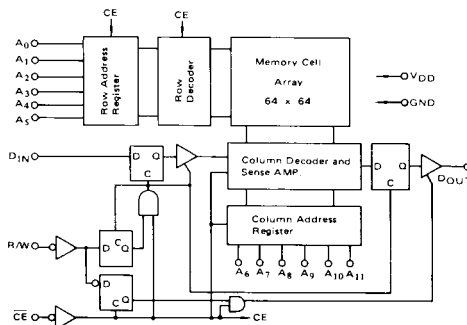
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{11}$	Address Inputs
R/W	Read Write Control Input
$\overline{\text{CE}}$	Chip Enable Input
D_{IN}	Data Input
D_{OUT}	Data Output
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	$-0.3 \sim 7.0$	V
V_{IN}	Input Voltage	$-0.3 \sim 7.0$	V
V_{OUT}	Output Voltage	$0 \sim V_{DD}$	V
P_D	Power Dissipation ($T_a = 85^\circ\text{C}$)	TC5504AP/APL 550	mW
T_{SOLDER}	Soldering Temperature - Time	260 - 10	$^\circ\text{C} \cdot \text{sec}$
T_{STG}	Storage Temperature	$-55 \sim 150$	$^\circ\text{C}$
T_{OPR}	Operating Temperature	$-30 \sim 85$	$^\circ\text{C}$

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V
V_{DH}	Data Retention Voltage	2.0	—	5.5	V

D.C. CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = -30^\circ\text{C}$ to 85°C , unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP. (1)	MAX.	UNIT
I _{IL}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{DD}			—	—	± 1.0	μA
I _{LO}	Output Leakage Current	CE = V _{DD} − 0.2V, 0V ≤ V _{OUT} ≤ V _{DD}			—	—	± 5.0	μA
I _{OH}	Output High Level Current	V _{OH} = 2.4V			−1.0	—	—	mA
I _{OL}	Output Low Level Current	V _{OL} = 0.4V			2.0	—	—	mA
I _{DD5}	Standby Current	V _{DD} = 2V ~ 5.5V CE = V _{DD} − 0.2V other inputs = 0.2V or V _{DD} − 0.2V	TC5504APL	T _a = 25°C	—	—	0.2	μA
				T _a = 60°C	—	—	1.0	
			TC5504AP	—	0.05	20	μA	
I _{DD01}	Operating Current	t _{cycle} = 1μs, I _{OUT} = 0mA			—	—	10.0	mA
I _{DD02}		t _{cycle} = 1μs, V _{IH} = V _{DD} , V _{IL} = 0V, I _{OUT} = 0mA			—	3.0	5.0	mA

Note (1) $V_{DD} = 5V$, $T_a = 25^\circ\text{C}$

CAPACITANCE¹⁾ ($T_a = 25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$ $f = 1\text{MHz}$	—	4	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$ $f = 1\text{MHz}$	—	5	10	pF

Note (2): This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($V_{DD} = 5V \pm 10\%$, $T_a = -30^\circ\text{C}$ to 85°C , unless otherwise noted)

SYMBOL	PARAMETER	TC5504AP-2/APL-2		TC5504AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	300	—	420	—	ns
t_{WC}	Write Cycle Time	300	—	420	—	ns
t_{RMWC}	Read Modify Write Cycle Time	390	—	580	—	ns
t_{AS}	Address Setup Time	5	—	5	—	ns
t_{AH}	Address Hold Time	60	—	80	—	ns
t_{PC}	Precharge Time	80	—	100	—	ns
t_{CEH}	Chip Enable Hold Time	200	—	300	—	ns
t_{ACC}	Access Time	—	200	—	300	ns
t_{OD}	Output Disable Time	—	70	—	100	ns
t_{COE}	Output Enable Time	0	—	0	—	ns
t_{RS}	Read Setup Time	0	—	0	—	ns
t_{RH}	Read Hold Time	0	—	0	—	ns
t_{WS}	Write Setup Time	0	—	0	—	ns
t_{WH}	Write Hold Time	60	—	80	—	ns
t_{DS}	Data Setup Time	5	—	5	—	ns
t_{DH}	Data Hold Time	60	—	80	—	ns
t_{WCH}	Write Enable to CE Hold Time	80	—	150	—	ns
t_{MD}	Modify Time	0	—	0	—	ns

A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels : 0.6 ~ 2.4V

Timing Measurement Reference Levels

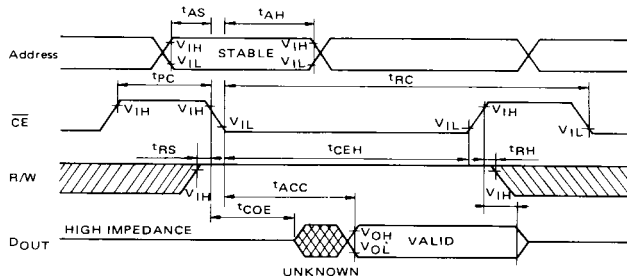
Input : 0.8V and 2.2V

Output : 0.8V and 2.2V

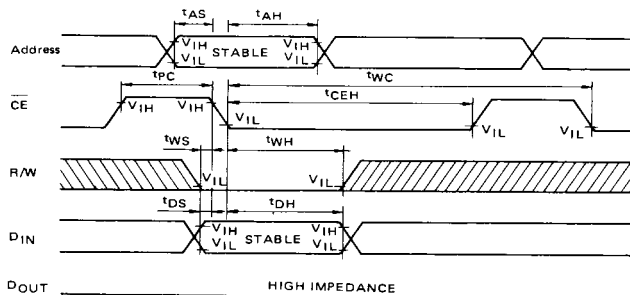
Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS

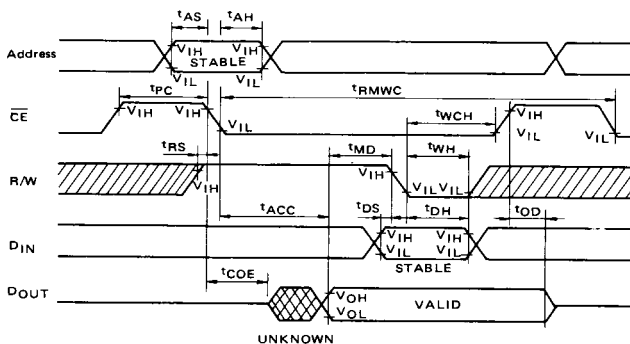
• READ CYCLE



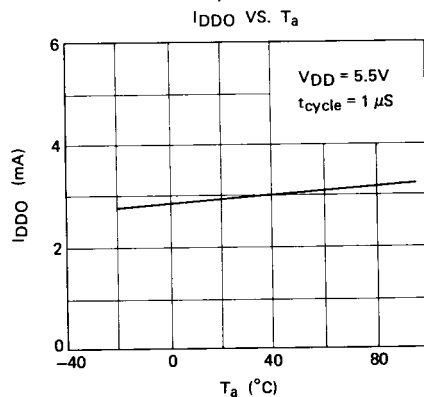
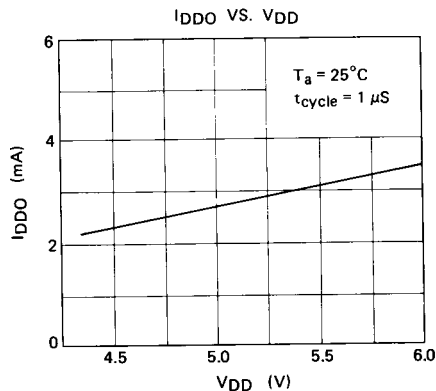
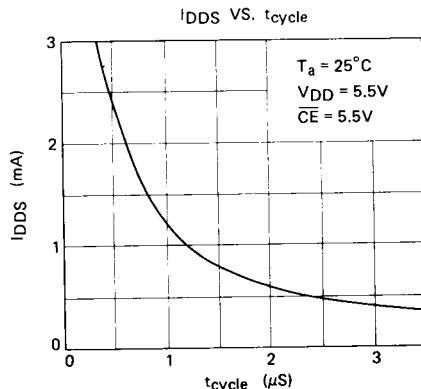
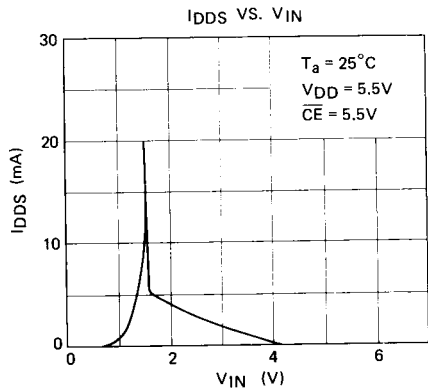
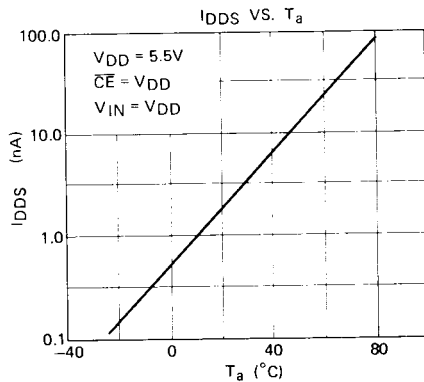
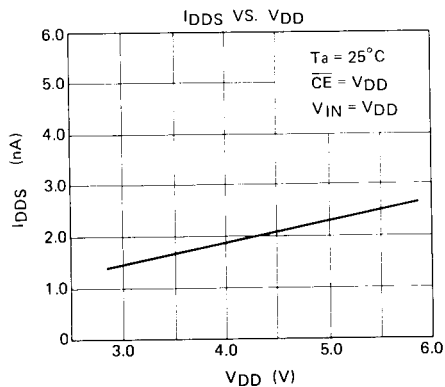
• WRITE CYCLE



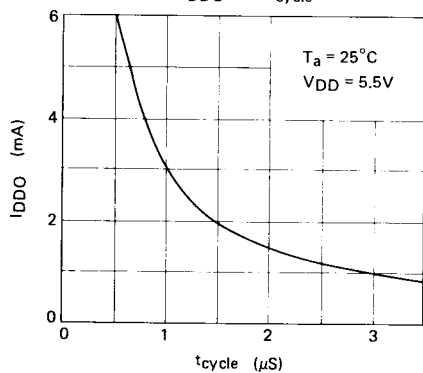
• READ MODIFY WRITE CYCLE



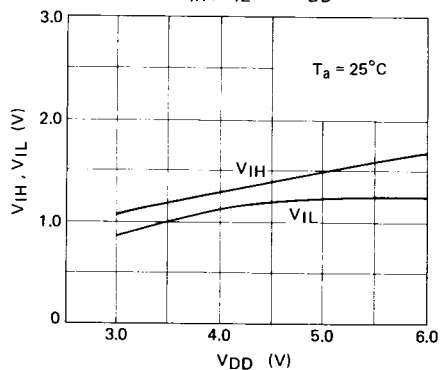
TYPICAL CHARACTERISTICS



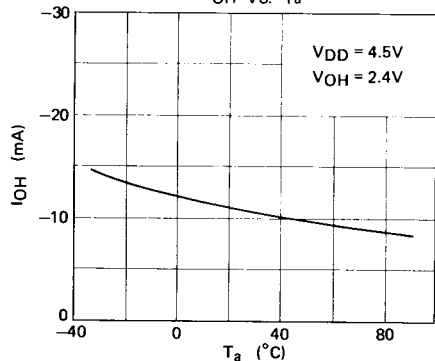
I_{DDO} VS. t_{cycle}



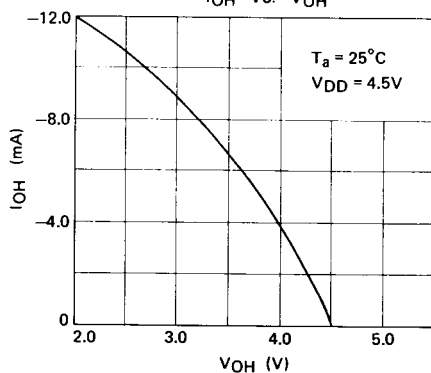
V_{IH} , V_{IL} VS. V_{DD}



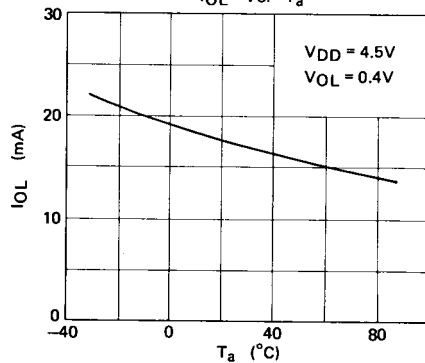
I_{OH} VS. T_a



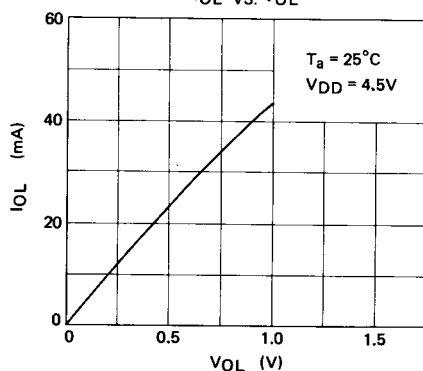
I_{OH} VS. V_{OH}

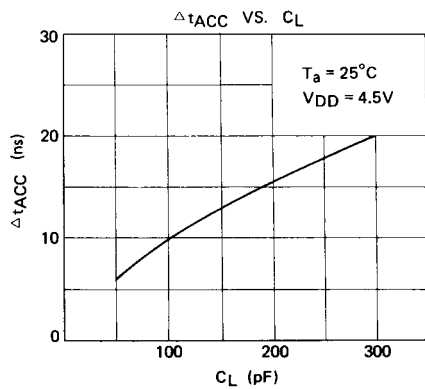
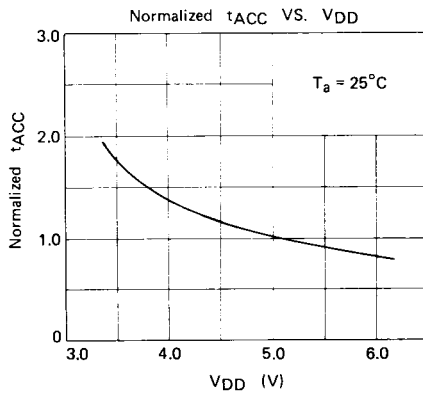
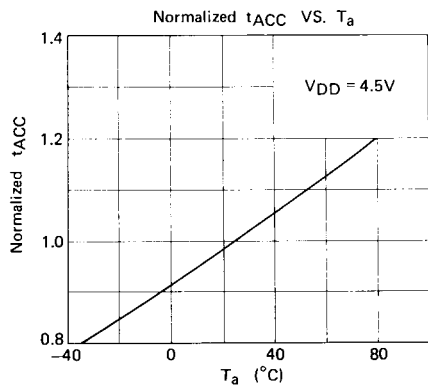


I_{OL} VS. T_a



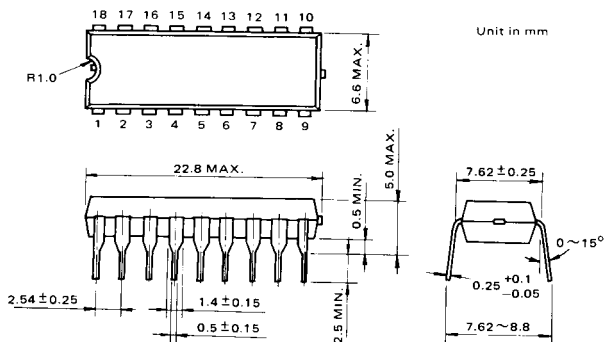
I_{OL} VS. V_{OL}



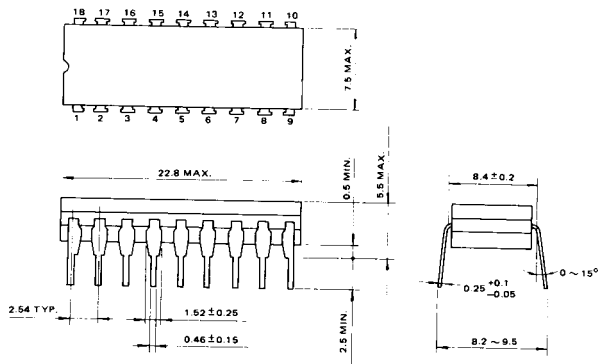


OUTLINE DRAWINGS

• PLASTIC PACKAGE



• Cerdip PACKAGE



Note: Each lead pitch is 2.54 mm. All leads are located within 0.25mm of their longitudinal position with respect to No. 1 and No. 18 leads.
All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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