

TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC55NEM208AFP/AFTN is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V $\pm$ 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz (typ) and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 1 μ A standby current (typ) when chip enable ($\overline{CE}$) is asserted high. There are two control inputs. $\overline{CE}$ is used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to 85°C , the TC55NEM208AFP/AFTN can be used in environments exhibiting extreme temperature conditions. The TC55NEM208AFP/AFTN is available in a standard plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 15 mW/MHz (typical)
- Single power supply voltage of 5 V $\pm$ 10%
- Power down features using $\overline{CE}$.
- Data retention supply voltage of 2.0 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C
- Standby Current (maximum): 20 μ A

- Access Times (maximum):

	TC55NEM208AFP/AFTN	
	55	70
Access Time	55 ns	70 ns
$\overline{CE}$ Access Time	55 ns	70 ns
$\overline{OE}$ Access Time	30 ns	35 ns

- Package:

SOP32-P-525-1.27 (AFP) (Weight: g typ)
TSOP II32-P-400-1.27 (AFTN) (Weight: g typ)

PIN ASSIGNMENT (TOP VIEW)

32 PIN SOP & TSOP

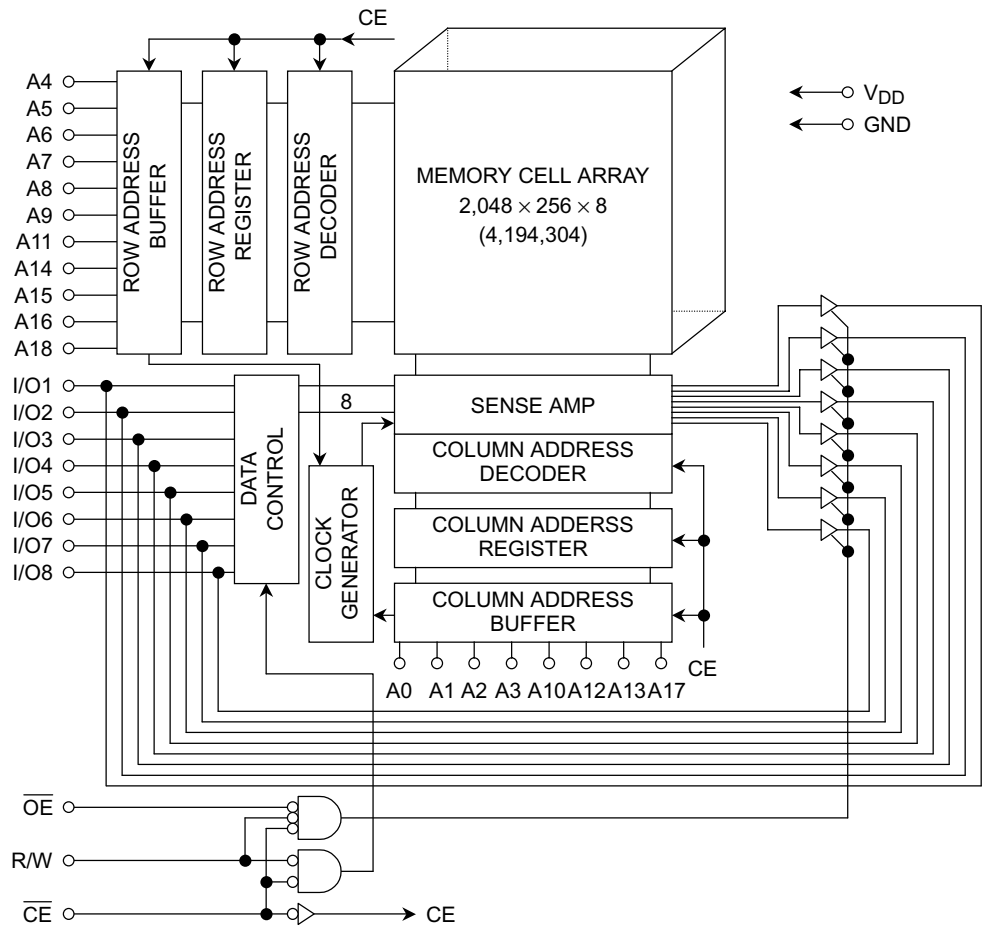
A18	1	32	V _{DD}
A16	2	31	A15
A14	3	30	A17
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$
A2	10	23	A10
A1	11	22	$\overline{CE}$
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

(AFP/AFTN)

PIN NAMES

A0~A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1~I/O8	Data Inputs/Outputs
V _{DD}	Power (+5 V)
GND	Ground

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	$I_{D DS}$

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	-0.3~7.0	V
V_{IN}	Input Voltage	-0.3*~7.0	V
$V_{I/O}$	Input/Output Voltage	-0.5~ $V_{DD} + 0.5$	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	-55~150	°C
T_{opr}	Operating Temperature	-40~85	°C

*: -2.0 V when measured at a pulse width of 20ns

DC RECOMMENDED OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	-0.3*	—	0.6	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

*: -2.0 V when measured at a pulse width of 20 ns

DC CHARACTERISTICS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 5\text{ V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V~V _{DD}			—	—	±1.0	μA
I _{OH}	Output High Current	V _{OH} = 2.4 V			−1.0	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V			2.1	—	—	mA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$, V _{OUT} = 0 V~V _{DD}			—	—	±1.0	μA
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ and R/W = V _{IH} , I _{OUT} = 0 mA, Other Input = V _{IH} /V _{IL}	t _{cycle}	MIN	—	—	35	mA
				1 μs	—	8	—	
I _{DDO2}		$\overline{CE} = 0.2\text{ V}$ and R/W = V _{DD} − 0.2 V, I _{OUT} = 0 mA, Other Input = V _{DD} − 0.2 V/0.2 V		MIN	—	—	30	mA
				1 μs	—	3	—	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$			—	—	3	mA
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{ V}$, V _{DD} = 2.0 V~5.5 V	Ta = 25°C		—	1	—	μA
			Ta = −40~40°C		—	—	3	
			Ta = −40~85°C		—	—	20	

CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 5\text{ V} \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55NEM208AFPN/AFTN				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	55	—	70	—	ns
t _{ACC}	Address Access Time	—	55	—	70	
t _{CO}	Chip Enable Access Time	—	55	—	70	
t _{OE}	Output Enable Access Time	—	30	—	35	
t _{COE}	Chip Enable Low to Output Active	5	—	5	—	
t _{OEE}	Output Enable Low to Output Active	0	—	0	—	
t _{OD}	Chip Enable High to Output High-Z	—	25	—	30	
t _{ODO}	Output Enable High to Output High-Z	—	25	—	30	
t _{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

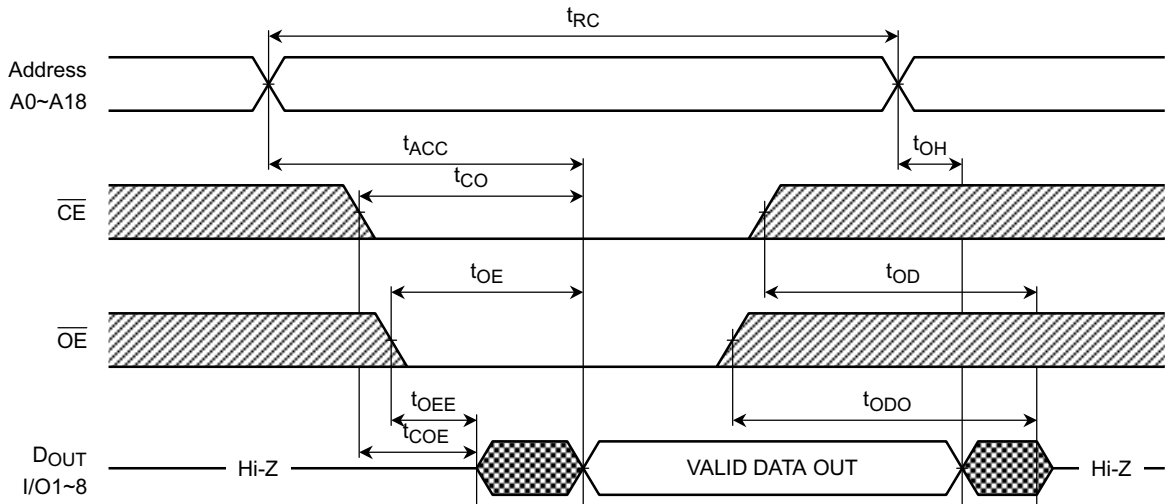
SYMBOL	PARAMETER	TC55NEM208AFPN/AFTN				UNIT
		55		70		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	55	—	70	—	ns
t _{WP}	Write Pulse Width	40	—	50	—	
t _{CW}	Chip Enable to End of Write	45	—	55	—	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	
t _{ODW}	R/W Low to Output High-Z	—	25	—	30	
t _{OEW}	R/W High to Output Active	0	—	0	—	
t _{DS}	Data Setup Time	25	—	30	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC TEST CONDITIONS

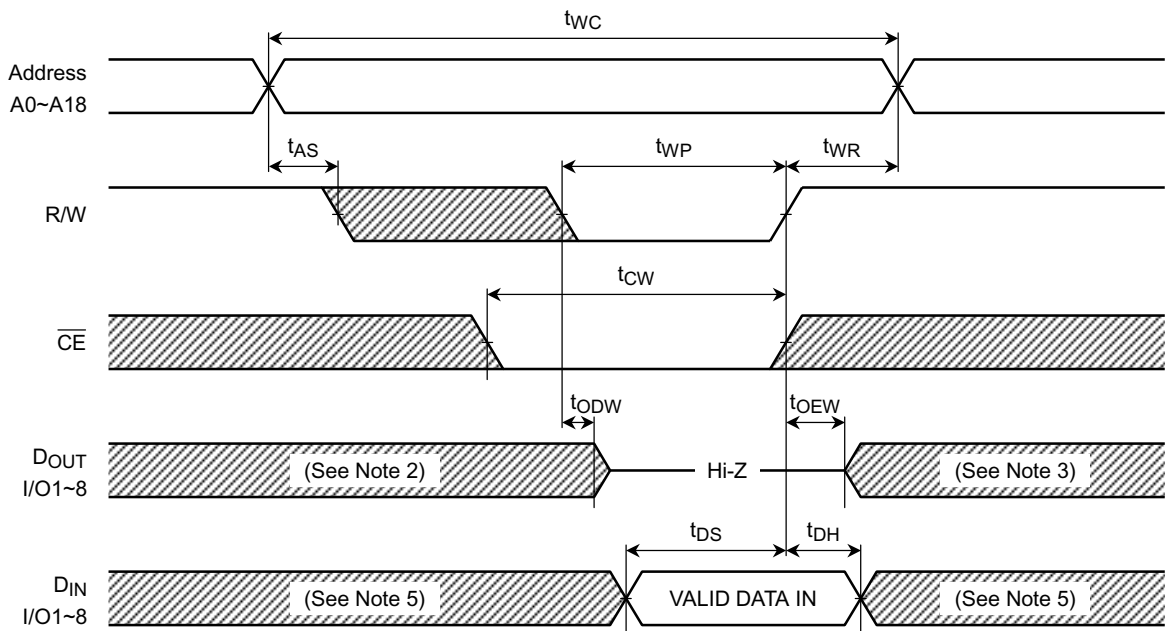
PARAMETER	TEST CONDITION
Output load	100 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.4 V
Timing measurements	1.5 V
Reference level	1.5 V
t_R , t_F	5 ns

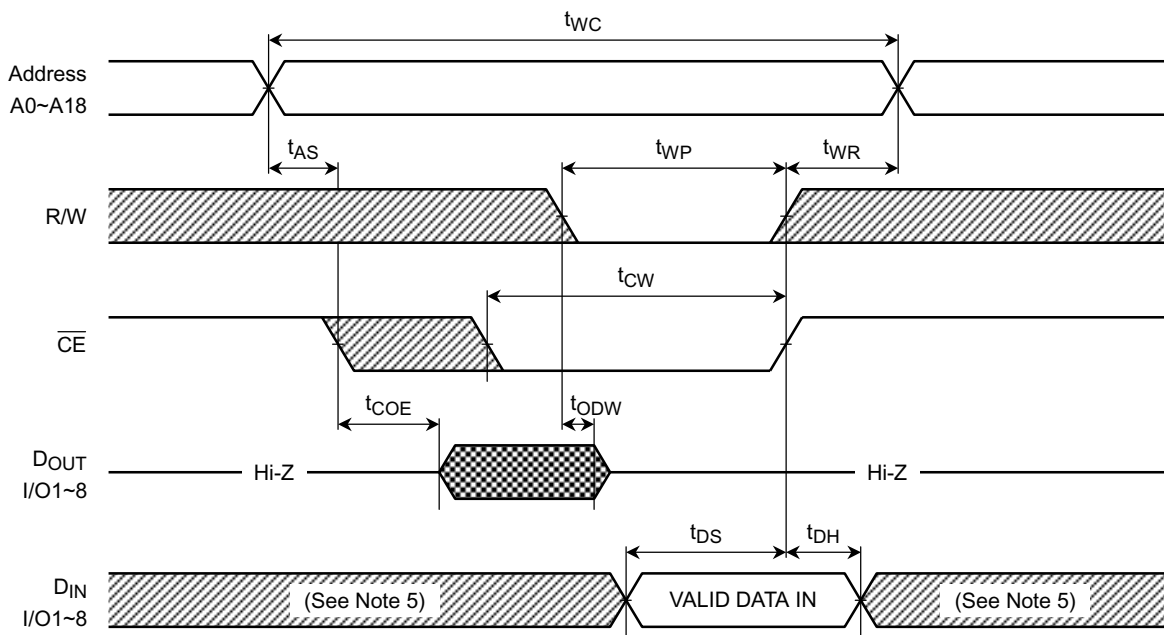
TIMING DIAGRAMS

READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 4)


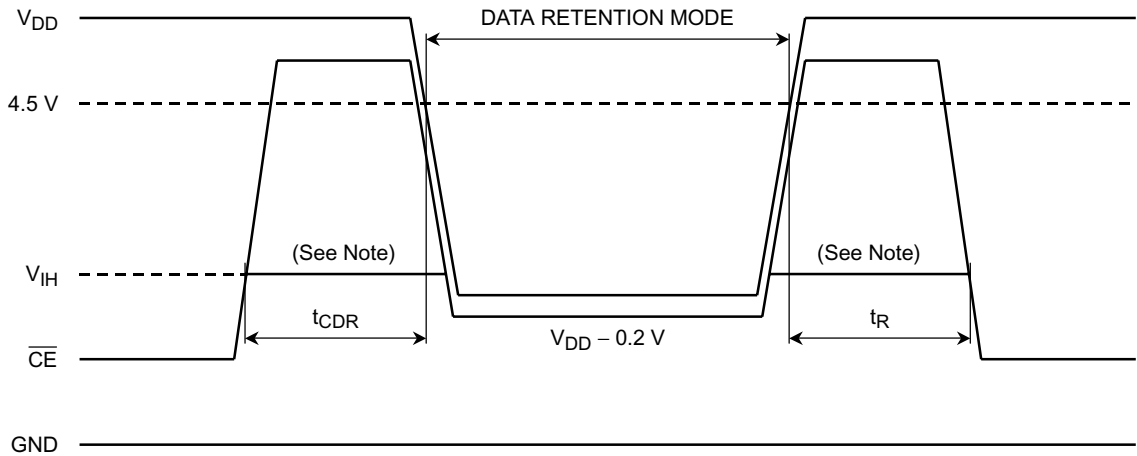
Note:

- (1) R/W remains HIGH for the read cycle.
- (2) If $\overline{\text{CE}}$ goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If $\overline{\text{CE}}$ goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I _{DDS2}	Standby Current	Ta = -40~40°C	—	—	3	μA
		Ta = -40~85°C	—	—	20	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns
t _R	Recovery Time		5	—	—	ms

CE CONTROLLED DATA RETENTION MODE

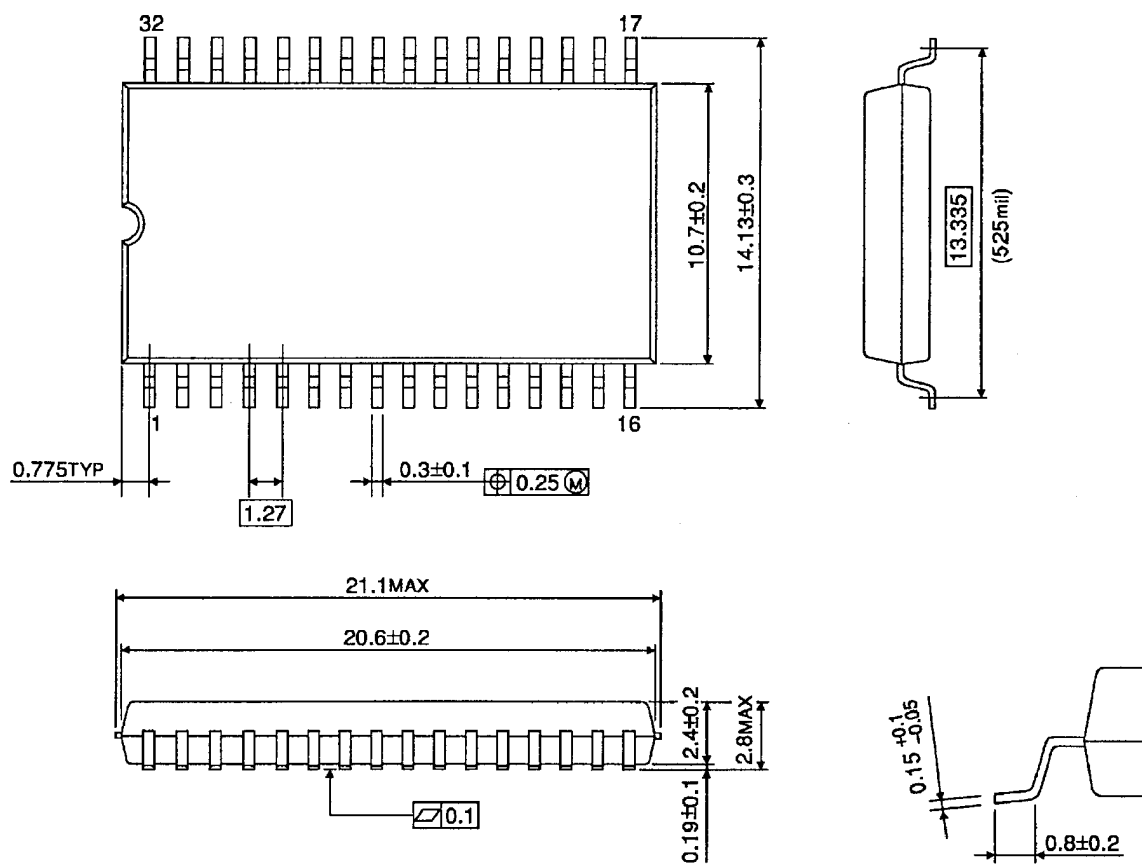


Note: When $\overline{CE}$ is operating at the V_{IH} level (2.2V), the standby current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.4V.

PACKAGE DIMENSIONS

SOP32-P-525-1.27

Unit : mm

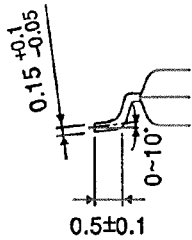
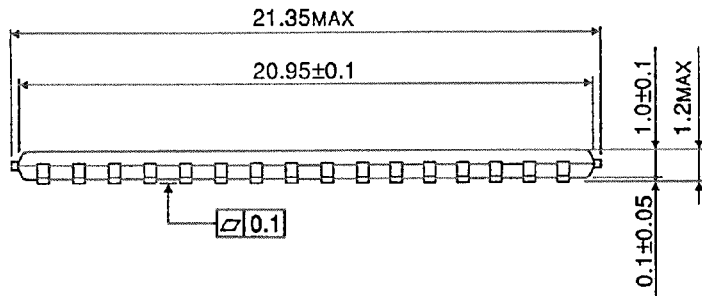
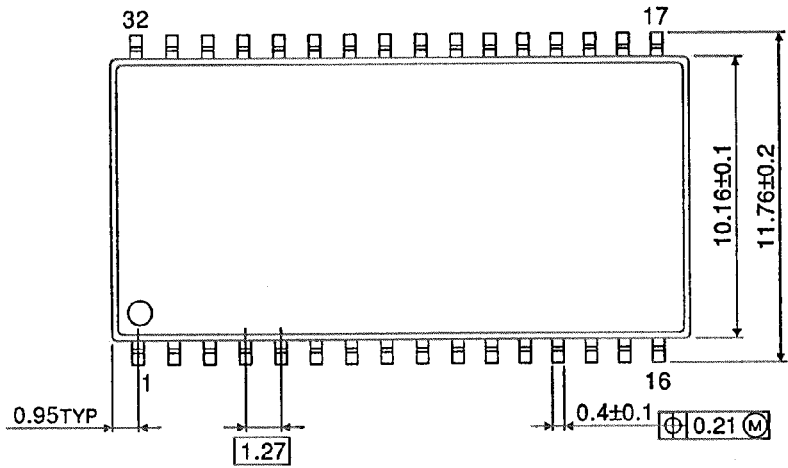


Weight: g (typ)

PACKAGE DIMENSIONS

TSOPII32-P-400-1.27

Unit: mm



Weight: g (typ)

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