

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

131,072-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC55V1001F/FT/TR/ST/SR is a 1,048,576-bit static random access memory (SRAM) organized as 131,072 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.7 to 3.6 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz (typ) and a minimum cycle time of 85 ns. It is automatically placed in low-power mode at 0.5 μ A standby current (typ) when chip enable ($\overline{\text{CE1}}$) is asserted high or ($\overline{\text{CE2}}$) is asserted low. There are three control inputs. $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are used to select the device and for data retention control, and output enable ($\overline{\text{OE}}$) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55V1001F/FT/TR/ST/SR is available in a plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 10.8 mW/MHz (typical)
- Standby current of 0.9 μ A (maximum) at
 $T_a = 25^\circ\text{C}$
- Single power supply voltage of 2.7 to 3.6 V
- Power down features using $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$.
- Data retention supply voltage of 2 to 3.6 V
- Direct TTL compatibility for all inputs and outputs

• Access Times (maximum):

	2.7 to 3.6 V	
	-85L	-10L
Access Time	85 ns	100 ns
$\overline{\text{CE1}}$ Access Time	85 ns	100 ns
$\overline{\text{CE2}}$ Access Time	85 ns	100 ns
$\overline{\text{OE}}$ Access Time	45 ns	50 ns

• Packages:

SOP32-P-525-1.27 (F)	(Weight: 1.04 g typ)
TSOP I 32-P-0820-0.50 (FT)	(Weight: 0.34 g typ)
TSOP I 32-P-0820-0.50A (TR)	(Weight: 0.34 g typ)
TSOP I 32-P-0.50 (ST)	(Weight: 0.24 g typ)
TSOP I 32-P-0.50A (SR)	(Weight: 0.24 g typ)

PIN ASSIGNMENT (TOP VIEW)

○ 32 PIN SOP

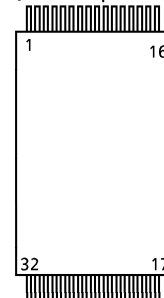
NC	1	32	V_{DD}
A16	2	31	A15
A14	3	30	$\overline{\text{CE2}}$
A12	4	29	R/W
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{\text{OE}}$
A2	10	23	A10
A1	11	22	$\overline{\text{CE1}}$
A0	12	21	I/O8
I/O1	13	20	I/O7
I/O2	14	19	I/O6
I/O3	15	18	I/O5
GND	16	17	I/O4

○ 32 PIN TSOP

(Normal pinout)



(Reverse pinout)



PIN NAMES

A0 to A16	Address Inputs
R/W	Read/Write Control
$\overline{\text{OE}}$	Output Enable
$\overline{\text{CE1}}$, $\overline{\text{CE2}}$	Chip Enable
I/O1 to I/O8	Data Input/Output
V_{DD}	Power
GND	Ground
NC	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A ₁₁	A ₉	A ₈	A ₁₃	R/W	$\overline{\text{CE2}}$	A ₁₅	V_{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{\text{CE1}}$	A ₁₀	$\overline{\text{OE}}$

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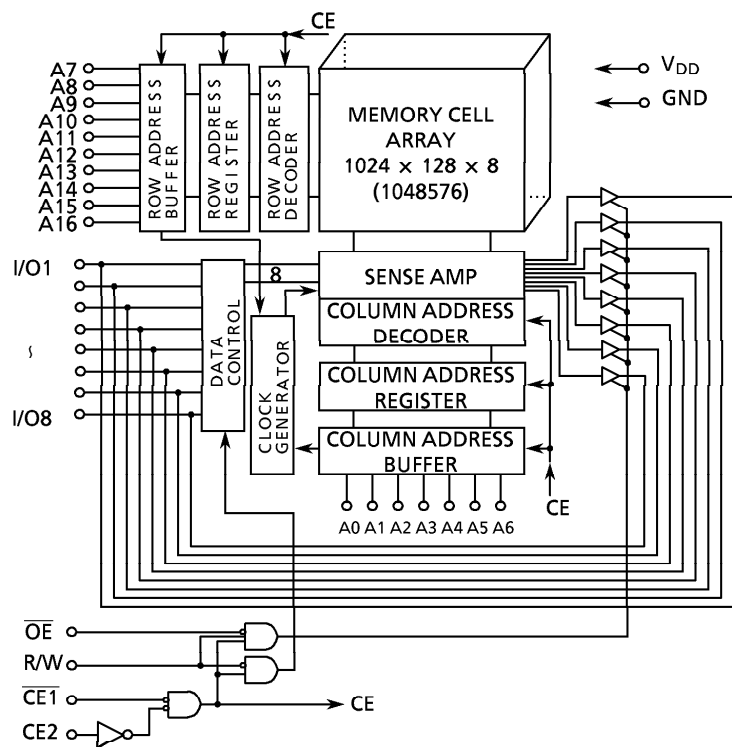
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BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 to I/O8	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	x	L	D _{IN}	I _{DDO}
Outputs Disabled	L	H	H	H	High-Z	I _{DDO}
Standby	H	x	x	x	High-Z	I _{DDS}
	x	L	x	x	High-Z	I _{DDS}

Note: x = don't care. H = logic high. L = logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 4.6	V
V _{IN}	Input Voltage	- 0.3* to 4.6	V
V _{I/O}	Input/Output Voltage	- 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.8	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg.}	Storage Temperature	- 55 to 150	°C
T _{opr.}	Operating Temperature	0 to 70	°C

* - 3.0 V when measured at a pulse width of 50 ns

** SOP

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	2.7 to 3.6 V			UNIT
		MIN	TYP	MAX	
V _{DD}	Power Supply Voltage	2.7	–	3.6	V
V _{IH}	Input High Voltage	2.0	–	V _{DD} + 0.3	
V _{IL}	Input Low Voltage	– 0.3*	–	0.8	
V _{DH}	Data Retention Supply Voltage	2.0	–	3.6	

* – 3.0 V when measured at a pulse width of 50 ns

DC CHARACTERISTICS (Ta = 0° to 70°C, V_{DD} = 2.7 to 3.6 V)

SYMBOL	PARAMETER	TEST CONDITION					MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}					–	–	± 1.0	μA
I _{OH}	Output High Current	V _{OH} = V _{DD} – 0.5 V					– 0.5	–	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.4 V					2.1	–	–	mA
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 V to V _{DD}					–	–	± 1.0	μA
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0 mA Other Input = V _{IH} /V _{IL}	V _{DD} = 3 V ± 10%	T _{cycle}	min	–	–	35	mA	
					1 μs	–	–	10		
			V _{DD} = 3.3 V ± 0.3 V	T _{cycle}	min	–	–	40		
					1 μs	–	–	12		
I _{DDO2}		CE1 = 0.2 V and CE2 = V _{DD} – 0.2 V R/W = V _{DD} – 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} – 0.2 V/0.2 V	V _{DD} = 3 V ± 10%	T _{cycle}	min	–	–	30		
					1 μs	–	–	5		
			V _{DD} = 3.3 V ± 0.3 V	T _{cycle}	min	–	–	35		
					1 μs	–	–	6		
I _{DDS1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL}					–	–	2	mA
I _{DDS2} (Note)		CE1 = V _{DD} – 0.2 V or CE2 = 0.2 V V _{DD} = 2.0 to 3.6 V	V _{DD} = 3 V ± 10%	Ta = 25°C		–	0.5	0.7	μA	
				Ta = 0° to 70°C		–	–	15		
			V _{DD} = 3.3 V ± 0.3 V	Ta = 25°C		–	0.7	0.9		
				Ta = 0° to 70°C		–	–	20		
			V _{DD} = 3.0 V	Ta = 25°C		–	–	0.5		
				Ta = 0° to 40°C		–	–	2		
				Ta = 0° to 70°C		–	–	10		

Note: In standby mode with $\overline{CE1} \geq V_{DD} - 0.2$ V, these limits are assured for the condition CE2 $\geq V_{DD} - 0.2$ V or CE2 ≤ 0.2 V.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = 0^\circ \text{ to } 70^\circ\text{C}$, $V_{DD} = 2.7 \text{ to } 3.6 \text{ V}$)

READ CYCLE

SYMBOL	PARAMETER	TC55V1001F/FT/TR/ST/SR				UNIT
		-85L		-10L		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	85	–	100	–	ns
t _{ACC}	Address Access Time	–	85	–	100	
t _{CO1}	Chip Enable (CE1) Access Time	–	85	–	100	
t _{CO2}	Chip Enable (CE2) Access Time	–	85	–	100	
t _{OE}	Output Enable Access Time	–	45	–	50	
t _{COE}	Chip Enable Low to Output Active	10	–	10	–	
t _{OEE}	Output Enable Low to Output Active	5	–	5	–	
t _{OD}	Chip Enable High to Output High-Z	–	30	–	35	
t _{ODO}	Output Enable High to Output High-Z	–	30	–	35	
t _{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V1001F/FT/TR/ST/SR				UNIT
		-85L		-10L		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	85	–	100	–	ns
t _{WP}	Write Pulse Width	60	–	60	–	
t _{CW}	Chip Enable to End of Write	75	–	80	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W Low to Output High-Z	–	30	–	35	
t _{OEW}	R/W High to Output Active	5	–	5	–	
t _{DS}	Data Setup Time	35	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

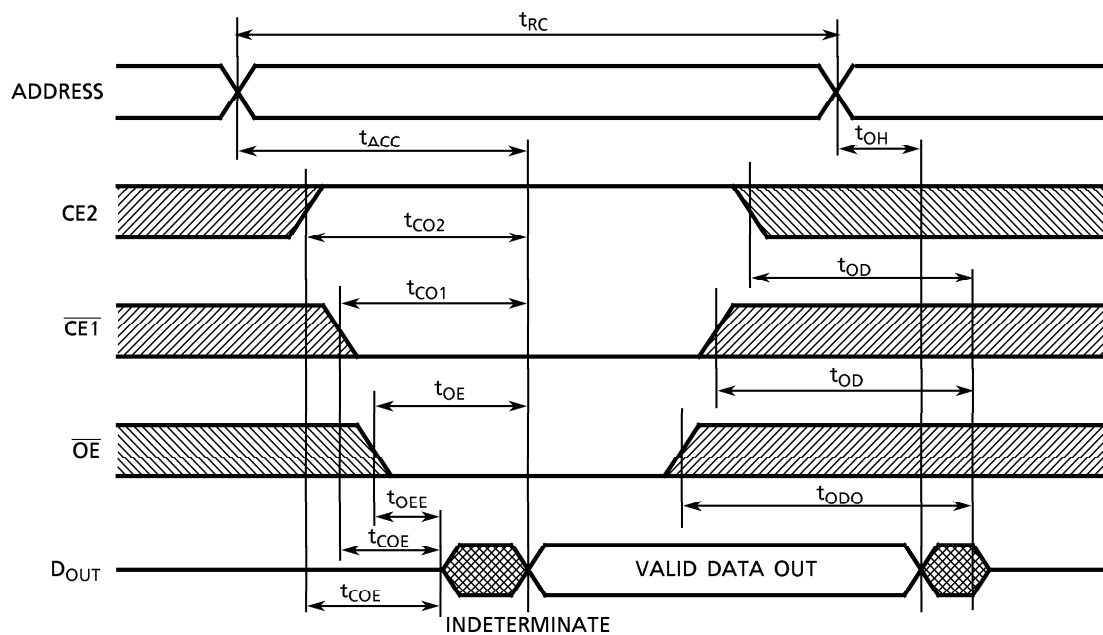
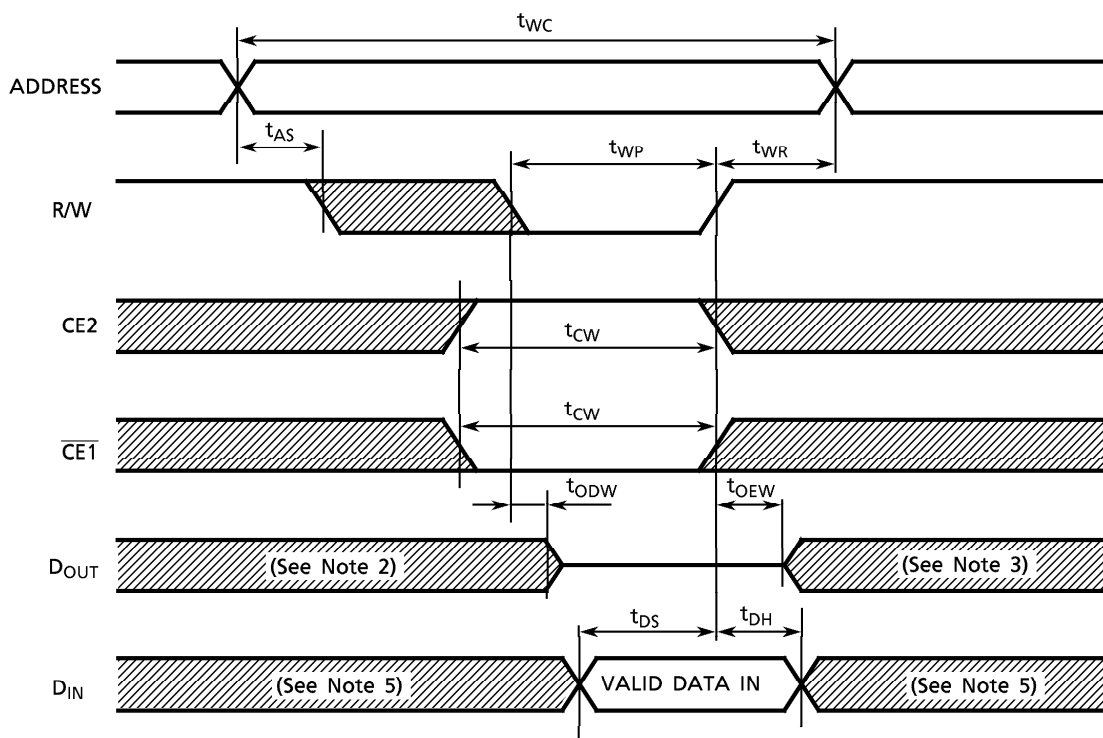
Output load: 100 pF + one TTL gate

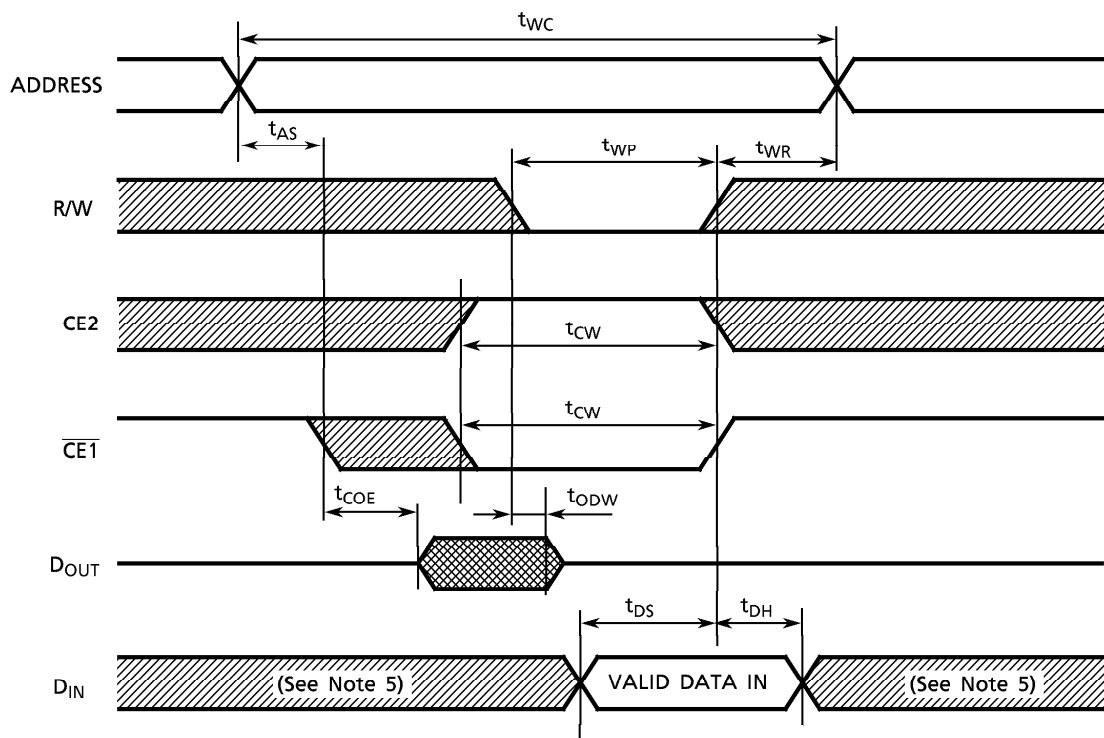
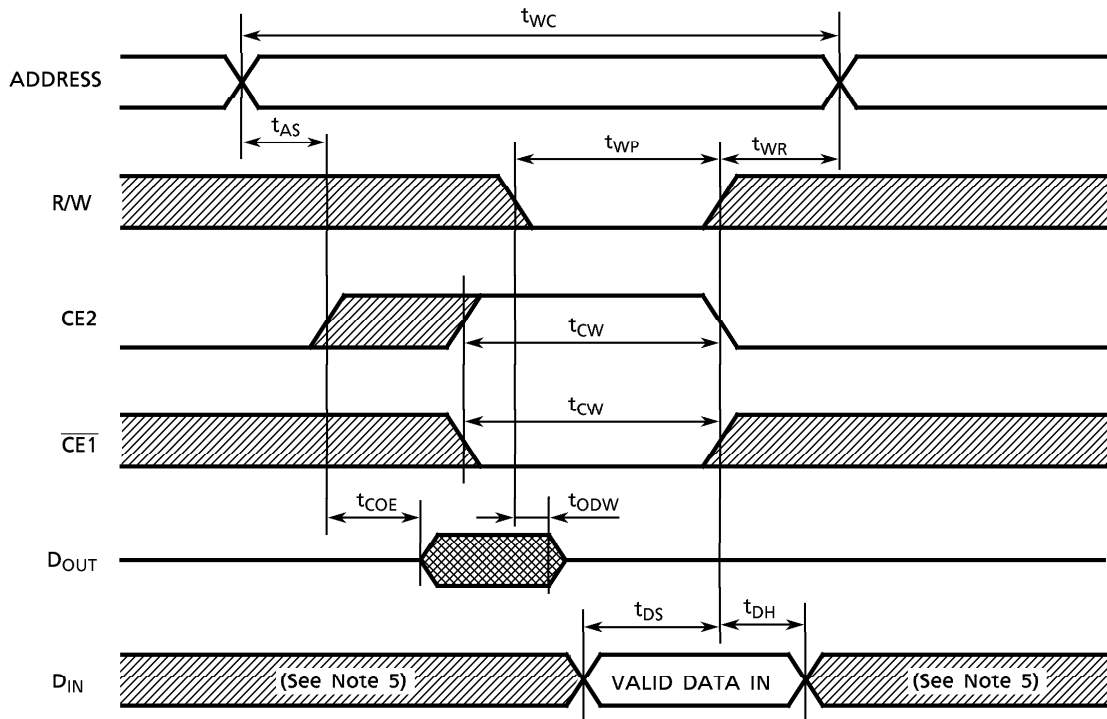
Input pulse level: 0.6 V, 2.2 V

Timing measurements: 1.5 V

Reference level: 1.5 V

t_R, t_F : 5 ns

TIMING DIAGRAMSREAD CYCLE (See Note 1)WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)

WRITE CYCLE 2 ($\overline{\text{CE1}}$ CONTROLLED) (See Note 4)WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)

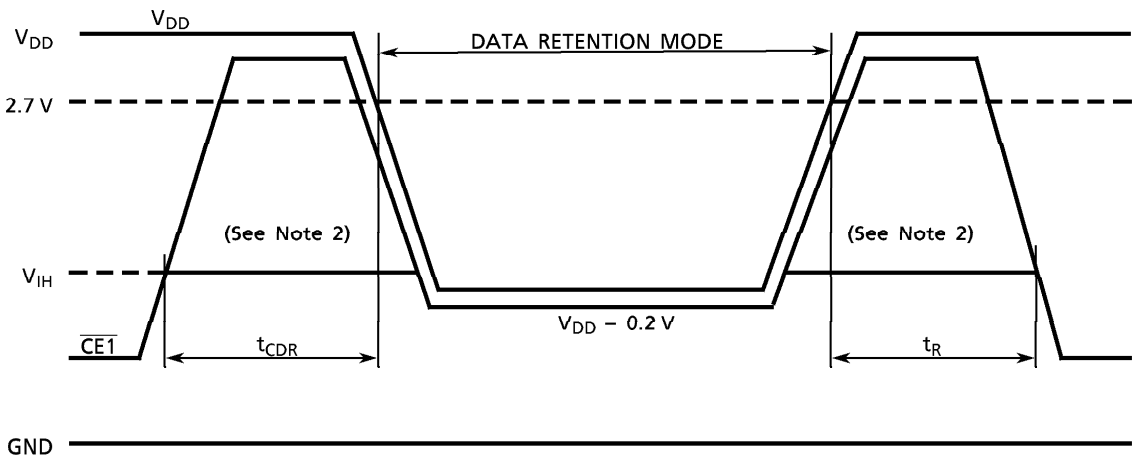
- Note: (1) R/W remains HIGH for the read cycle.
- (2) If $\overline{\text{CE1}}$ goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If $\overline{\text{CE1}}$ goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

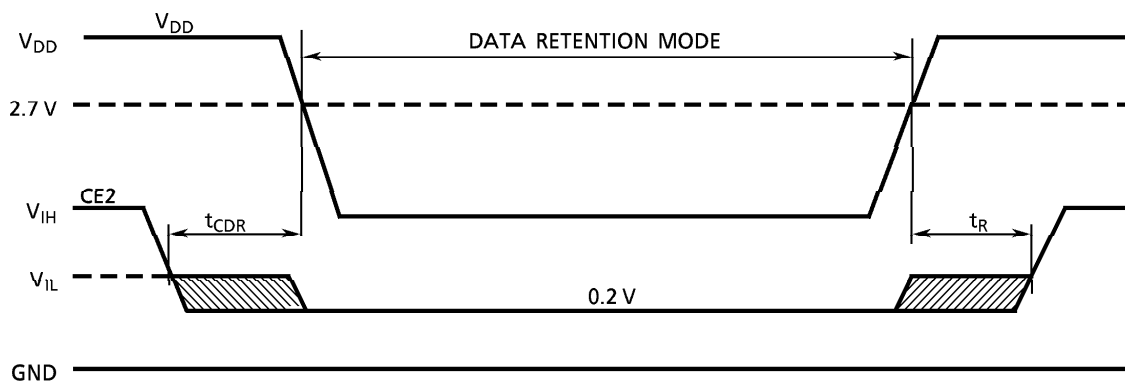
DATA RETENTION CHARACTERISTICS (Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage		2.0	–	3.6	V
I _{DDS2}	Standby Current	V _{DH} = 3.0 V	–	–	10*	μA
		V _{DH} = 3.6 V	–	–	20	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	–	–	nS
t _R	Recovery Time		5	–	–	mS

* 2 μA (max) at Ta = 0° to 40°C

$\overline{\text{CE1}}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)

Note: (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when

$$CE2 \leq 0.2 \text{ V or } CE2 \geq V_{DD} - 0.2 \text{ V.}$$

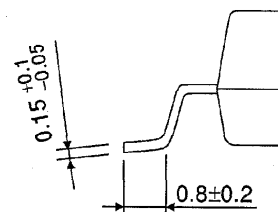
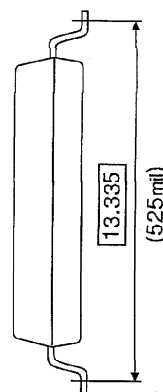
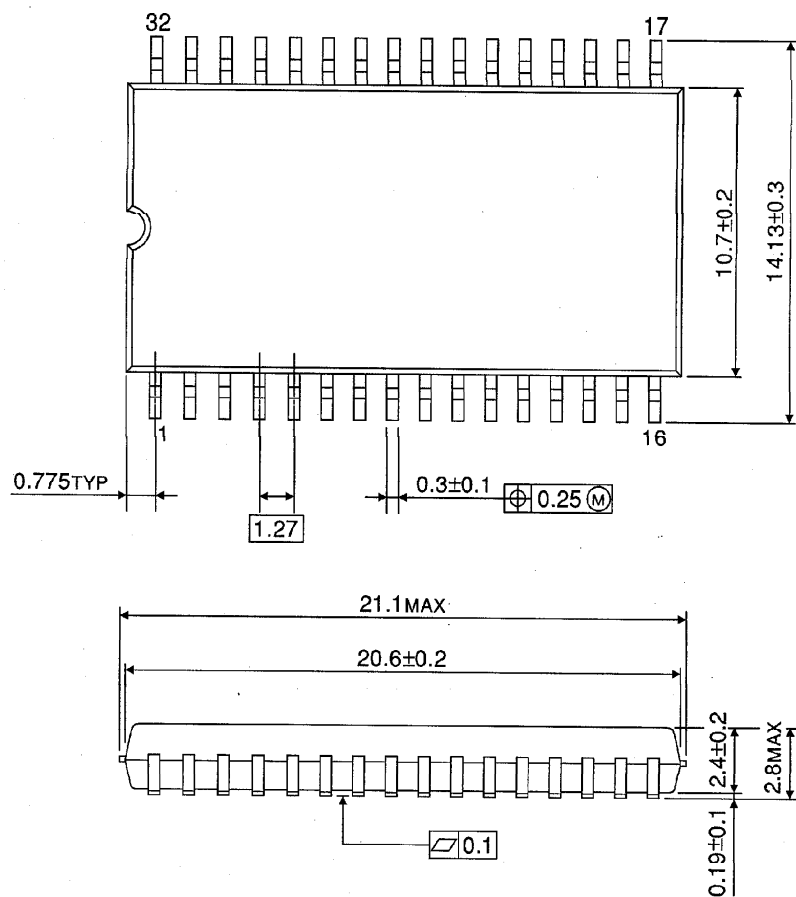
(2) When $\overline{CE1}$ is operating at the V_{IH} level (2 V), the operating current is given by I_{DDs1} during the transition of V_{DD} from 3.6 to 2.2 V.

(3) In $CE2$ controlled data retention mode, minimum standby current mode is entered when

$$CE2 \leq 0.2 \text{ V.}$$

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

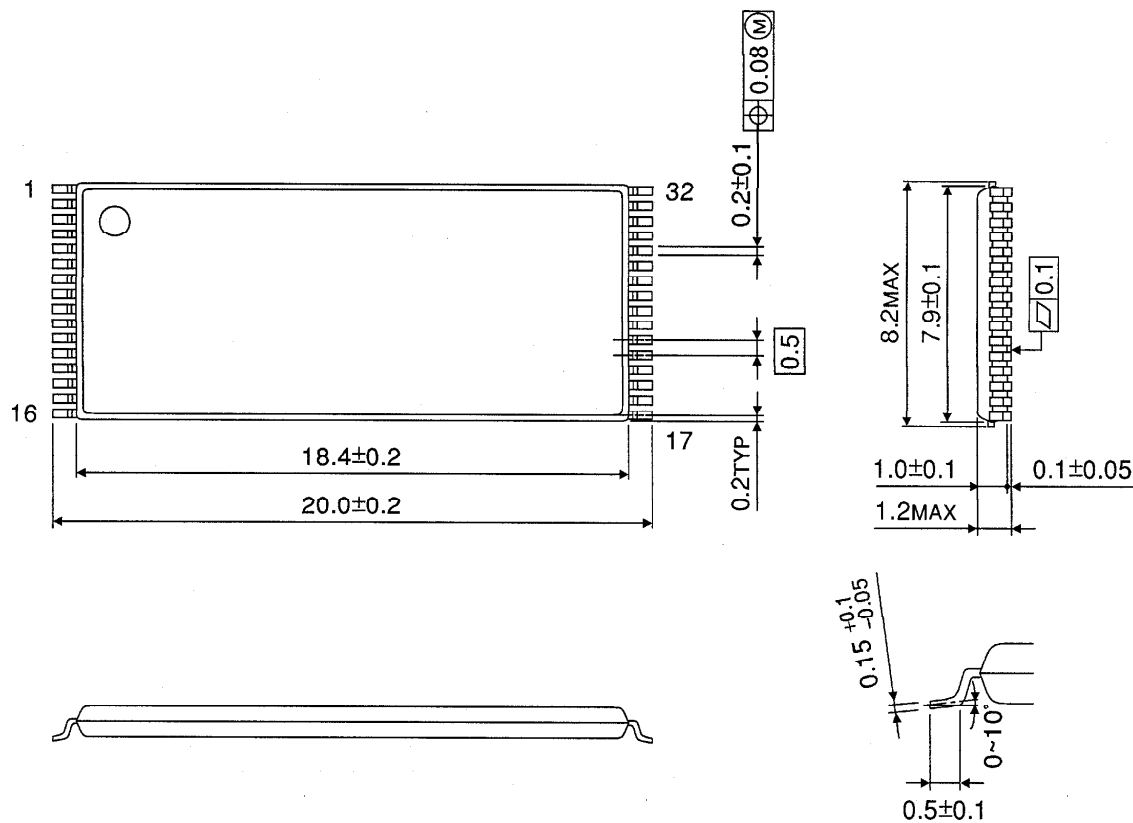
Units in mm



Weight: 1.04 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50)

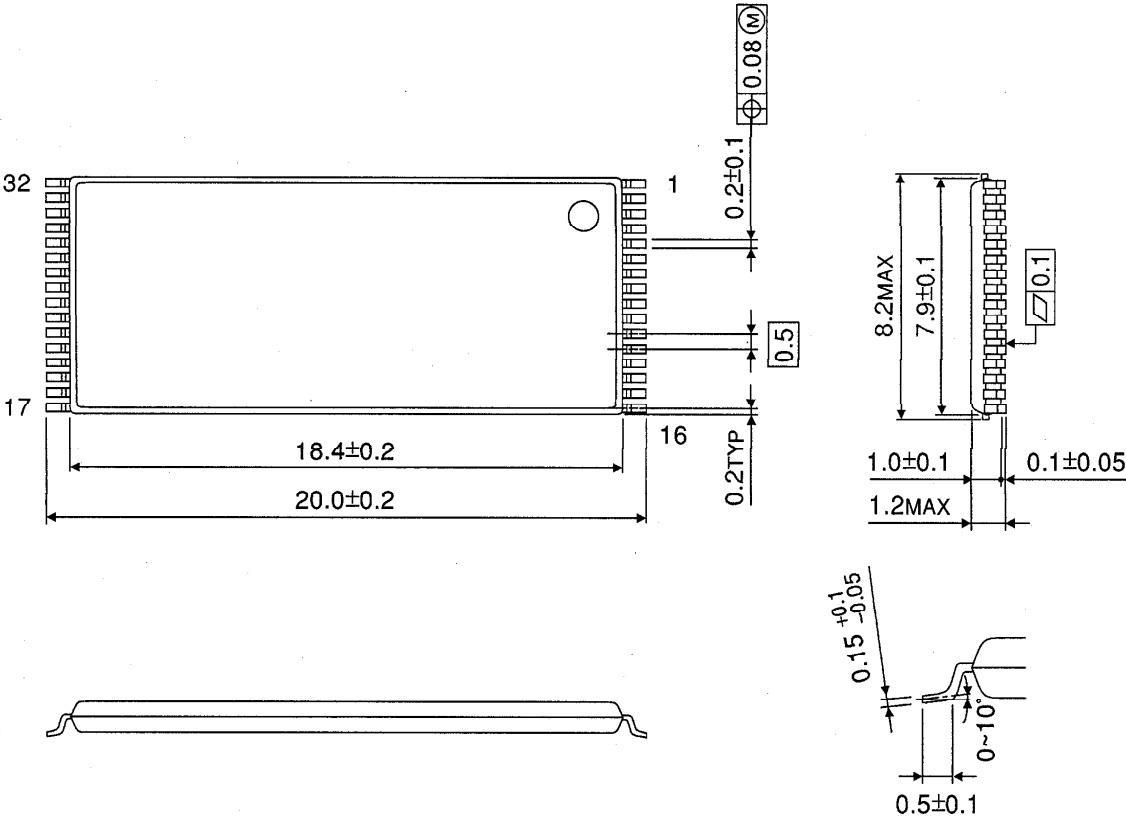
Units in mm



Weight: 0.34 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50A)

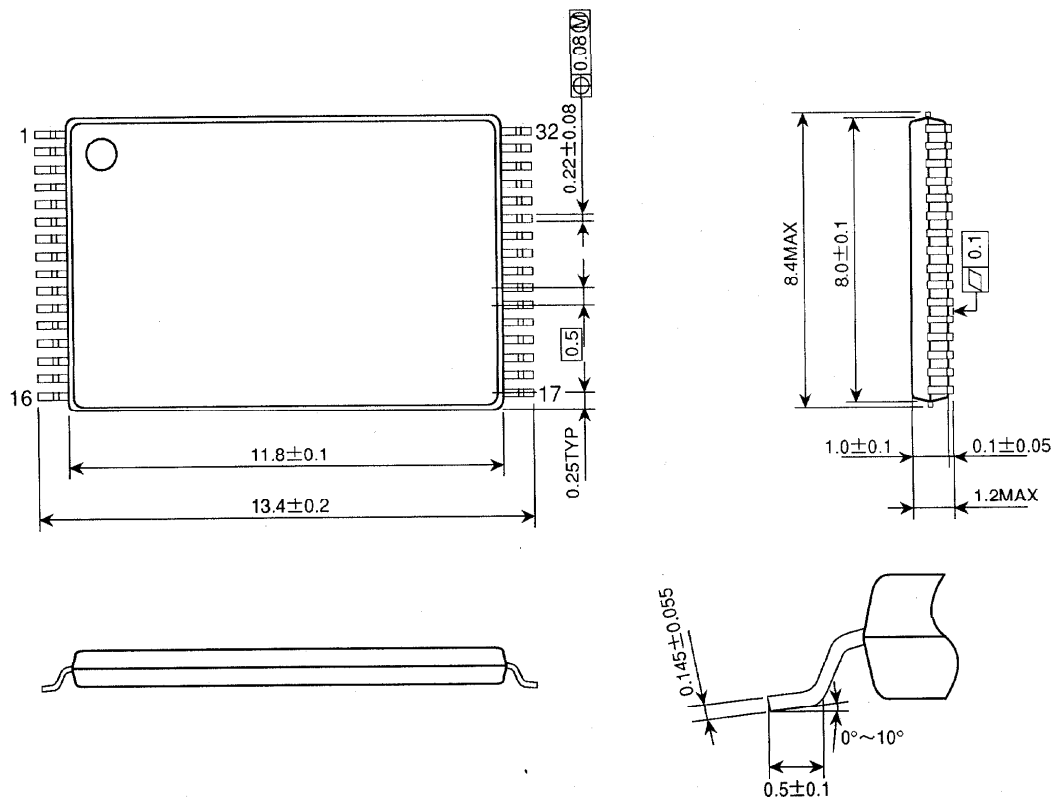
Units in mm



Weight: 0.34 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0.50)

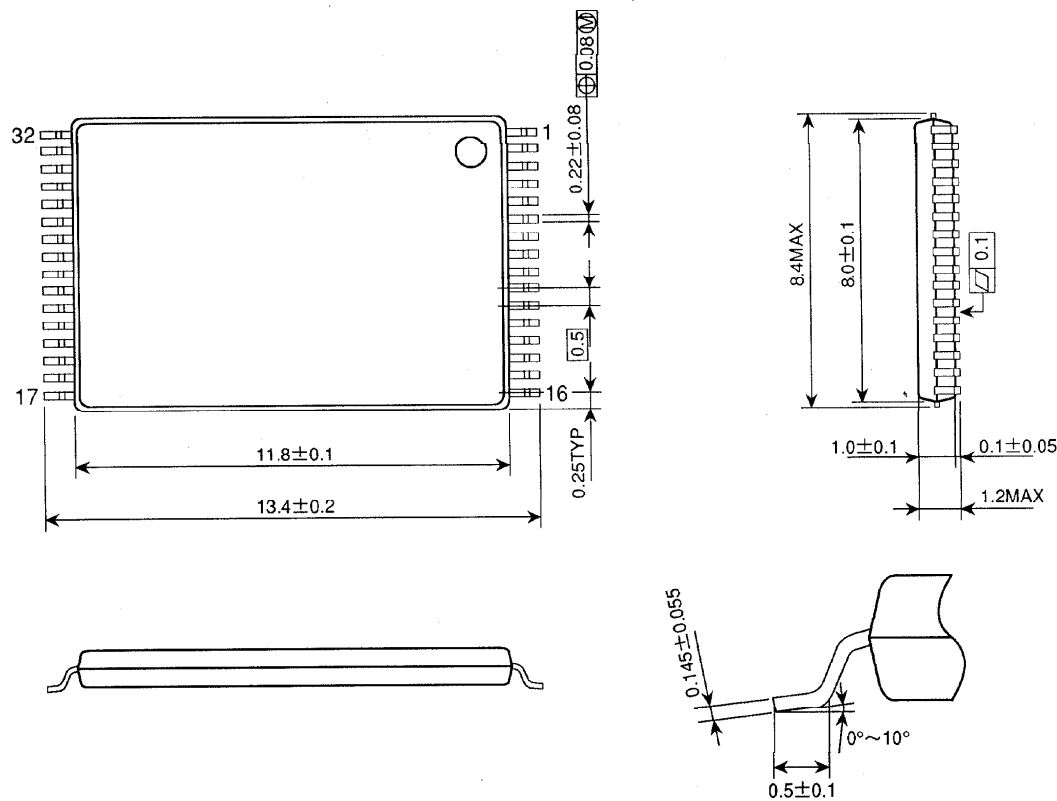
Units in mm



Weight: 0.24 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0.50A)

Units in mm



Weight: 0.24 g (typ)