

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

262,144-WORD BY 16-BIT CMOS STATIC RAM

DESCRIPTION

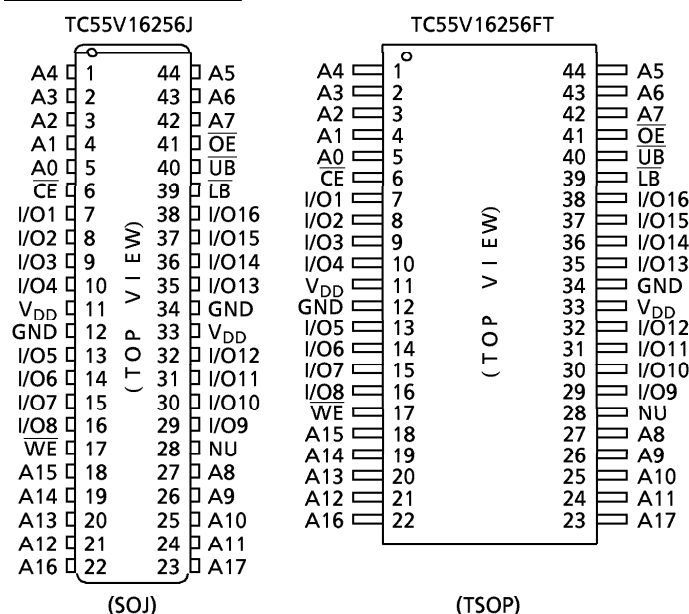
The TC55V16256J/FT is a 4,194,304-bit high-speed static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable ($\overline{CE}$) can be used to place the device in a low-power mode, and output enable ($\overline{OE}$) provides fast memory access. Data byte control signals ($\overline{LB}$, $\overline{UB}$) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55V16256J/FT is available in plastic 44-pin SOJ and TSOP with 400mil width for high density surface assembly.

FEATURES

- Fast access time (the following are maximum values)
 - TC55V16256J/FT-12: 12 ns
 - TC55V16256J/FT-15: 15 ns
- Low-power dissipation (the following are maximum values)

Cycle Time	12	15	20	25	ns
Operation (max)	200	190	160	140	mA

 Standby: 4 mA (both devices)
- Single power supply voltage of $3.3V \pm 0.3V$
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using $\overline{OE}$
- Data byte control using $\overline{LB}$ (I/O1 to I/O8) and $\overline{UB}$ (I/O9 to I/O16)
- Package:
 - SOJ44-P-400-1.27 (J) (Weight: 1.64g typ)
 - TSOP 44-P-400-0.80 (FT) (Weight: 0.45g typ)

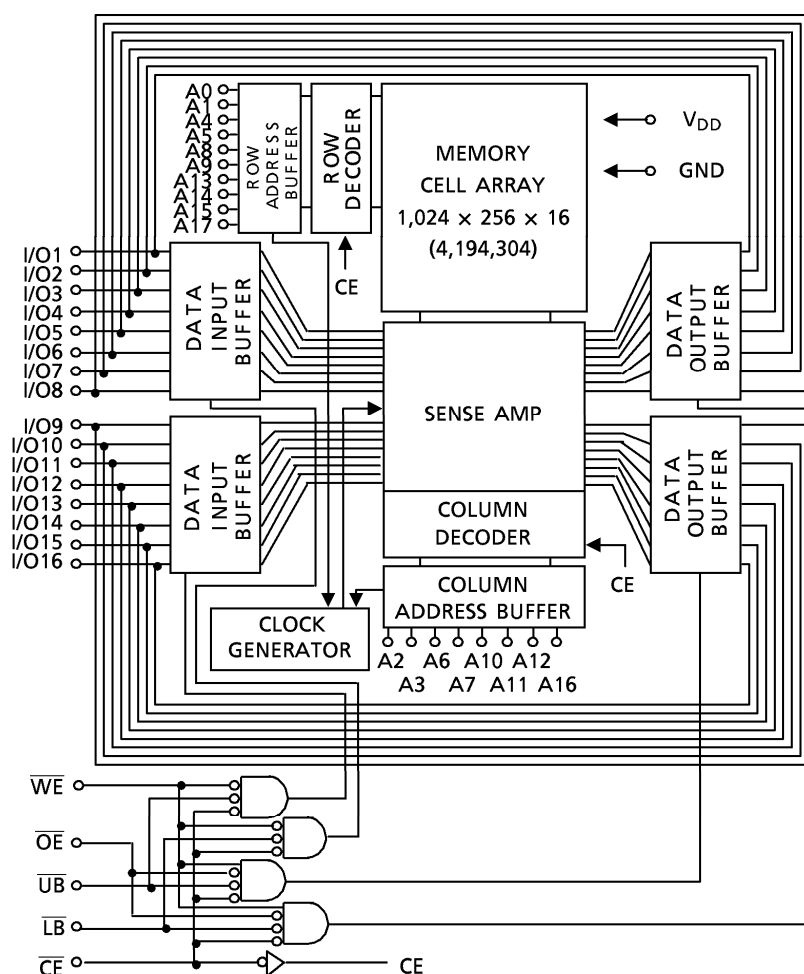
PIN ASSIGNMENT**PIN NAMES**

A0 to A17	Address Inputs
I/O1 to I/O16	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power (+ 3.3V)
GND	Ground
NU	Not Usable (Input)

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BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	- 0.5 to 4.6	V
V_{IN}	Input Terminal Voltage	- 0.5* to 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	- 0.5* to $V_{DD} + 0.5^{**}$	V
P_D	Power Dissipation	1.4	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	- 65 to 150	°C
T_{opr}	Operating Temperature	- 10 to 85	°C

* : -1.5V with a pulse width of 20% · t_{RC} min (4ns max)

** : $V_{DD} + 1.5V$ with a pulse width of 20% · t_{RC} min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS ($T_a = 0^\circ$ to $70^\circ C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	$V_{DD} + 0.3^{**}$	V
V_{IL}	Input Low Voltage	- 0.3*	-	0.8	V

* : -1.0V with a pulse width of 20% · t_{RC} min (4ns max)

** : $V_{DD} + 1.0V$ with a pulse width of 20% · t_{RC} min (4ns max)

DC CHARACTERISTICS ($T_a = 0^\circ \text{ to } 70^\circ \text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current (Except NU pin)	V _{IN} = 0 to V _{DD}		− 1	−	1	μA
I _{LO}	Output Leakage Current	CE = V _{IH} or WE = V _{IL} or OE = V _{IH} V _{OUT} = 0 to V _{DD}		− 1	−	1	μA
I _{I(NU)}	Input Current (NU pin)	V _{IN} = 0 to 0.8V		− 1	−	20	μA
		V _{IN} = 0 to 0.2V		− 1	−	1	
V _{OH}	Output High Voltage	I _{OH} = − 2mA		2.4	−	−	V
		I _{OH} = − 100μA		V _{DD} − 0.2	−	−	
V _{OL}	Output Low Voltage	I _{OL} = 2mA		−	−	0.4	
		I _{OL} = 100μA		−	−	0.2	
I _{DDO}	Operating Current	CE = V _{IL} , I _{out} = 0mA OE = V _{IH} Other Inputs = V _{IH} / V _{IL}	tcycle = 12ns	−	−	200	mA
			tcycle = 15ns	−	−	190	
			tcycle = 20ns	−	−	160	
			tcycle = 25ns	−	−	140	
I _{DDS 1}	Standby Current	CE = V _{IH} , Other Inputs = V _{IH} or V _{IL}		−	−	50	mA
I _{DDS 2}		CE = V _{DD} − 0.2V Other Inputs = V _{DD} − 0.2V or 0.2V		−	−	4	

CAPACITANCE ($T_a = 25^\circ \text{C}$, $f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	x	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Outputs Disable	L	H	H	x	x	High Impedance	High Impedance	I_{DDO}
	L	x	x	H	H			
Standby	H	x	x	x	x	High Impedance	High Impedance	I_{DD5}

x: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V.
You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS ($T_a = 0^\circ \text{ to } 70^\circ \text{C}$ (Note 1), $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)**READ CYCLE**

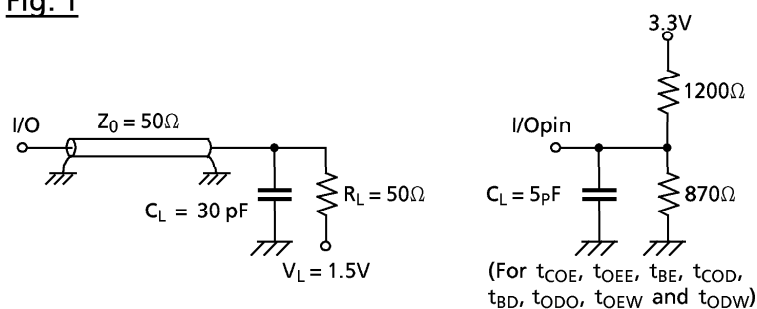
SYMBOL	PARAMETER	TC55V16256J/FT-12		TC55V16256J/FT-15		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	12	–	15	–	ns
t_{ACC}	Address Access Time	–	12	–	15	
t_{CO}	Chip Enable Access Time	–	12	–	15	
t_{OE}	Output Enable Access Time	–	6	–	8	
t_{BA}	Upper Byte, Lower Byte Access Time	–	6	–	8	
t_{OH}	Output Data Hold Time from Address Change	3	–	4	–	
t_{COE}	Output Enable Time from Chip Enable	3	–	4	–	
t_{OEE}	Output Enable Time from Output Enable	1	–	1	–	
t_{BE}	Output Enable Time from Upper Byte, Lower Byte	1	–	1	–	
t_{COD}	Output Disable Time from Chip Enable	–	7	–	8	
t_{ODO}	Output Disable Time from Output Enable	–	7	–	8	
t_{BD}	Output Disable Time from Upper Byte, Lower Byte	–	7	–	8	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V16256J/FT-12		TC55V16256J/FT-15		UNIT
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	12	–	15	–	ns
t_{WP}	Write Pulse Width	8	–	9	–	
t_{CW}	Chip Enable to End of Write	10	–	12	–	
t_{BW}	Upper Byte, Lower Byte Enable to End of Write	10	–	12	–	
t_{AW}	Address Valid to End of Write	10	–	12	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	7	–	8	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEw}	Output Enable Time from Write Enable	1	–	1	–	
t_{ODw}	Output Disable Time from Write Enable	–	7	–	8	

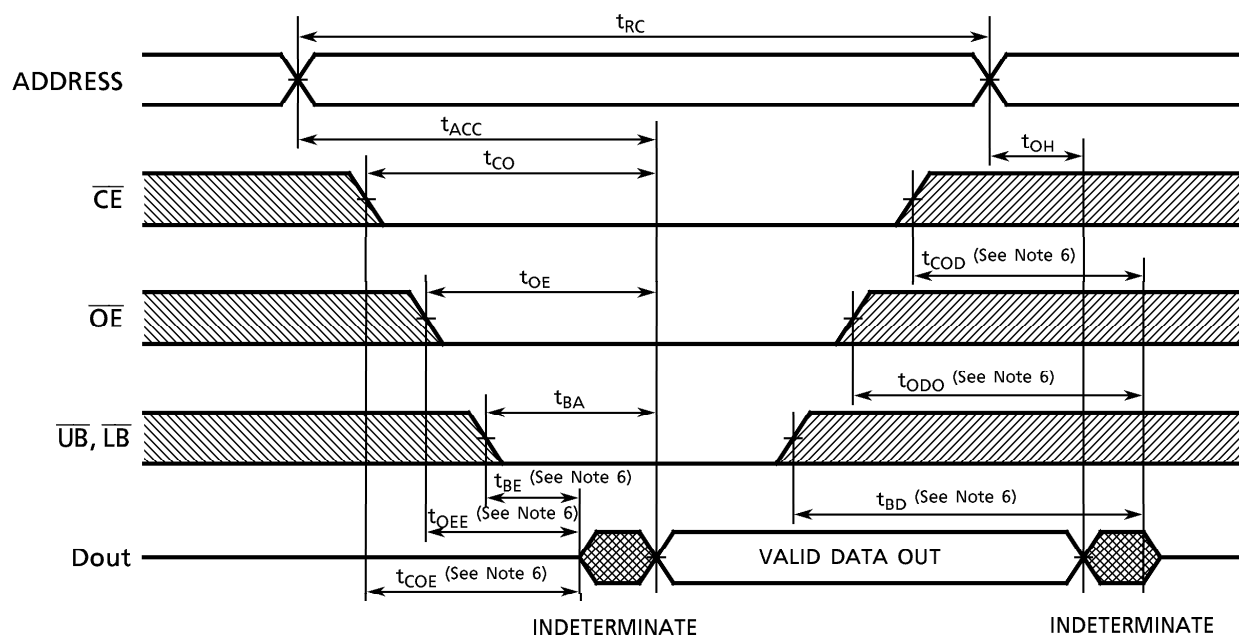
AC TEST CONDITIONS

Input Pulse Level	3.0V/0.0V
Input Pulse Rise and Fall Time	2ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

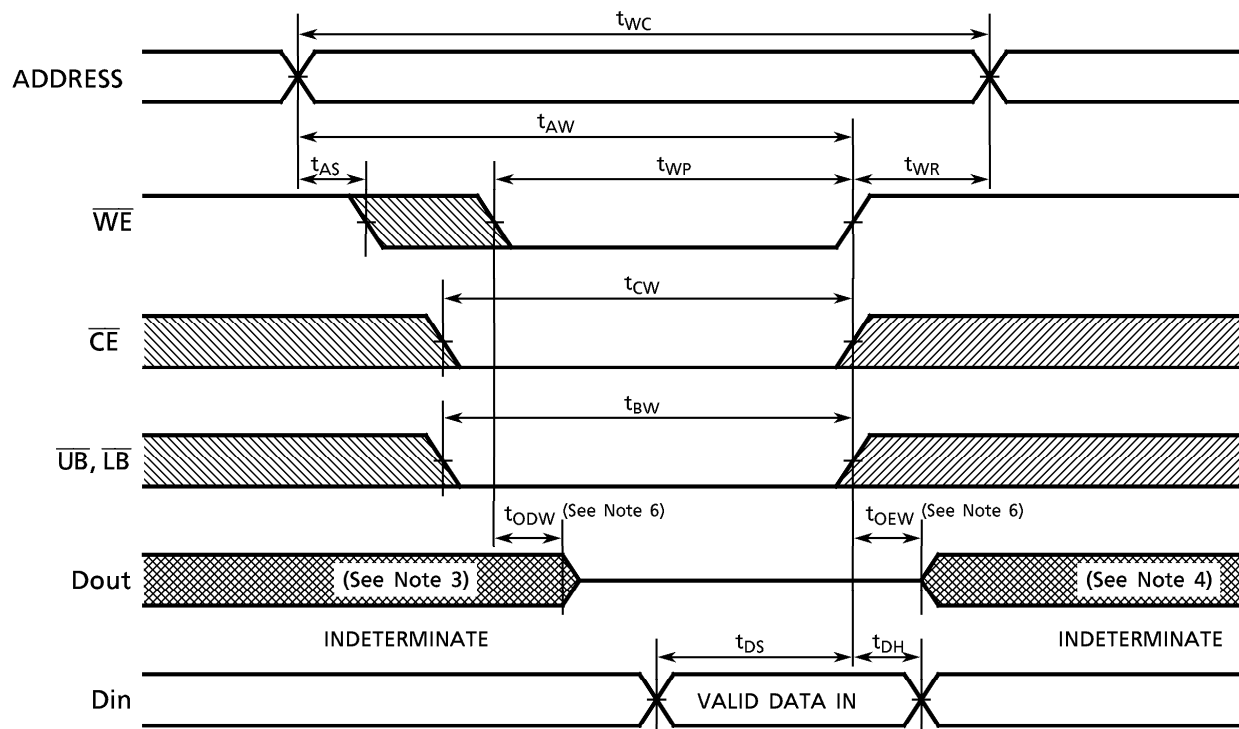
Fig. 1

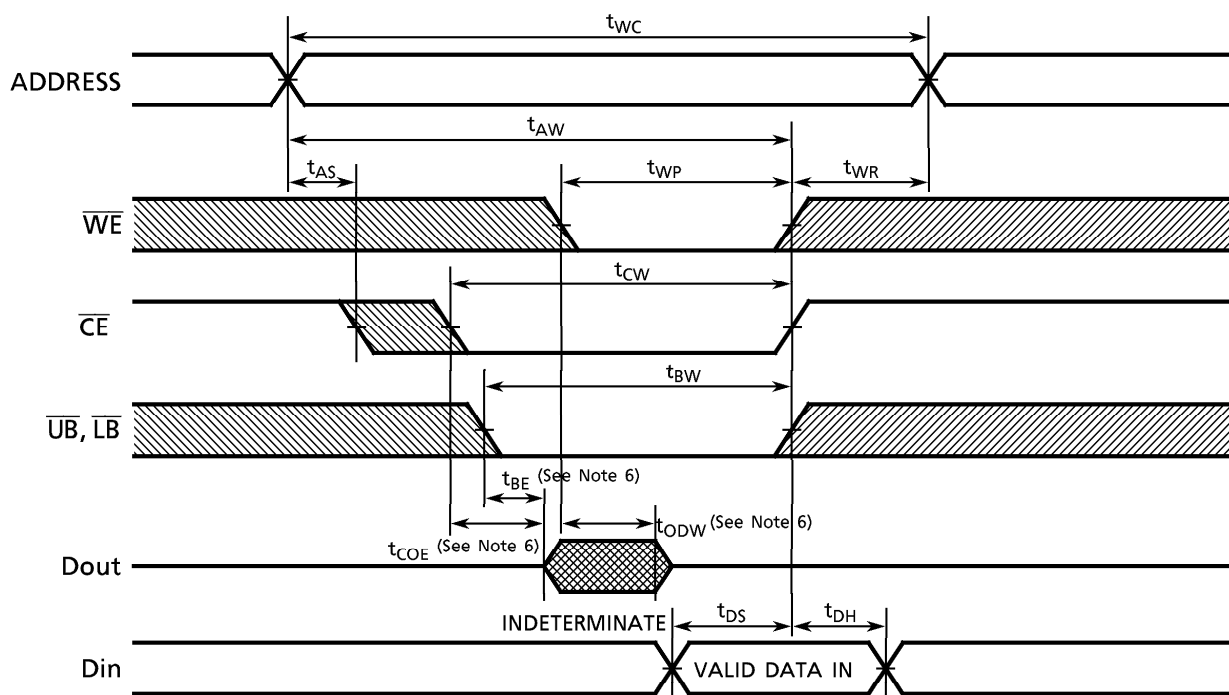
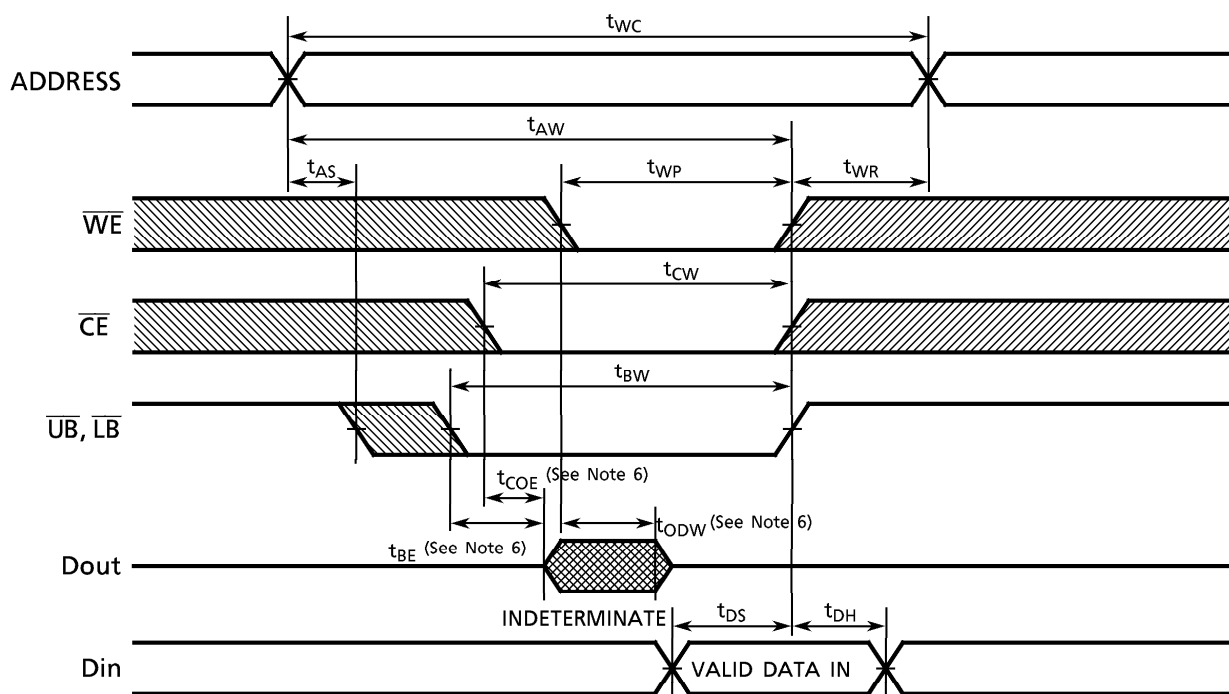
TIMING DIAGRAMS

READ CYCLE (See Note 2)



WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (See Note 5)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 5)WRITE CYCLE 3 ($\overline{\text{UB}}, \overline{\text{LB}}$ CONTROLLED) (See Note 5)

Note: (1) Operating temperature (T_a) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) $\overline{WE}$ remains HIGH for the Read Cycle.

(3) If $\overline{CE}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

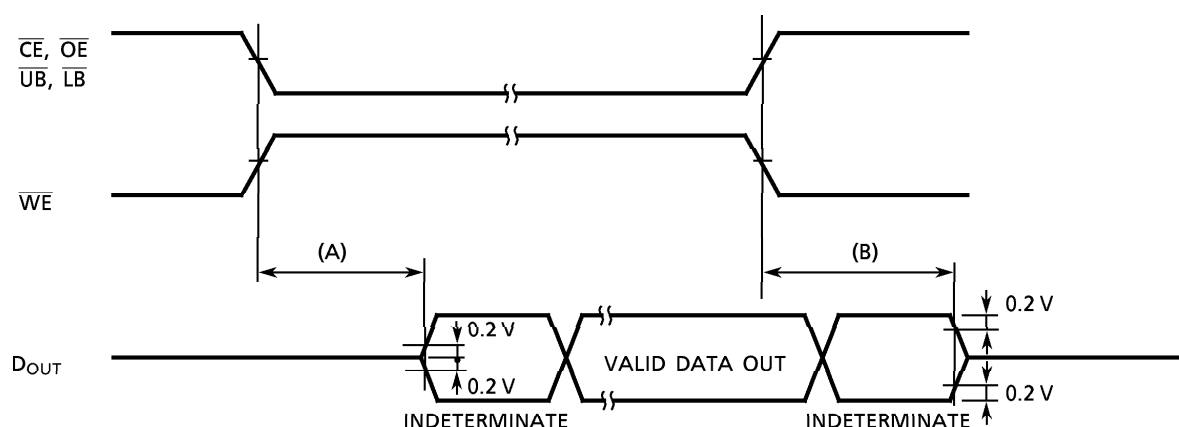
(4) If $\overline{CE}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

(5) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A) t_{COE} , t_{OEE} , t_{BE} , $t_{OE\overline{W}}$ Output Enable Time

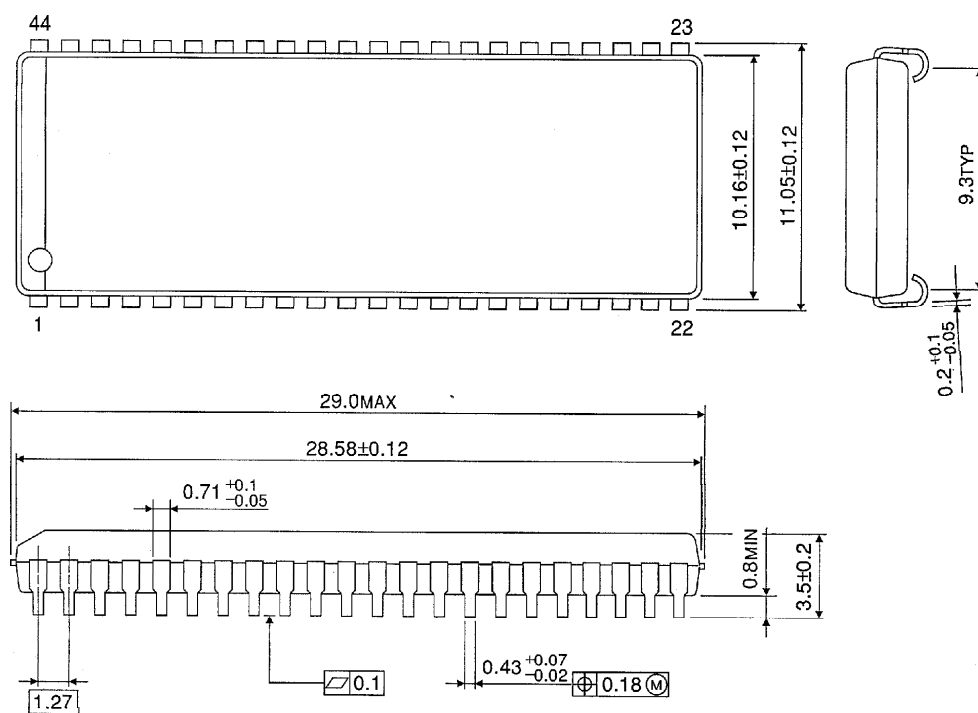
(B) t_{COD} , t_{ODO} , t_{BD} , t_{ODW} Output Disable Time



PACKAGE DIMENSIONS

Plastic SOJ (SOJ44-P-400-1.27)

Unit in mm

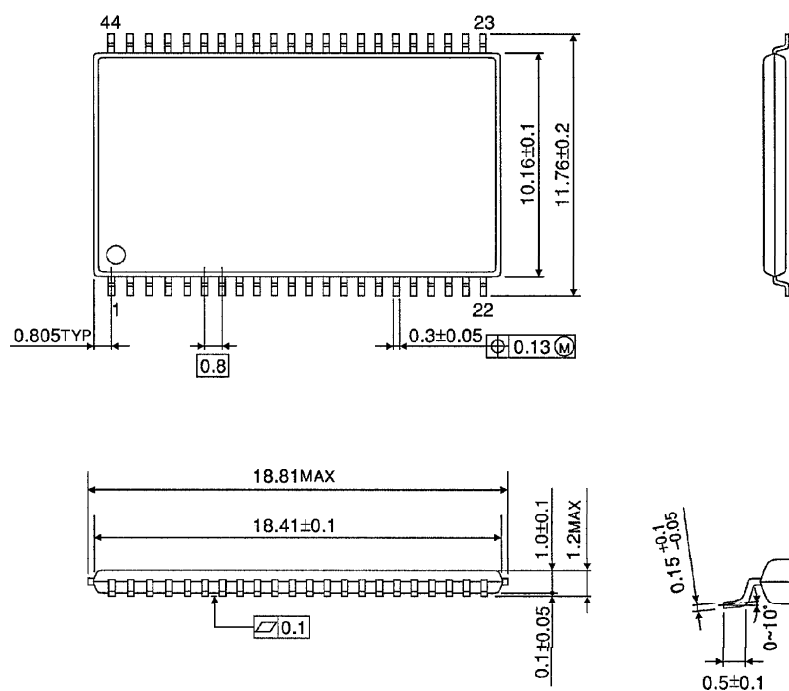


Weight : 1.64g (Typ)

PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 44-P-400-0.80)

Unit in mm



Weight : 0.45g (Typ)