

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

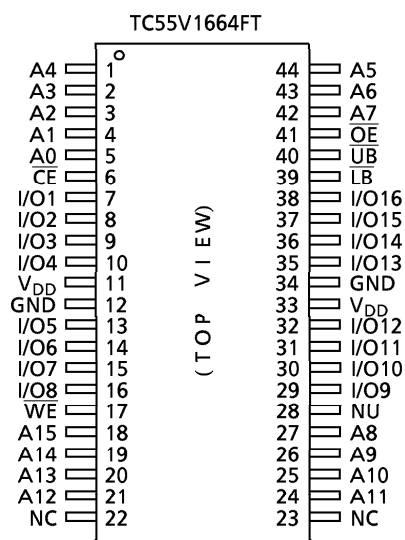
65,536-WORD BY 16-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V1664FT is a 1,048,576-bit high-speed static random access memory (SRAM) organized as 65,536 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed and low-voltage operation, it operates from a single 3.3 V power supply. Chip enable ($\overline{CE}$) can be used to place the device in a low-power mode, and output enable ($\overline{OE}$) provides fast memory access. Data byte control signals (LB, UB) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55V1664FT is available in plastic 44-pin TSOP packages (400 mil width) for high density surface assembly.

FEATURES

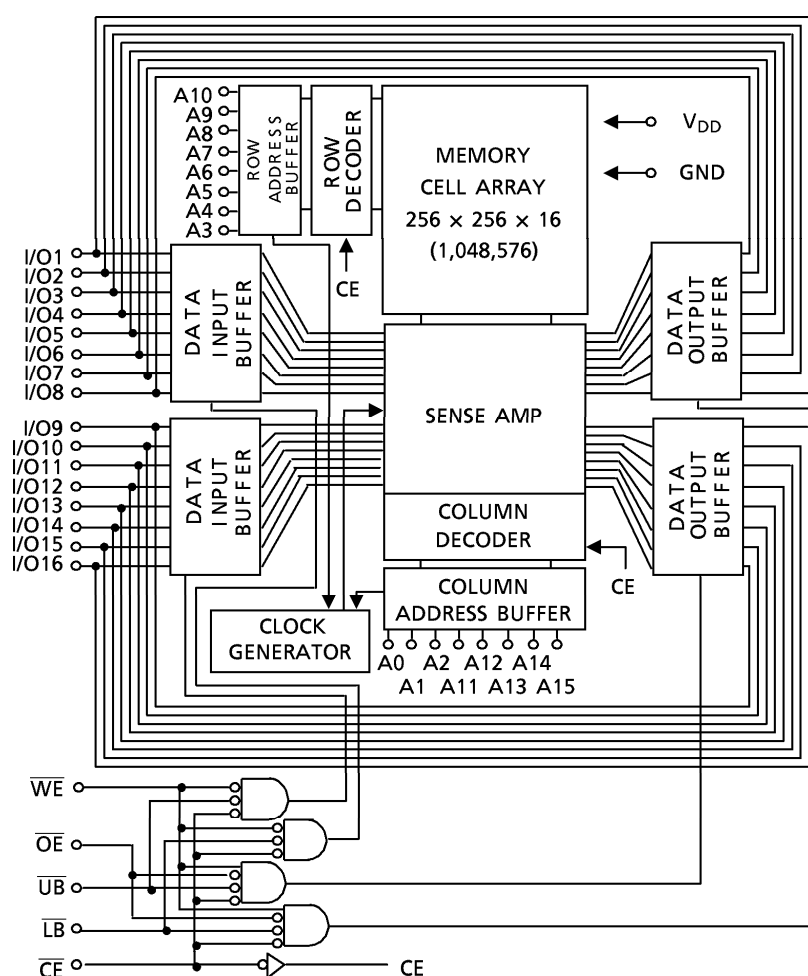
- Fast access time (the following are maximum values)
 - TC55V1664FT-12: 12 ns
 - TC55V1664FT-13: 13 ns
 - TC55V1664FT-15: 15 ns
 - Low-power dissipation (the following are maximum values)
- | | | | | | | |
|-----------------|-----|-----|-----|-----|-----|----|
| Cycle Time | 12 | 13 | 15 | 20 | 30 | ns |
| Operation (max) | 190 | 180 | 170 | 150 | 130 | mA |
- Standby: 2 mA (all devices)
- Single power supply voltage of 3.3 ± 0.3 V.
 - TC55V1664FT-12, -13: $3.3 \text{ V} \pm 5\%$
 - TC55V1664FT-15: 3.3 ± 0.3 V
 - Fully static operation
 - All inputs and outputs are LVTTL compatible
 - Output buffer control using $\overline{OE}$
 - Data byte control using $\overline{LB}$ (IO1 to IO8) and $\overline{UB}$ (IO9 to IO16)
 - Packages:
 - TSOP II 44-P-400-0.80 (Weight: 0.45 g typ)

PIN ASSIGNMENT**PIN NAMES**

A0 to A15	Address Inputs
I/O1 to I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
V_{DD}	Power (+ 3.3 V)
GND	Ground
NC	No Connection
NU	Not Used (Input)

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BLOCK DIAGRAM

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	- 0.5 to 4.6	V
V_{IN}	Input Terminal Voltage	- 0.5 * to 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	- 0.5 * to $V_{DD} + 0.5^{**}$	V
P_D	Power Dissipation	1.2	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	- 65 to 150	°C
T_{opr}	Operating Temperature	- 10 to 85	°C

*: - 1.5 V with a pulse width of $20\% \cdot t_{RC}$ min (4 ns max)

**: $V_{DD} + 1.5$ V with a pulse width of $20\% \cdot t_{RC}$ min (4 ns max)

DC RECOMMENDED OPERATING CONDITIONS ($T_a = 0^\circ \text{ to } 70^\circ \text{C}$)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	- 12, - 13	3.135	3.3	3.465	V
		- 15	3.0	3.3	3.6	
V_{IH}	Input High Voltage		2.0	–	$V_{DD} + 0.3^{**}$	V
V_{IL}	Input Low Voltage		- 0.3 *	–	0.8	V

*: - 1.0 V with a pulse width of $20\% \cdot t_{RC}$ min (4 ns max)**: $V_{DD} + 1.0$ V with a pulse width of $20\% \cdot t_{RC}$ min (4 ns max)DC CHARACTERISTICS ($T_a = 0^\circ \text{ to } 70^\circ \text{C}$, -12, -13: $V_{DD} = 3.3 \text{ V} \pm 5\%$, -15: $V_{DD} = 3.3 \pm 0.3 \text{ V}$)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
I _{IL}	Input Leakage Current (Except NU Pin)	V _{IN} = 0 V to V _{DD}		– 1	–	1	μA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ V _{OUT} = 0 V to V _{DD}		– 1	–	1	μA
I _{I(NU)}	Input Current (NU Pin)	V _{IN} = 0 to 0.8 V		– 1	–	20	μA
		V _{IN} = 0 to 0.2 V		– 1	–	1	
V _{OH}	Output High Voltage	I _{OH} = – 2 mA		2.4	–	–	V
		I _{OH} = – 100 μA		V _{DD} – 0.2	–	–	
V _{OL}	Output Low Voltage	I _{OL} = 2 mA		–	–	0.4	
		I _{OL} = 100 μA		–	–	0.2	
I _{DDO}	Operating Current	$\overline{CE} = V_{IL}$, I _{out} = 0 mA Other Inputs = V _{IH} or V _{IL}	tcycle = 12 ns	–	–	190	mA
			tcycle = 13 ns	–	–	180	
			tcycle = 15 ns	–	–	170	
			tcycle = 20 ns	–	–	150	
			tcycle = 30 ns	–	–	130	
I _{DDS 1}	Standby Current	$\overline{CE} = V_{IH}$, Other Inputs = V _{IH} /V _{IL}		–	–	20	mA
I _{DDS 2}		$\overline{CE} = V_{DD} - 0.2 \text{ V}$ Other Inputs = V _{DD} – 0.2 V/0.2 V		–	–	2	

CAPACITANCE ($T_a = 25^\circ \text{C}$, $f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = \text{GND}$	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	POWER
Read	L	L	H	L	L	Output	Output	I_{DDO}
				H	L	High Impedance	Output	I_{DDO}
				L	H	Output	High Impedance	I_{DDO}
Write	L	x	L	L	L	Input	Input	I_{DDO}
				H	L	High Impedance	Input	I_{DDO}
				L	H	Input	High Impedance	I_{DDO}
Outputs Disable	L	H	H	x	x	High Impedance	High Impedance	I_{DDO}
	L	x	x	H	H			
Standby	H	x	x	x	x	High Impedance	High Impedance	I_{DDs}

x: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V.
 You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS(Ta = 0°C to 70°C (Note 1), -12,-13: V_{DD} = 3.3 V ± 5%, -15: V_{DD} = 3.3 ± 0.3 V)**READ CYCLE**

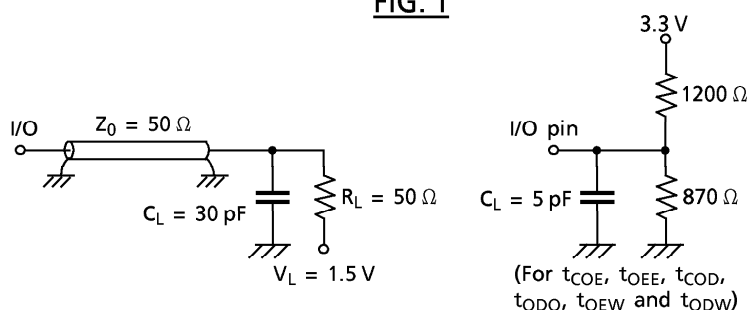
SYMBOL	PARAMETER	TC55V1664FT-12		TC55V1664FT-13		TC55V1664FT-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	12	—	13	—	15	—	ns
t _{ACC}	Address Access Time	—	12	—	13	—	15	
t _{CO}	Chip Enable Access Time	—	12	—	13	—	15	
t _{OE}	Output Enable Access Time	—	6	—	6	—	8	
t _{BA}	Upper Byte, Lower Byte Access Time	—	6	—	6	—	8	
t _{OH}	Output Data Hold Time from Address Change	3	—	3	—	3	—	
t _{COE}	Output Enable Time from Chip Enable	3	—	3	—	3	—	
t _{OEE}	Output Enable Time from Output Enable	1	—	1	—	1	—	
t _{BE}	Output Enable Time from Upper Byte, Lower Byte	1	—	1	—	1	—	
t _{COD}	Output Disable Time from Chip Enable	—	7	—	7	—	8	
t _{ODO}	Output Disable Time from Output Enable	—	7	—	7	—	8	
t _{BD}	Output Disable Time from Upper Byte, Lower Byte	—	7	—	7	—	8	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V1664FT-12		TC55V1664FT-13		TC55V1664FT-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	12	—	13	—	15	—	ns
t _{WP}	Write Pulse Width	8	—	8	—	9	—	
t _{CW}	Chip Enable to End of Write	10	—	10	—	12	—	
t _{BW}	Upper Byte, Lower Byte Enable to End of Write	10	—	10	—	11	—	
t _{AW}	Address Valid to End of Write	10	—	10	—	11	—	
t _{AS}	Address Setup Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	0	—	
t _{DS}	Data Setup Time	7	—	7	—	8	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	
t _{OEW}	Output Enable Time from Write Enable	1	—	1	—	1	—	
t _{ODW}	Output Disable Time from Write Enable	—	7	—	7	—	8	

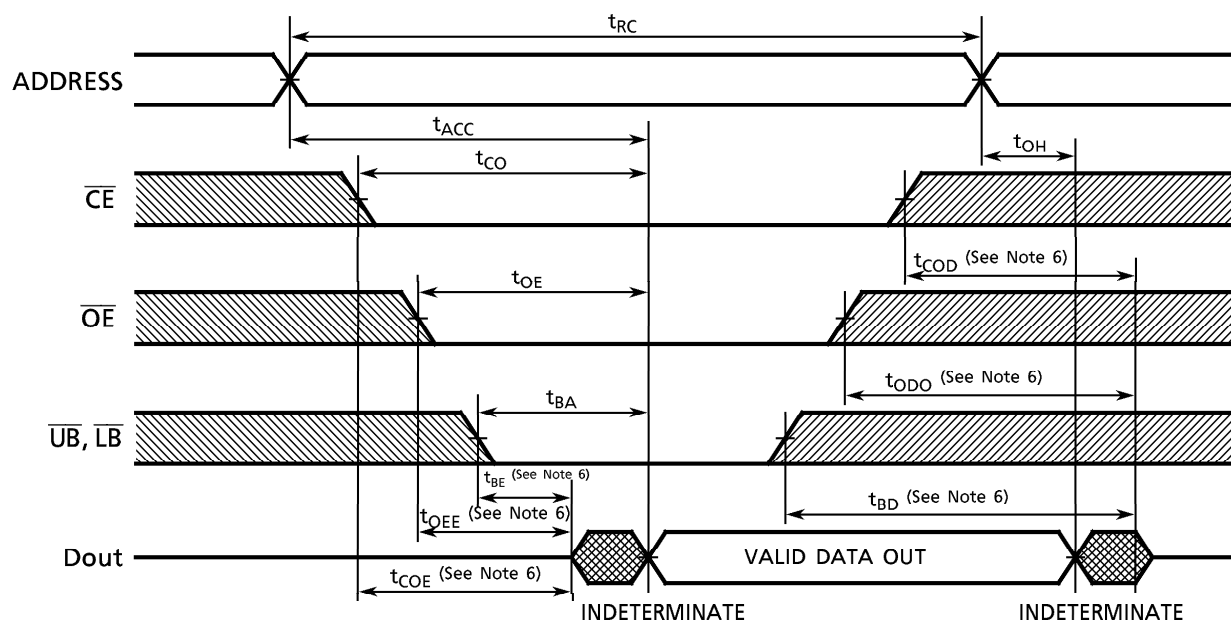
AC TEST CONDITIONS

Input Pulse Level	3.0 V, 0.0 V
Input Pulse Rise and Fall Time	3 ns
Input Timing Measurement Reference Level	1.5 V
Output Timing Measurement Reference Level	1.5 V
Output Load	Fig. 1

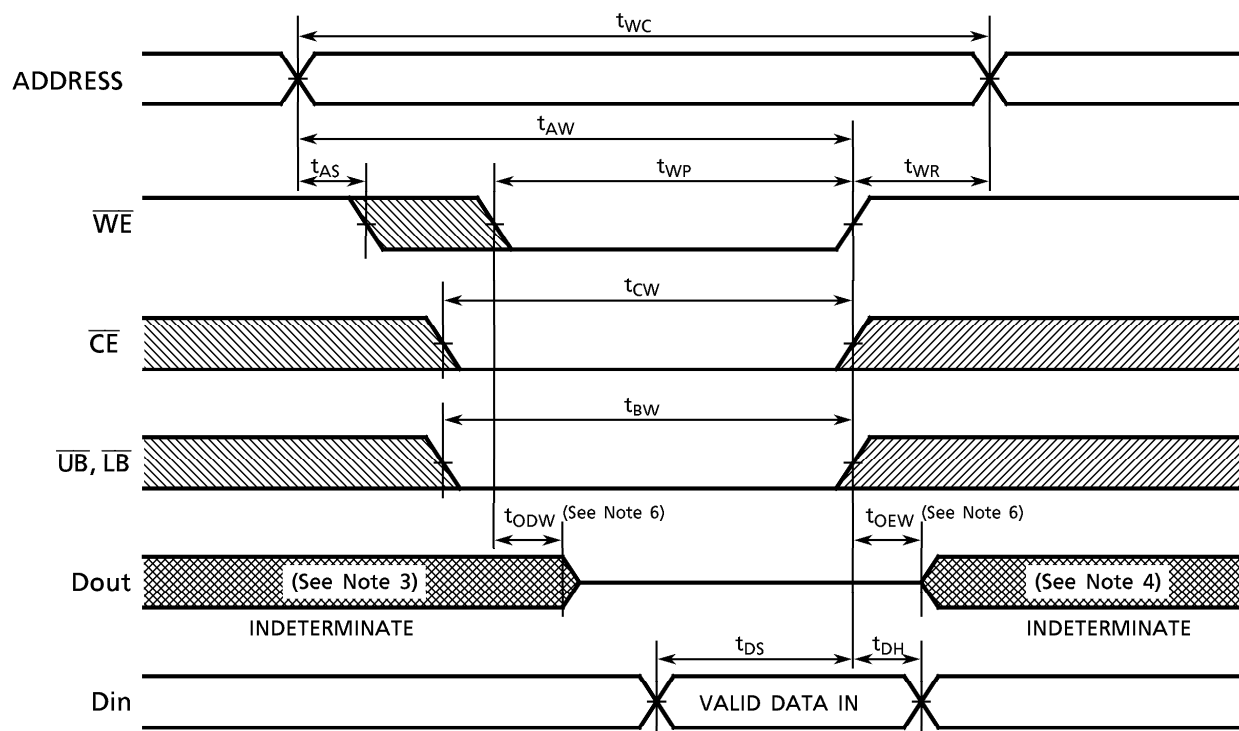
FIG. 1

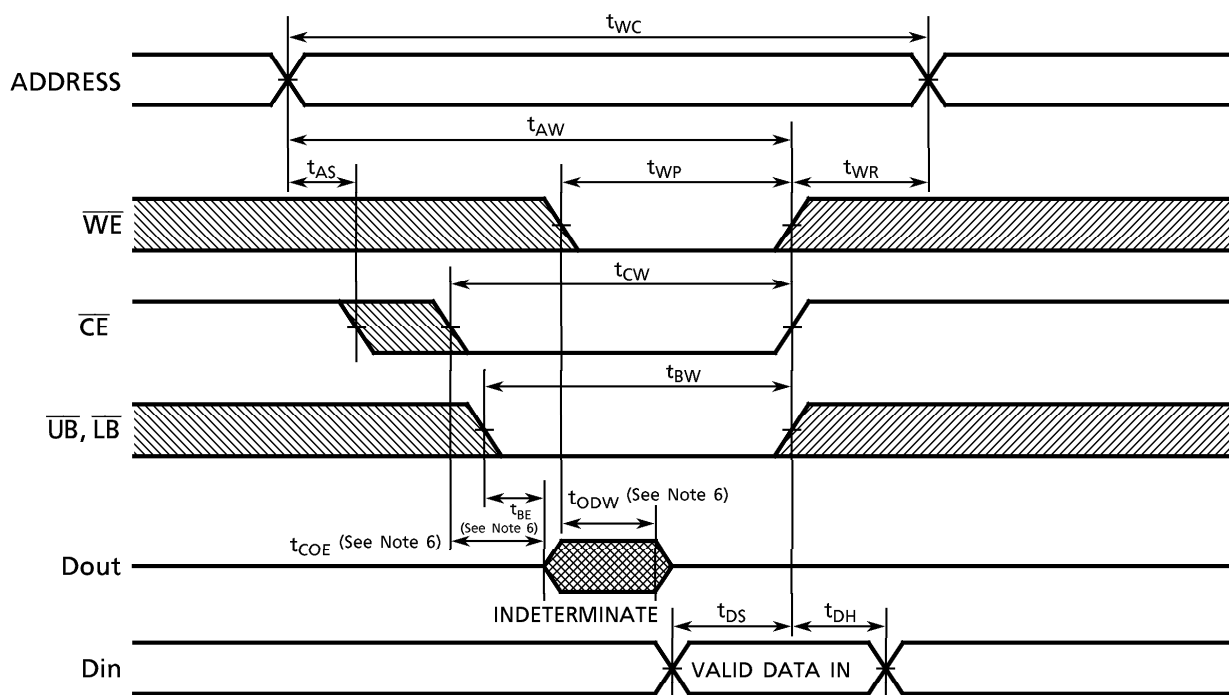
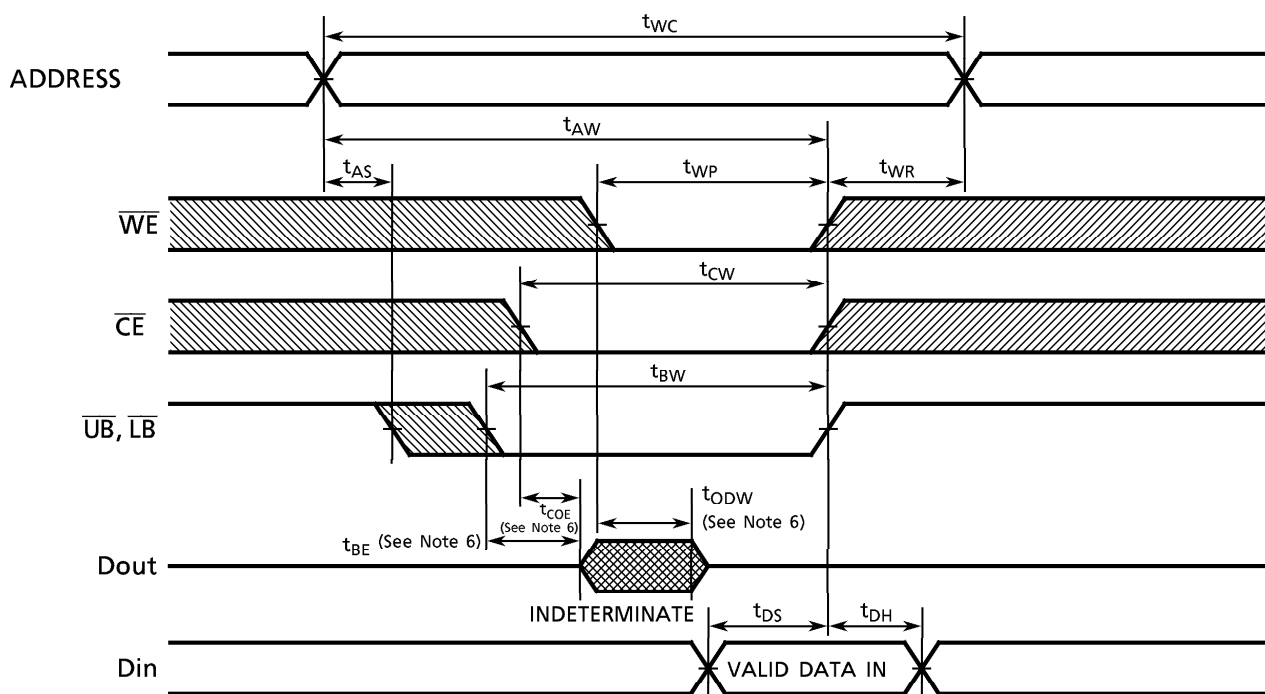
TIMING DIAGRAMS

READ CYCLE (See Note 2)



WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (Note 5)



WRITE CYCLE 2 ($\overline{\text{CE}}$ CONTROLLED) (See Note 5)WRITE CYCLE 3 ($\overline{\text{UB}}, \overline{\text{LB}}$ CONTROLLED) (See Note 5)

Note: (1) Operating temperature (T_a) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) $\overline{WE}$ remains High for the Read Cycle.

(3) If $\overline{CE}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

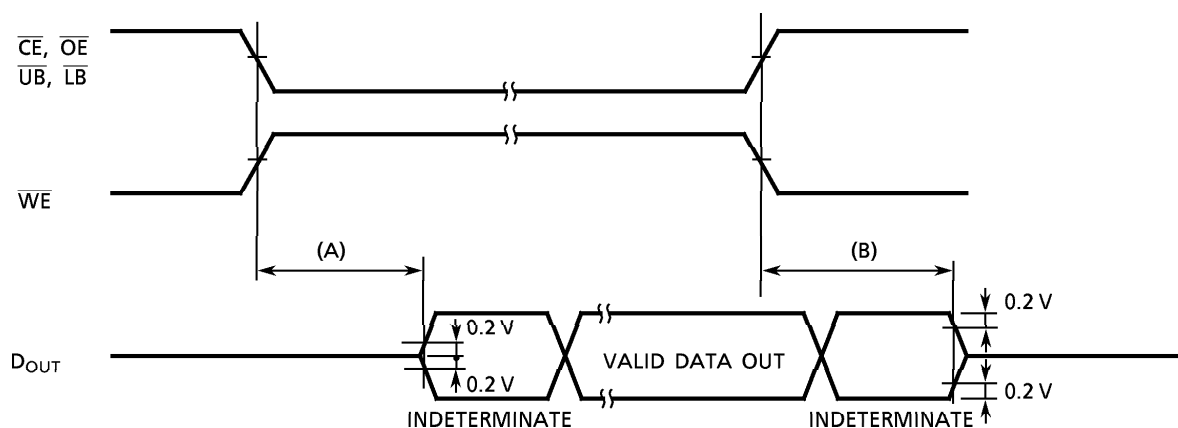
(4) If $\overline{CE}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

(5) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1

(A) $t_{COE}, t_{OEE}, t_{BE}, t_{OE\overline{W}}$ Output Enable Time

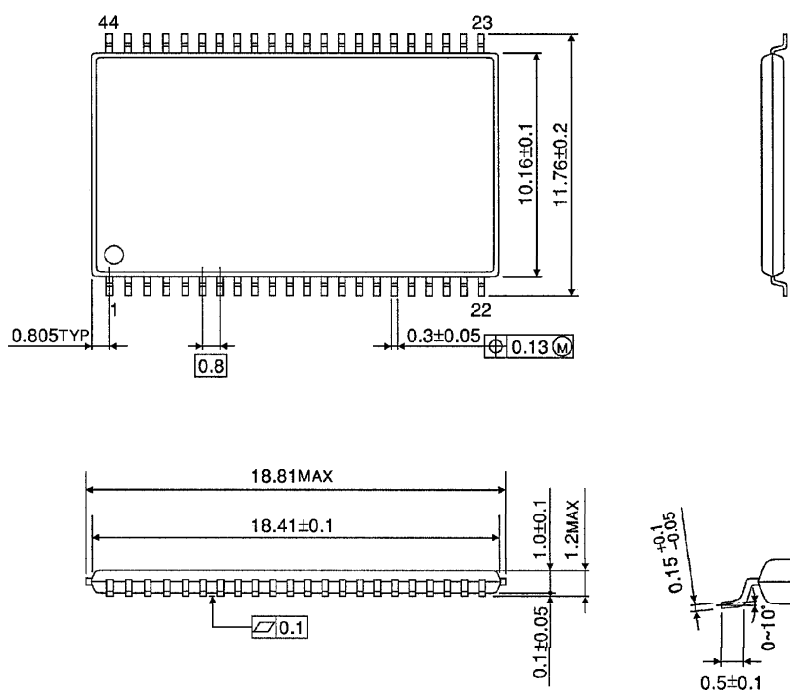
(B) $t_{COD}, t_{ODO}, t_{BD}, t_{OD\overline{W}}$ Output Disable Time



PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 44-P-400-0.80)

Units in mm



Weight: 0.45 g (typ)