TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

131,072-WORD BY 36-BIT SYNCHRONOUS PIPELINED BURST STATIC RAM

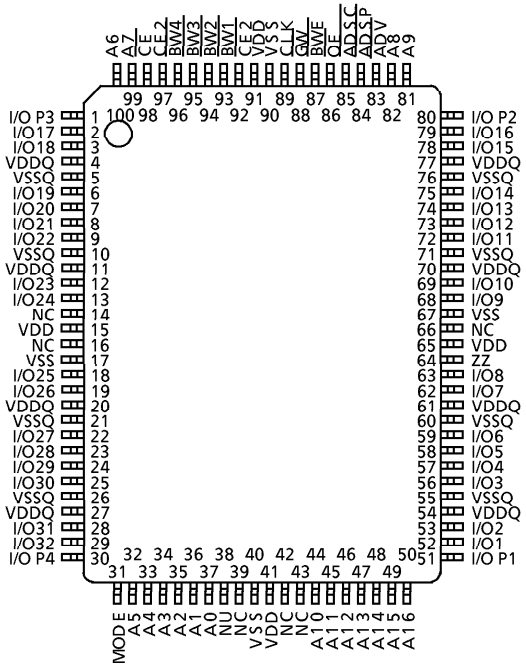
DESCRIPTION

The TC55V4366FFI is a 4,718,592-bit synchronous pipelined burst static random access memory (SRAM) organized as 131,072 words by 36 bits. It is designed for use as a secondary cache to support microprocessor units equipped with burst functions. A 2-bit burst address counter and control logic is integrated with a 128 K × 36 static RAM. All inputs except output enable $\overline{OE}$ are synchronized to the rising edge of the CLK input. Read operations are initiated by the $\overline{ADSP}$ address status processor input or $\overline{ADSC}$ address status controller input. Subsequent burst addresses can be generated internally under control of the $\overline{ADV}$ address advance input. Write operations are internally self-timed and are initiated by the rising edge of CLK. Byte write enables ($\overline{BW1}$ through $\overline{BW4}$) allow one- to four-byte write operations to be performed. It guarantees −40° to 85°C operating temperature so it is suitable for use in wide operating temperature system. The TC55V4366FFI uses dual power supplies (3.3 V for core and 3.3 V/2.5 V for output buffer) and is available in a low-profile 100-pin plastic QFP (LQFP).

FEATURES

- Organization as 128K words by 36 bits.
- Fast cycle time of 6.6ns per minimum (150MHz maximum)
- Fast access time of 4.4ns maximum (from clock edge to data output)
- Pipelined burst operation
- 2-bit burst address counter (interleaved or linear burst sequences)
- Synchronous self-timed write (global write or byte write)
- Stop-clock mode for power down
- Snooze mode pin(ZZ) for power down
- 2 cycle Enable, 1 cycle Disable
- LVTTL compatible interface
- Dual power supply (3.3V for core and 3.3 V/2.5V for output buffer)
- Operating temperature range : −40° to 85°C
- Available in 100-pin LQFP package(LQFP100-P-1420-0.65K:0.65mm pitch, 1.6mm height, typically 0.56 grams)

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 to A16	Address Inputs
I/O1 to I/O32	Data Inputs/Outputs
I/O P1 to I/O P4	Parity Inputs/Outputs
CLK	Clock Input
$\overline{CE}$, $\overline{CE2}$, CE2	Chip Enable
$\overline{ADSP}$	Address Status Processor Input
$\overline{ADSC}$	Address Status Controller Input
$\overline{ADV}$	Address Advance Input
$\overline{GW}$	Global Write Enable Input
$\overline{BWE}$	Byte Write Enable Input
$\overline{BW1}$ to $\overline{BW4}$	Byte Write Enable Inputs
$\overline{OE}$	Output Enable
MODE	Mode Select Input
ZZ	Snooze Input
NU	Not Usable Input
V_{DD}	Power Supply for Core
V_{SS}	Ground for Core
V_{DDQ}	Power Supply for Output Buffer
V_{SSQ}	Ground for Output Buffer
NC	No Connection

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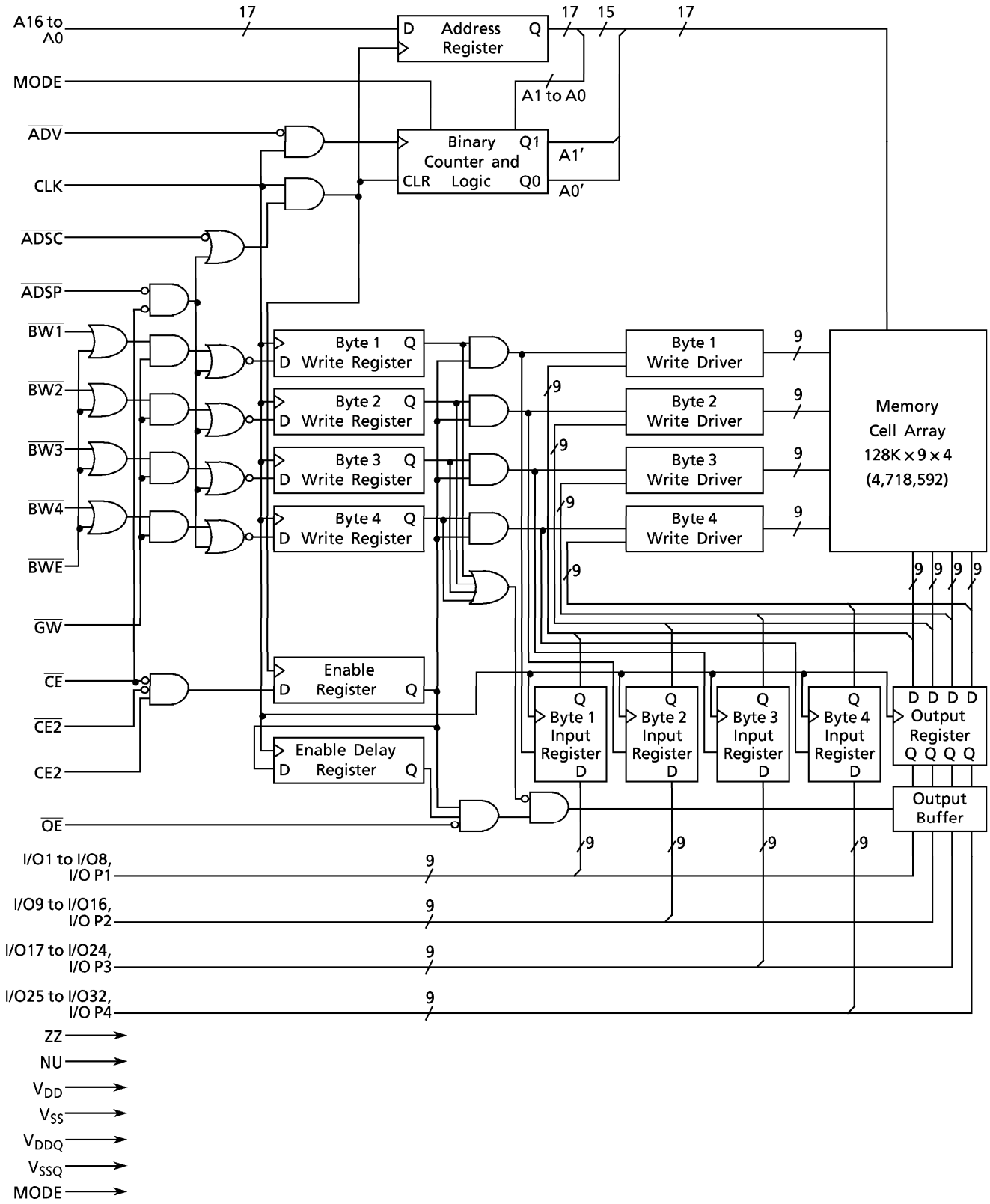
BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50	A0 to A16	Input (synchronous)	**Synchronous Address Inputs** Registered on the rising edge of CLK. Address inputs must meet the specified setup and hold times with respect to the CLK rising edge when the chip is enabled.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input (synchronous)	**Synchronous Byte Write Enables** These active low inputs control byte write operations when $\overline{BWE}$ is low. $\overline{BW1}$ controls I/O1 through I/O8 and I/O P1. $\overline{BW2}$ controls I/O9 through I/O16 and I/O P2. $\overline{BW3}$ controls I/O17 through I/O24 and I/O P3. $\overline{BW4}$ controls I/O25 through I/O32 and I/O P4. For byte write operations, when any of these four inputs go Low, all outputs go to high impedance.
87	$\overline{BWE}$	Input (synchronous)	**Synchronous Byte Write Enable** This active low input controls byte write operations.
88	$\overline{GW}$	Input (synchronous)	**Synchronous Global Write** This active low input controls 32-bit write operations independent of the $\overline{BWE}$ and $\overline{BW1}$ to $\overline{BW4}$ inputs.
89	CLK	Input	**Reference Clock** All synchronous input signals are registered on the rising edge of CLK. Synchronous signal timings are measured from the rising edge of CLK. Synchronous input signals must meet the specified setup and hold times with respect to the rising edge of CLK.
83	$\overline{ADV}$	Input (synchronous)	**Synchronous Burst Advance** This active low signal controls the internal burst address counter after an external address has been loaded. When Low, the internal burst address is advanced. When High, the internal burst address is not advanced. If a write operation initiated by $\overline{ADSP}$ is desired, this signal must be High to write the loaded address on the rising edge of the first clock after the assertion of $\overline{ADSP}$.
84	$\overline{ADSP}$	Input (synchronous)	**Synchronous Address Status Processor** This active low signal controls the burst start by registering a new external address. The write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ to $\overline{BW4}$) are ignored at the assertion of $\overline{ADSP}$ and a read operation is initiated. Subsequent operations are dependent on the write enables at the rising edge of the first clock after the assertion of $\overline{ADSP}$. This signal is ignored if $\overline{CE}$ is High.

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
85	$\overline{ADSC}$	Input (synchronous)	**Synchronous Address Status Controller** This active low signal initiates a burst read or write, depending on the write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ to $\overline{BW4}$), by registering a new external address.
98	$\overline{CE}$	Input (synchronous)	**Synchronous Chip Enable** This active low signal controls the chip status (enable or disable) and the internal use of $\overline{ADSP}$. It is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input (synchronous)	**Synchronous Chip Enable** This active low signal controls the chip status (enable or disable). It is sampled only when a new external address is loaded. It can be used for memory expansion.
97	CE2	Input (synchronous)	**Synchronous Chip Enable** This active high signal controls the chip status (enable or disable). It is sampled only when a new external address is loaded. It can be used for memory expansion.
86	$\overline{OE}$	Input (asynchronous)	**Asynchronous Output Enable** This active low signal controls all 32-bit I/O output buffers. It must be high while write data is being driven prior to the assertion of the byte write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ to $\overline{BW4}$) following a read operation.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	I/O1 to I/O32	Input / Output (synchronous)	**Synchronous Data Inputs/Outputs** Byte1 is I/O1 to I/O8, Byte2 is I/O9 to I/O16, Byte3 is I/O17 to I/O24, Byte4 is I/O25 to I/O32.
51, 80, 1, 30	I/O P1 to I/O P4	Input / Output (synchronous)	**Synchronous Parity Inputs/Outputs** I/O P1 is a parity bit for Byte1 as I/O1 to I/O8. I/O P2 is a parity bit for Byte2 as I/O9 to I/O16. I/O P3 is a parity bit for Byte3 as I/O17 to I/O24. I/O P4 is a parity bit for Byte4 as I/O25 to I/O32.
31	MODE	Input (asynchronous)	**Mode Select** This signal selects the burst sequence. If High or not connected, the burst sequence defaults to Interleaved Burst. If Low, the burst sequence is Linear Burst. This input is pulled up internally. Do not alter the input state while the device is operating.

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
64	ZZ	Input (asynchronous)	**Snooze** This active high signal is used to place the device into sleep mode (low power standby mode). When Low or not connected, the device remains in the active state. When high, the device goes into a sleep state, and memory data is retained. After this signal is deasserted, the device wakes up when a read or write operation is initiated by $\overline{ADSP}$ or $\overline{ADSC}$. If ZZ (sleep) mode will not be used, connect this input to V_{SS}.
38	NU	Input (asynchronous)	**Not Usable** This signal is used only by the manufacturer. This signal must be low or not connected. This input is internally pulled down.
14, 16, 39, 42, 43, 66	NC	—	**No Connection** These inputs are not internally connected.
15, 41, 65, 91	V_{DD}	Supply	**Power Supply**
17, 40, 67, 90	V_{SS}	Ground	**Ground**
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	Supply	**Output Buffer Power Supply**
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	Ground	**Output Buffer Ground**

OPERATING MODE

(1) Synchronous Input Truth Table

OPERATION	CLK	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$ [4]	ZZ [1]	ADDRESS USED	I/O, I/O P [5]	CURRENT [2]
Begin Burst Read	L→H	L	L	H	L	×	×	×	L	External Address	Dout (n)	I_{DDO1}
	L→H	L	L	H	H	L	×	H	L			
Continue Burst Read	L→H	×	×	×	H	H	L	H	L	Next Burst Address	Dout (n)	I_{DDO1}
	L→H	H	×	×	L [6]	H	L	H	L			
Suspend Burst Read	L→H	×	×	×	H	H	H	H	L	Current Burst Address	Dout (n)	I_{DDO2}
	L→H	H	×	×	L [6]	H	H	H	L			
Begin Burst Write	L→H	L	L	H	H	L	×	L	L	External Address	Din (p)	N/A
	L→H	×	×	×	H	H	H	L	L	Current Burst Address		
	L→H	H	×	×	L [6]	H	H	L	L			
Continue Burst Write	L→H	×	×	×	H	H	L	L	L	Next Burst Address	Din (p)	N/A
	L→H	H	×	×	L [6]	H	L	L	L			
Suspend Burst Write	L→H	×	×	×	H	H	H	L	L	Current Burst Address	Din (p)	N/A
	L→H	H	×	×	L [6]	H	H	L	L			
Deselected	L→H	H	×	×	×	L	×	×	L	None	Hi - Z (p)	I_{DDS2}
	L→H	L	H	×	L	×	×	×	L			
	L→H	L	×	L	L	×	×	×	L			
	L→H	L	H	×	H	L	×	×	L			
	L→H	L	×	L	H	L	×	×	L			
Snooze	L→H	×	×	×	×	×	×	×	H	None	Hi - Z (p)	I_{DDS3}

Note: 1. ZZ input, although asynchronous, is included in this table.
2. Consumption current does not include output buffer current.
3. H means logical High and L means logical Low. × means Don't Care.
4. $\overline{WRITE}$ = L means any one or more of the byte write enable inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and $\overline{BWE}$ are Low, or that $\overline{GW}$ is Low. $\overline{WRITE}$ = H means $\overline{GW}$ and $\overline{BWE}$ are High, or $\overline{GW}$ is High and $\overline{BWE}$ is Low and all byte write enable inputs are High.
5. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is the present cycle.
6. When $\overline{CE}$ = H, $\overline{ADSP}$ is disabled ($\overline{ADSP}$ = X). $\overline{ADSP}$ = L to avoid redundancy with the previous truth table entry when $\overline{CE}$ = H and $\overline{ADSP}$ = H.

(2) Partial Truth Table for Write Enables (Synchronous Input)

OPERATION	CLK	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	I/O1 to I/O8, I/O P1	I/O9 to I/O16, I/O P2	I/O17 to I/O24, I/O P3	I/O25 to I/O32, I/O P4
Read	L→H	H	H	×	×	×	×	Dout (n)	Dout (n)	Dout (n)	Dout (n)
	L→H	H	L	H	H	H	H	Dout (n)	Dout (n)	Dout (n)	Dout (n)
Write	L→H	L	×	×	×	×	×	Din (p)	Din (p)	Din (p)	Din (p)
		H	L	L	L	L	L	Din (p)	Din (p)	Din (p)	Din (p)
		H	L	L	H	H	H	Din (p)	Hi - Z (p)	Hi - Z (p)	Hi - Z (p)
				H	L	H	H	Hi - Z (p)	Din (p)	Hi - Z (p)	Hi - Z (p)
				H	H	L	H	Hi - Z (p)	Hi - Z (p)	Din (p)	Hi - Z (p)
				H	H	H	L	Hi - Z (p)	Hi - Z (p)	Hi - Z (p)	Din (p)
				The other 11 combinations of $\overline{BW1}$ to $\overline{BW4}$ are also effective. $\overline{BW1}$ controls I/O1 to I/O8 and I/O P1. $\overline{BW2}$ controls I/O9 to I/O16 and I/O P2. $\overline{BW3}$ controls I/O17 to I/O24 and I/O P3. $\overline{BW4}$ controls I/O25 to I/O32 and I/O P4.						

Note : 1. (n) and (p) indicate the cycles affected by the synchronous control inputs. (n) is the next cycle, (p) is the present cycle.

(3) Asynchronous Truth Table

OPERATION	$\overline{OE}$	ZZ	I/O1 to I/O32, I/O P1 to I/O P4
Read	L	L	Dout
	H	L	Hi - Z
Write	×	L	Din, Hi - Z
Deselected	×	L	Hi - Z
Snooze	×	H	Hi - Z

(4) Write Pass-through Truth Table

Previous Cycle				Present Cycle											Next Cycle
Operation	Addr.	$\overline{WRITE}$	I/O	Operation	Addr.	$\overline{WRITE}$	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	I/O, I/O P	I/O, I/O P
Write Cycle	Ak	L	Dn (Ak)	$\overline{ADSP}$ Initiated Read Cycle	Am	×	L	L	H	L	×	×	L	Qn (Ak)	Q1 (Am)
				$\overline{ADSC}$ Initiated Read Cycle	Am	H	L	L	H	H	L	×	L		
				Continue Read Cycle	×	H	×	×	×	H	H	L	L		Qn + 1 (Ak)
					×	H	H	×	×	L	H	L	L		

Note: 1. Dn (Ak) represents input data for the n^{th} burst address starting from address Ak.
2. Qn (Ak) represents output data from the n^{th} burst address starting from address Ak.
3. n = 1, 2, 3, or 4
4. $\overline{WRITE}$ = L means that any one or more of the byte write enable inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and $\overline{BWE}$ are Low, or that $\overline{GW}$ is Low. $\overline{WRITE}$ = H means $\overline{GW}$ and $\overline{BWE}$ are High, or $\overline{GW}$ is High and $\overline{BWE}$ is Low and all byte write enable inputs are High.

(5) Interleaved Burst Sequence (MODE Input = NC or V_{DD})

Bit Order : A_{16} A_{13} ..... A_3 A_2 A_1 A_0
The lower 2 bits are internally generated from the external address.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
XX ····· XX00	XX ····· XX01	XX ····· XX10	XX ····· XX11
XX ····· XX01	XX ····· XX00	XX ····· XX11	XX ····· XX10
XX ····· XX10	XX ····· XX11	XX ····· XX00	XX ····· XX01
XX ····· XX11	XX ····· XX10	XX ····· XX01	XX ····· XX00

The burst address wraps around to its initial state.

(6) Linear Burst Sequence (MODE Input = V_{SS})

Bit Order : A_{16} A_{13} ..... A_3 A_2 A_1 A_0
The lower 2 bits are internally generated from the external address.

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
XX ····· XX00	XX ····· XX01	XX ····· XX10	XX ····· XX11
XX ····· XX01	XX ····· XX10	XX ····· XX11	XX ····· XX00
XX ····· XX10	XX ····· XX11	XX ····· XX00	XX ····· XX01
XX ····· XX11	XX ····· XX00	XX ····· XX01	XX ····· XX10

The burst address wraps around to its initial state.

(7) Stop-Clock Mode for Power Down

The TC55V4366FFI achieves low power standby mode by stopping the clock input.
It can retains all state and data values even though the clock is not running.

To achieve the lowest possible power operation, the following signal states are required.

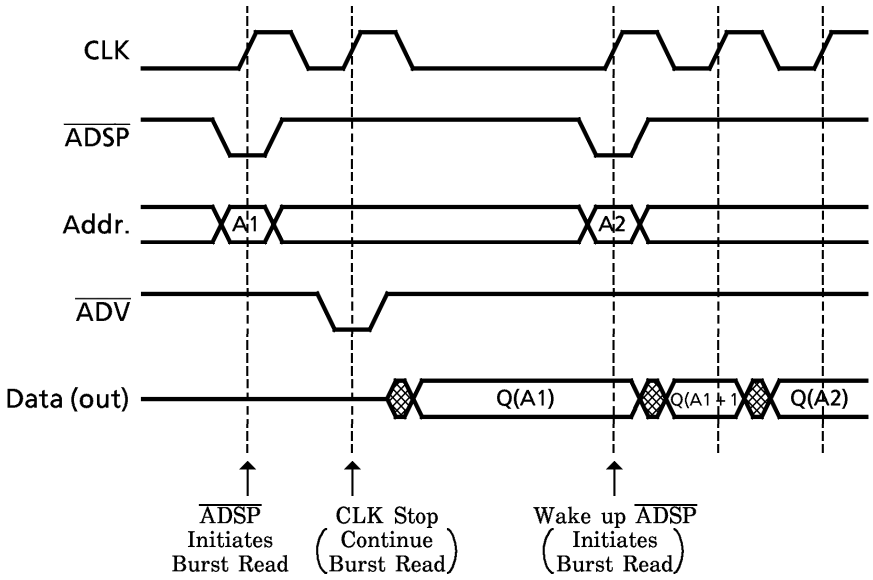
i) Clock is Low

ii) Control signals are inactive (for example, $\overline{ADSP}$ is High)

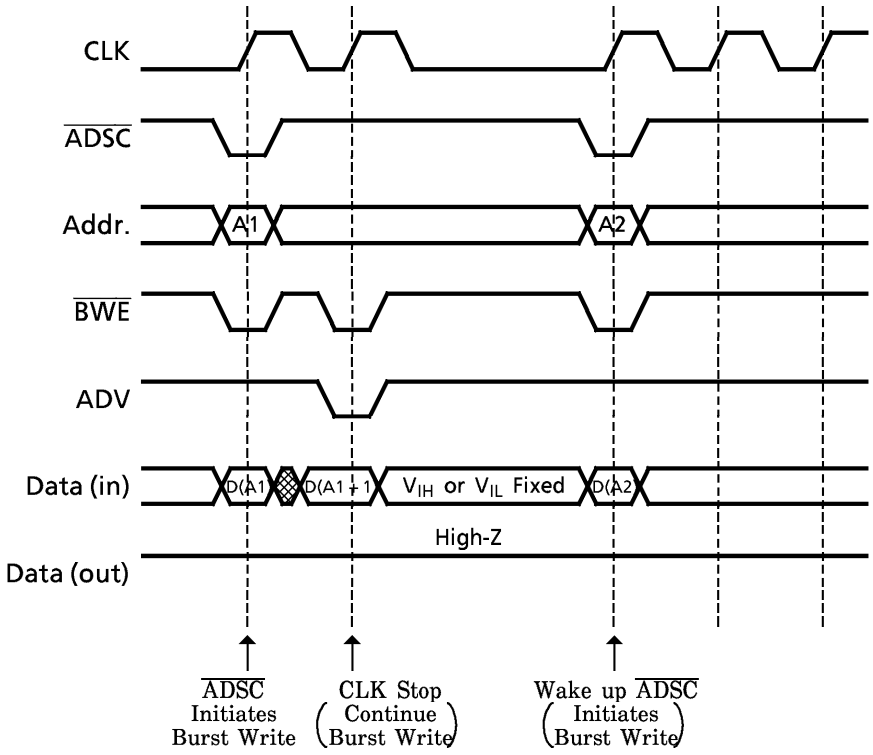
For the lowest possible power consumption during stop-clock mode, the address inputs should be driven to MOS level ($V_{IH} \geqq V_{DD} - 0.2$ V or $V_{IL} \leqq 0.2$ V), and the data inputs should be driven to MOS low level ($V_{IL} \leqq 0.2$ V).

· Clock restart sequence

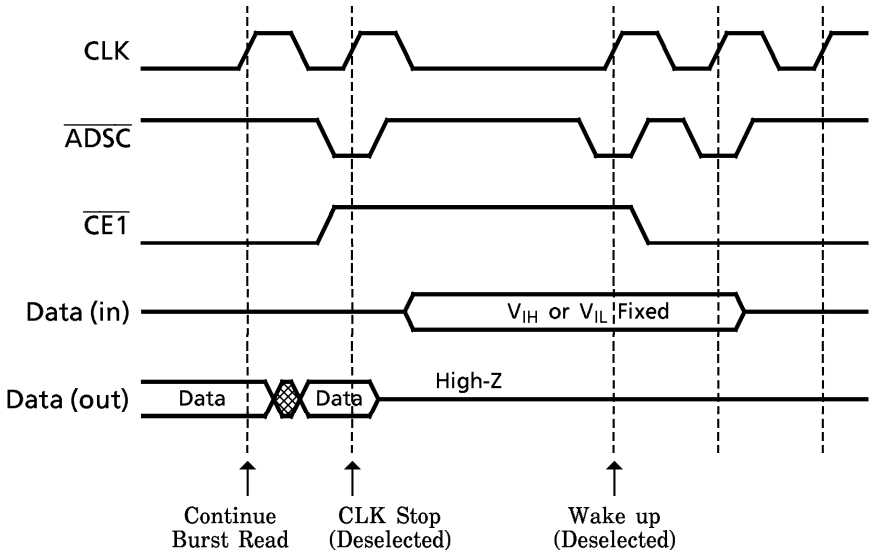
The device can be waked up by the first rising edge of the clock signal after having been in power down mode.



i) Stop-Clock Timing for Read Operation



ii) Stop-Clock Timing for Write Operation



iii) Stop-Clock Timing for Deselect Operation

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	− 0.5 to 4.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	− 0.5 to V_{DD}	V
V_{IN}	Input Terminal Voltage	− 0.5 * to 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	− 0.5* to V_{DDQ} + 0.5**	V
P_D	Power Dissipation	1.2	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	− 65 to 150	°C
T_{opr}	Operating Temperature	− 40 to 85	°C

* : −1.5V with a pulse width of 20% · t_{KC} min
** : V_{DDQ}+1.5V with a pulse width of 20% · t_{KC} min

DC RECOMMENDED OPERATING CONDITIONS (Ta = − 40~85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	3.1	3.3	3.6	V
V_{DDQ}	Output Buffer Power Supply Voltage	2.3	−	3.6	V
V_{IH}	Input High Voltage for Address and Control pins (except I/O and Mode pin)	1.7	−	V_{DD} + 0.3	V
	Input High Voltage for I/O pins	1.7	−	V_{DDQ} + 0.3**	
$V_{IH\,1}$	Input High Voltage for MODE pin	V_{DD} − 0.3	V_{DD}	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	− 0.3*	−	0.7	V
$V_{IL\,1}$	Input Low Voltage for MODE and NU pins	− 0.3	0.0	0.3	V

* : −1.0V with a pulse width of 20% · t_{KC} min
** : V_{DDQ}+1.0V with a pulse width of 20% · tKC min

Note : NU pin must be low or not connected.
You must not apply a voltage of more than 0.8 V to the NU.

DC CHARACTERISTICS (Ta = −40° to 85°C, V_{DD} = 3.1V to 3.6V, V_{DDQ} = 2.3V to 2.7V or 3.1V to 3.6V)

SYMBOL	PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current (Except MODE, ZZ, NU pins)		V_{IN} = 0 to V_{DD}		−	−	±1	μA
I_{LO}	Output Leakage Current		Device Deselected or Output Deselected, V_{OUT} = 0 to V_{DD}		−	−	±1	μA
I_I	Input Current	MODE pin	V_{IN} = V_{DD} to V_{DD} − 0.3V		−1	−	1	μA
			V_{IN} = 0 to 0.3V		−100	−	1	
		ZZ pin	V_{IN} = V_{DD} to 2.0V		−1	−	100	
			V_{IN} = 0 to 0.8V		−1	−	20	
			V_{IN} = 0 to 0.3V		−1	−	1	
		NU pin	V_{IN} = 0 to 0.3V		−1	−	1	
V_{OH}	Output High Voltage	V_{DDQ} = 3.3V	I_{OH} = −8mA		2.4	−	−	V
			I_{OH} = −100μA		V_{DDQ} − 0.2	−	−	
		V_{DDQ} = 2.5V	I_{OH} = −2mA		1.9	−	−	
			I_{OH} = −100μA		V_{DDQ} − 0.2	−	−	
V_{OL}	Output Low Voltage	V_{DDQ} = 3.3V	I_{OL} = 8mA		−	−	0.4	
			I_{OL} = 100μA		−	−	0.2	
		V_{DDQ} = 2.5V	I_{OL} = 2mA		−	−	0.4	
			I_{OL} = 100μA		−	−	0.2	
I_{DDO1}	Operating Current		Device Selected, Iout = 0mA All inputs = V_{IH} / V_{IL} CLK ≧ t_{KC} min	150MHz	−	−	365	mA
				133MHz	−	−	340	
I_{DDO2}	Operating Current (Idle)		Device Selected, Iout = 0mA $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≧ V_{IH} All inputs = V_{IH} / V_{IL}, CLK ≧ t_{KC} min	150MHz	−	−	325	mA
				133MHz	−	−	300	
I_{DDS1}	Standby Current (CLK running)		Device Deselected, All inputs ≦ V_{IH} / V_{IL} CLK ≧ t_{KC} min	150MHz	−	−	105	mA
				133MHz	−	−	100	
I_{DDS2}	Standby Current		Device Deselected, All inputs ≦ V_{DD} − 0.2V or 0.2V, CLK frequency = 0Hz		−	−	3	mA
I_{DDS3}	Snooze Current while ZZ Pin is High		ZZ = V_{DD} − 0.2V, All inputs = V_{IH} / V_{IL} CLK ≧ t_{KC} min		−	−	3	mA
I_{DDS4}	Snooze Current during Stop-Clock Mode		ZZ ≦ 0.2V, Chip Deselected CLK ≦ 0.2V, $\overline{ADSP}$, $\overline{ADSC}$ = V_{DD} − 0.2V All inputs ≦ 0.2V		−	−	3	mA

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
	Input Capacitance for MODE, ZZ, NU pin	V_{IN} = GND	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	6	pF

Note: This parameter is periodically sampled and is not 100% tested.

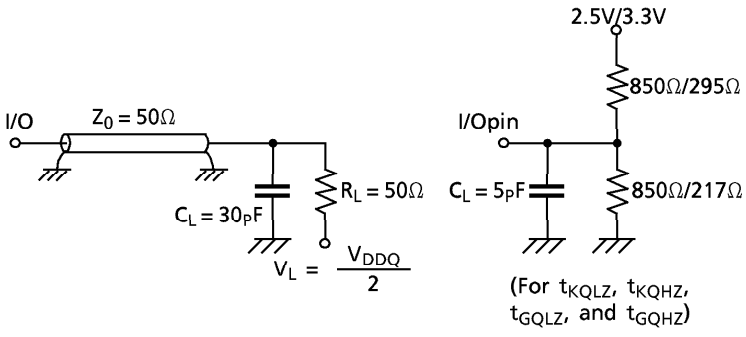
AC CHARACTERISTICS (Ta = −40° to 85°C, V_{DD} = 3.1V to 3.6V, V_{DDQ} = 2.3V to 2.7V or 3.1V to 3.6V)

SYMBOL	PARAMETER	TC55V4366FFI-150		TC55V4366FFI-133		UNIT
		MIN	MAX	MIN	MAX	
t_{KC}	CLK Cycle Time	6.6	–	7.5	–	ns
t_{KH}	CLK High Pulse Width	2.2	–	2.5	–	
t_{KL}	CLK Low Pulse Width	2.2	–	2.5	–	
t_{KQV}	Access Time from CLK	–	4.4	–	5	
t_{KQX}	Output Hold Time from CLK	1.5	–	1.5	–	
t_{KQLZ}	Output Enable Time from CLK	0	–	0	–	
t_{KQHZ}	Output Disable Time from CLK	1.5	6.6	1.5	7.5	
t_{GQV}	Access Time from $\overline{OE}$	–	4	–	4.5	
t_{GQLZ}	Output Enable Time from $\overline{OE}$	0	–	0	–	
t_{GQHZ}	Output Disable Time from $\overline{OE}$	–	4	–	4.5	
t_{AS}	Address Input Setup Time from CLK	1.5	–	1.5	–	
t_{AH}	Address Input Hold Time from CLK	0.5	–	0.5	–	
t_{ADSS}	$\overline{ADSP}$, $\overline{ADSC}$ Input Setup Time from CLK	1.5	–	1.5	–	
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Input Hold Time from CLK	0.5	–	0.5	–	
t_{AVS}	$\overline{ADV}$ Input Setup Time from CLK	1.5	–	1.5	–	
t_{AVH}	$\overline{ADV}$ Input Hold Time from CLK	0.5	–	0.5	–	
t_{WS}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ to $\overline{BW4}$ Input Setup Time from CLK	1.5	–	1.5	–	
t_{WH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ to $\overline{BW4}$ Input Hold Time from CLK	0.5	–	0.5	–	
t_{CES}	$\overline{CE}$, $\overline{CE2}$, CE2 Input Setup Time from CLK	1.5	–	1.5	–	
t_{CEH}	$\overline{CE}$, $\overline{CE2}$, CE2 Input Hold Time from CLK	0.5	–	0.5	–	
t_{DS}	Data Setup Time from CLK	1.5	–	1.5	–	
t_{DH}	Data Hold Time from CLK	0.5	–	0.5	–	
t_{ZS}	ZZ Standby Time	5	–	5	–	
t_{ZR}	ZZ Recovery Time	6	–	6	–	
t_{ZHZ}	Output Disable Time from ZZ	–	2	–	2	cycle

AC TEST CONDITIONS

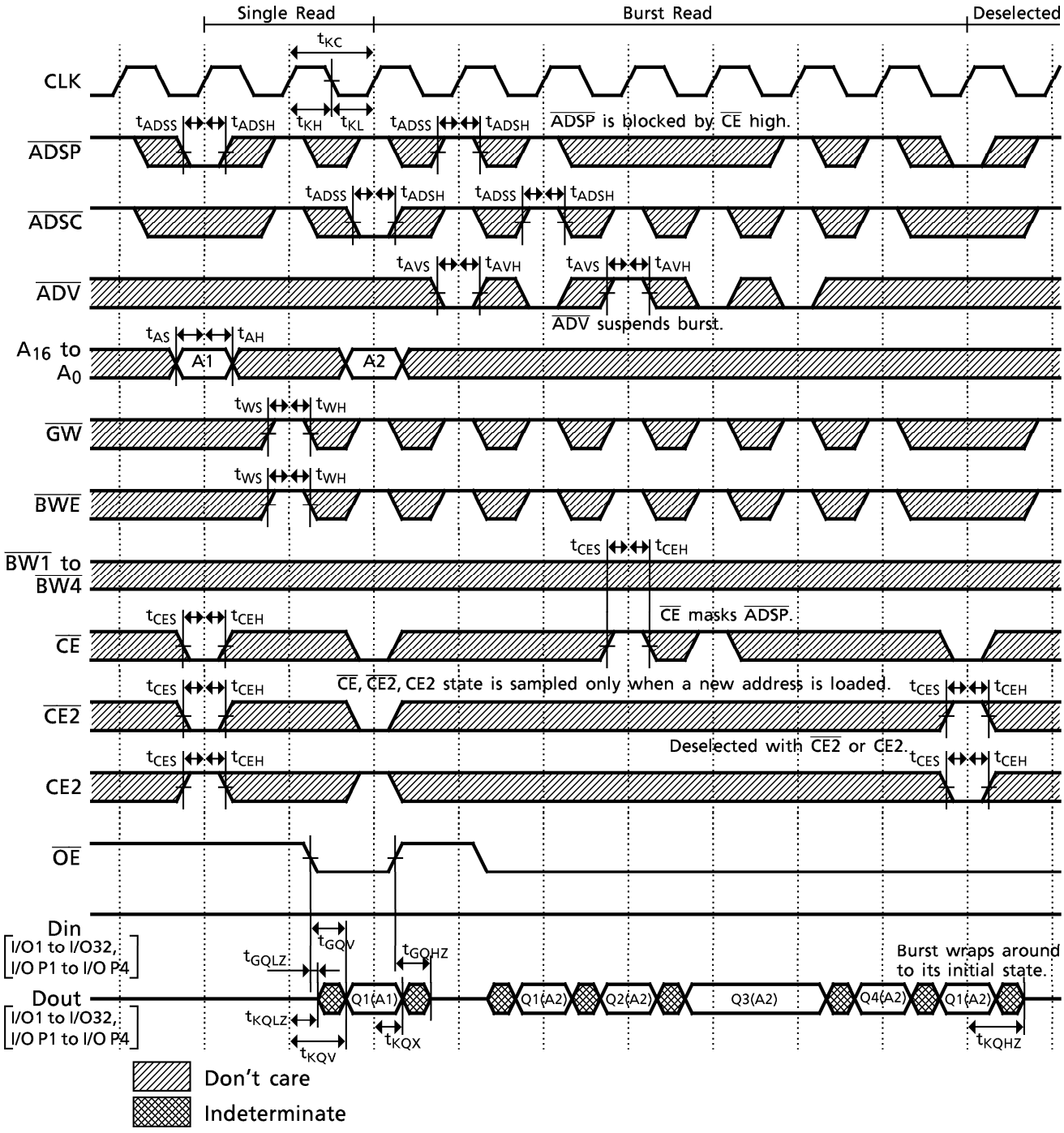
	V_{DDQ} = 2.5V	V_{DDQ} = 3.0V
Input Pulse Level	2.5V/0.0V	3.0V/0.0V
Input Pulse Rise and Fall Time	1.8ns	2.0ns
Input Timing Measurement Reference Level	1.25V	1.5V
Output Timing Measurement Reference Level	$\frac{V_{DDQ}}{2}$	$\frac{V_{DDQ}}{2}$
Output Load	Fig. 1	Fig. 1

Fig. 1



TIMING DIAGRAMS

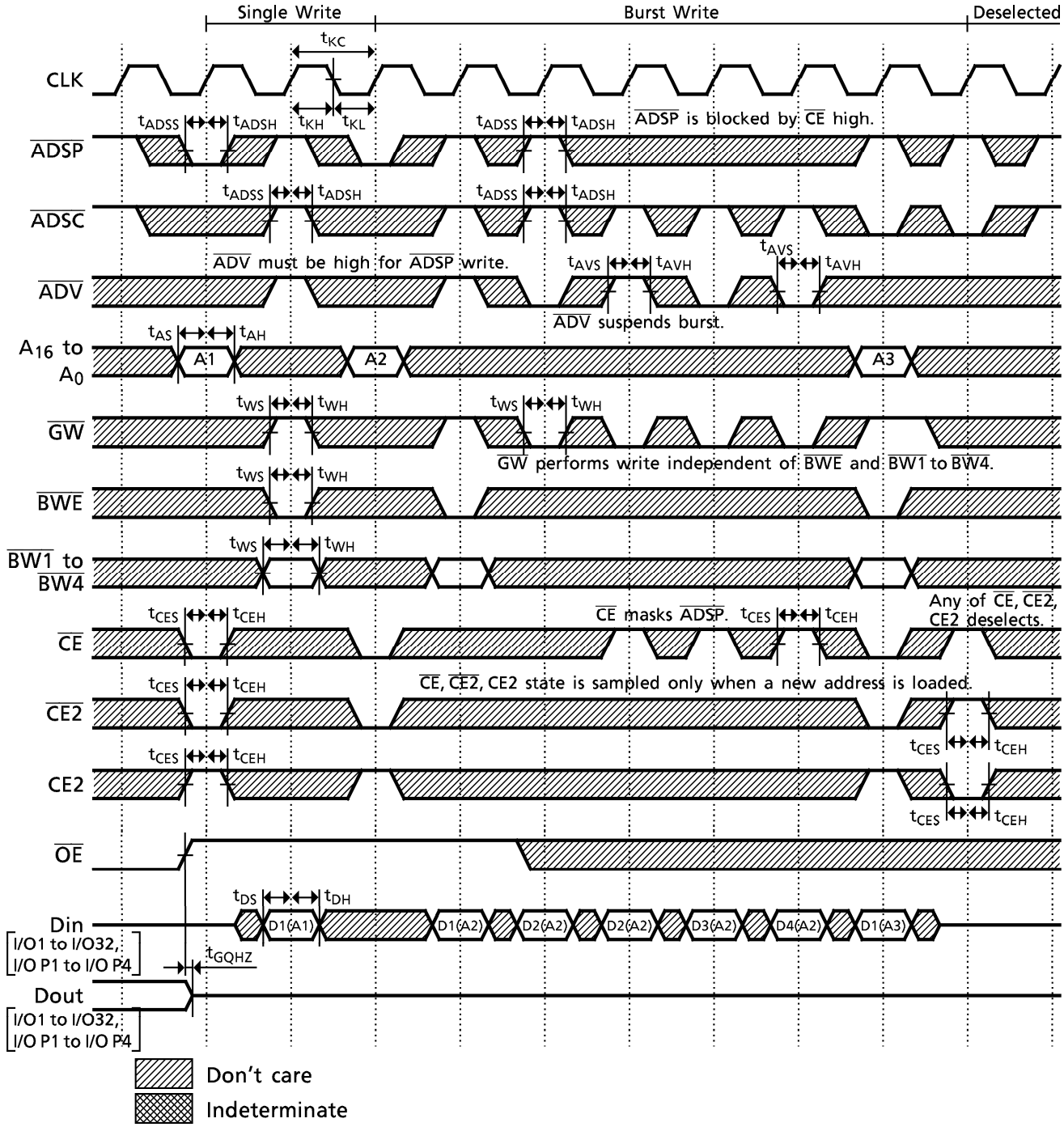
READ CYCLE



Note

1. Q1(A2) represents output data from 1st burst address starting from address A2. Q2(A2) represents output data from 2nd burst address starting from address A2.
2. ZZ is Low.

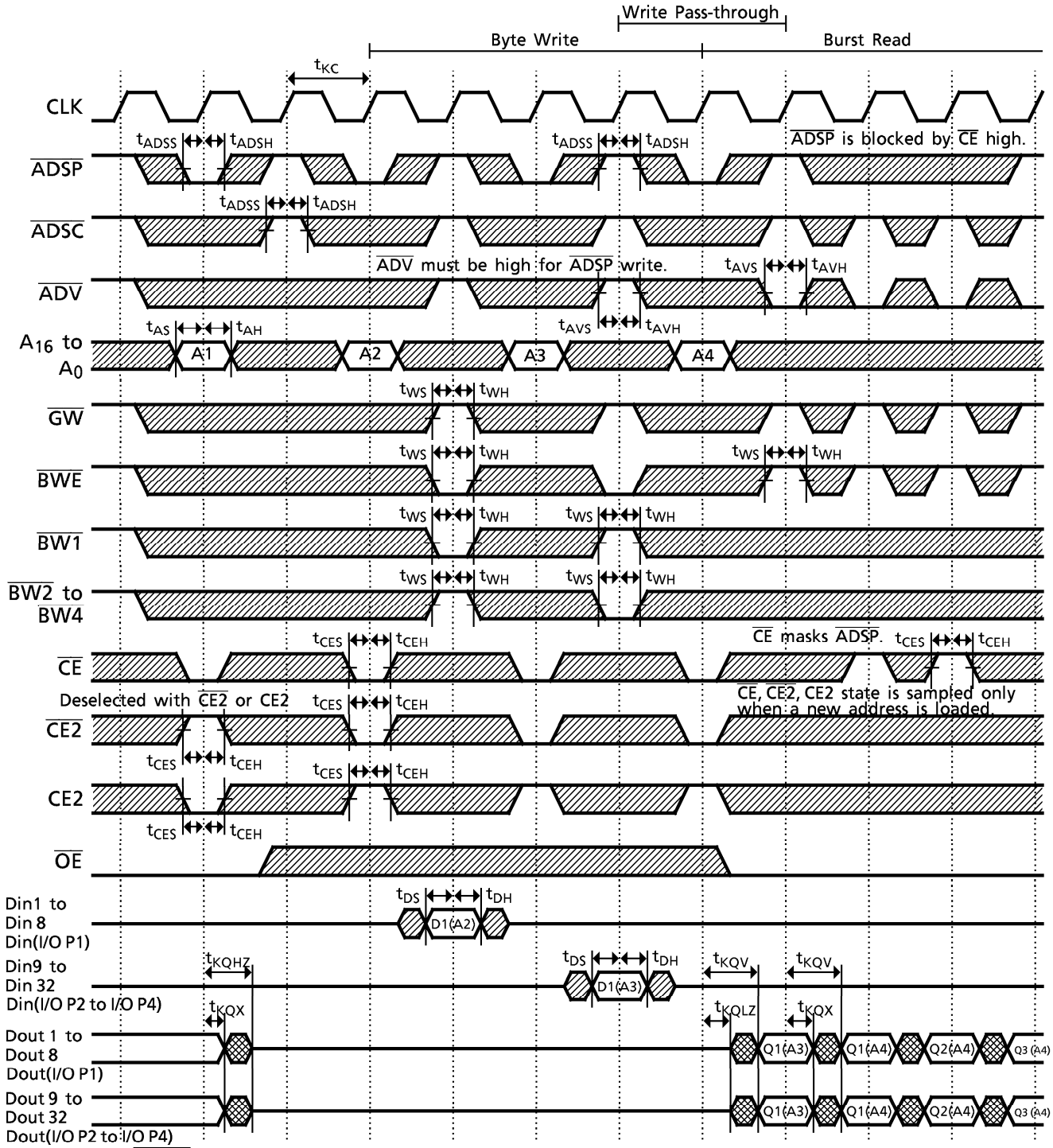
WRITE CYCLE



Note

1. D1(A2) represents input data for 1st burst address starting from address A2. D2(A2) represents input data for 2nd burst address starting from address A2.
2. ZZ is Low.

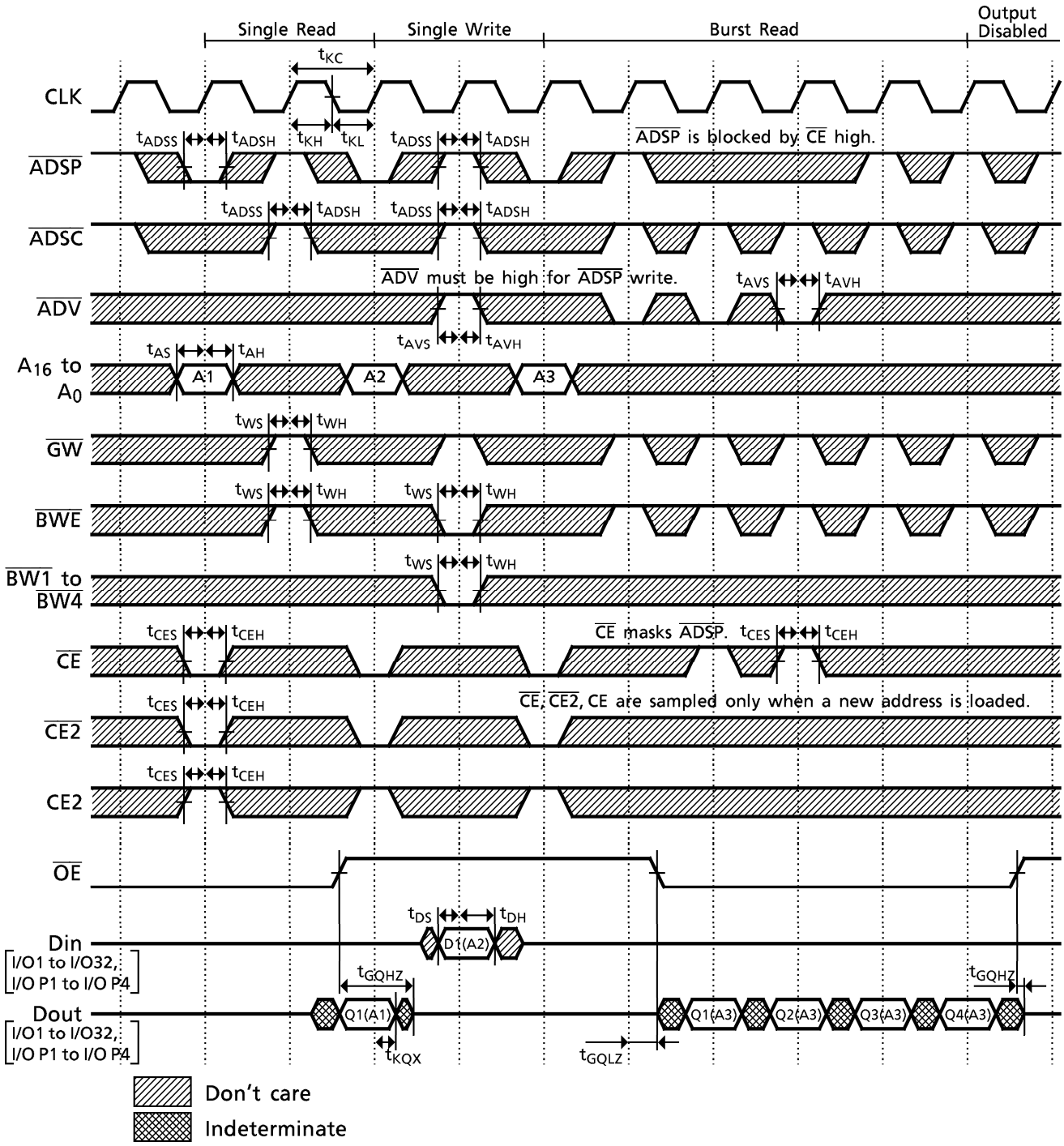
WRITE CYCLE (BYTE WRITE TIMING)



Note

1. ZZ is Low.

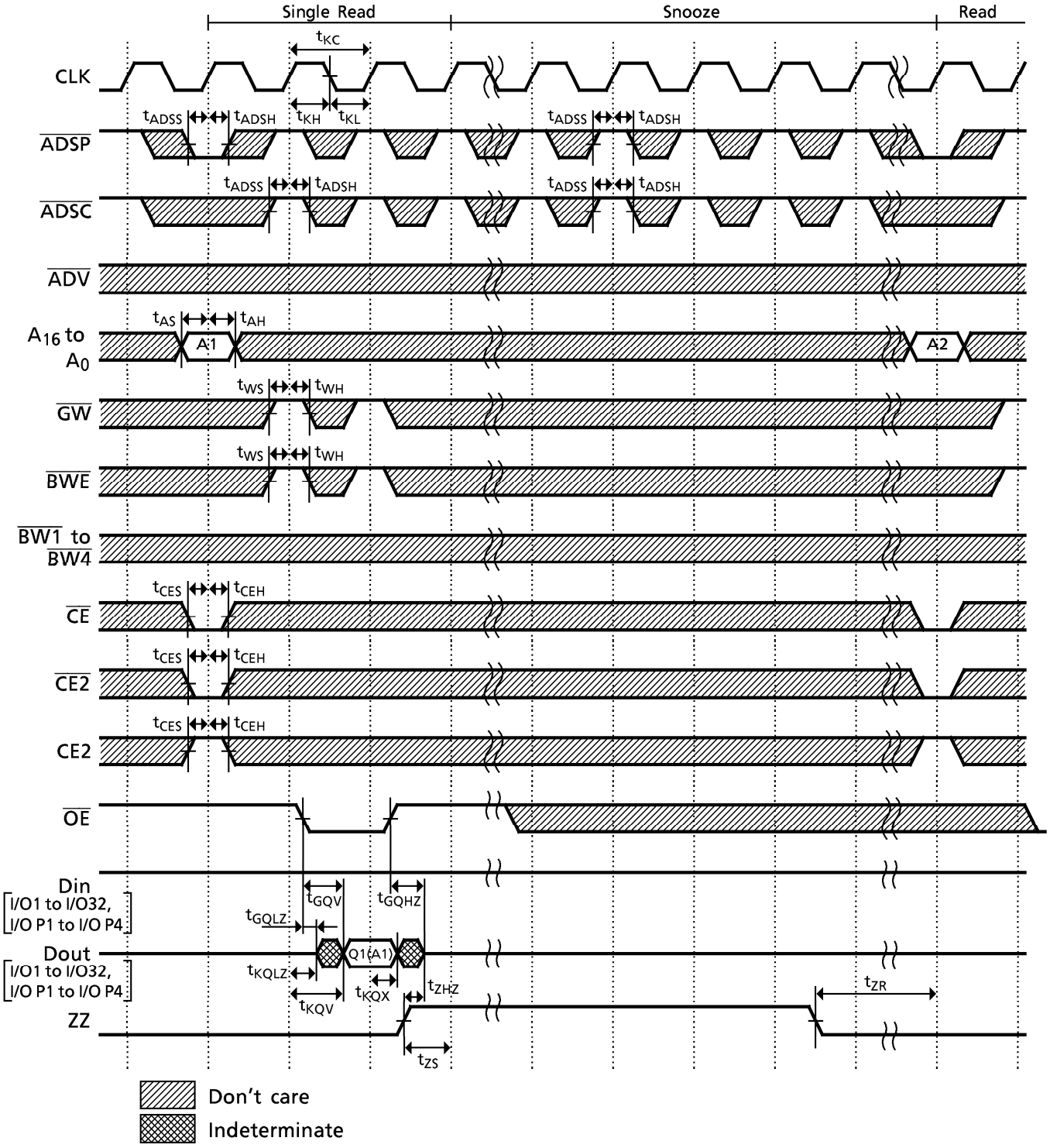
READ / WRITE CYCLE



Note

1. When a write operation follows a read operation, $\overline{OE}$ must be driven high prior to the assertion of the byte write enables ($\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$ to $\overline{BW4}$) and before input data is applied to avoid data bus contention.
2. ZZ is Low.

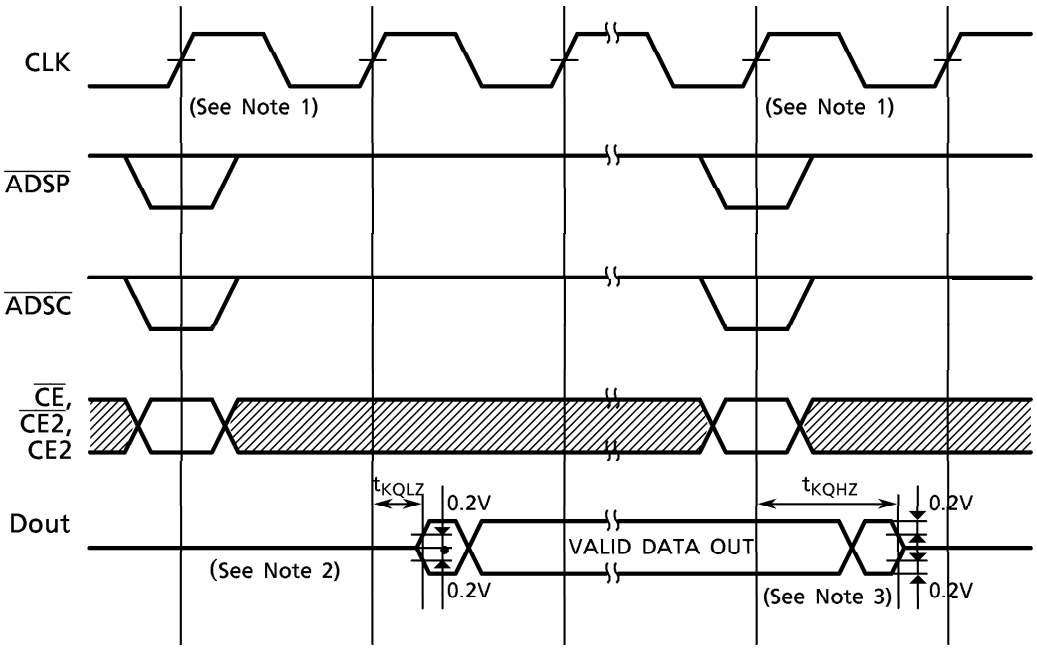
SNOOZE CYCLE



NOTE : 1. Do not apply opposite data polarity to the I/O pins when they are in the output state.

2. Output enable and output disable times are specified as follows using the output load shown in Fig. 1.

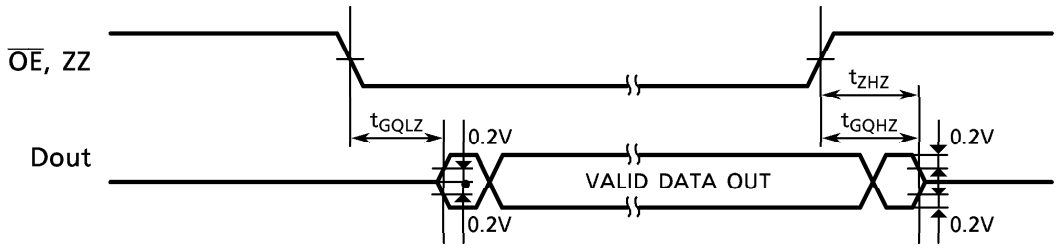
(a) t_{KQLZ}, t_{KQHZ}



Note:

1. Input states are defined in the Synchronous Input Truth Table.
2. If the device was previously deselected, when the device is selected, the output remains in a high impedance state in the present clock cycle regardless of $\overline{OE}$ because of the output enable delay register.
   Valid data appears in the second clock cycle when $\overline{OE}$ is low.
3. When the device is deselected, the output goes into a high impedance state in the present clock cycle regardless of $\overline{OE}$.

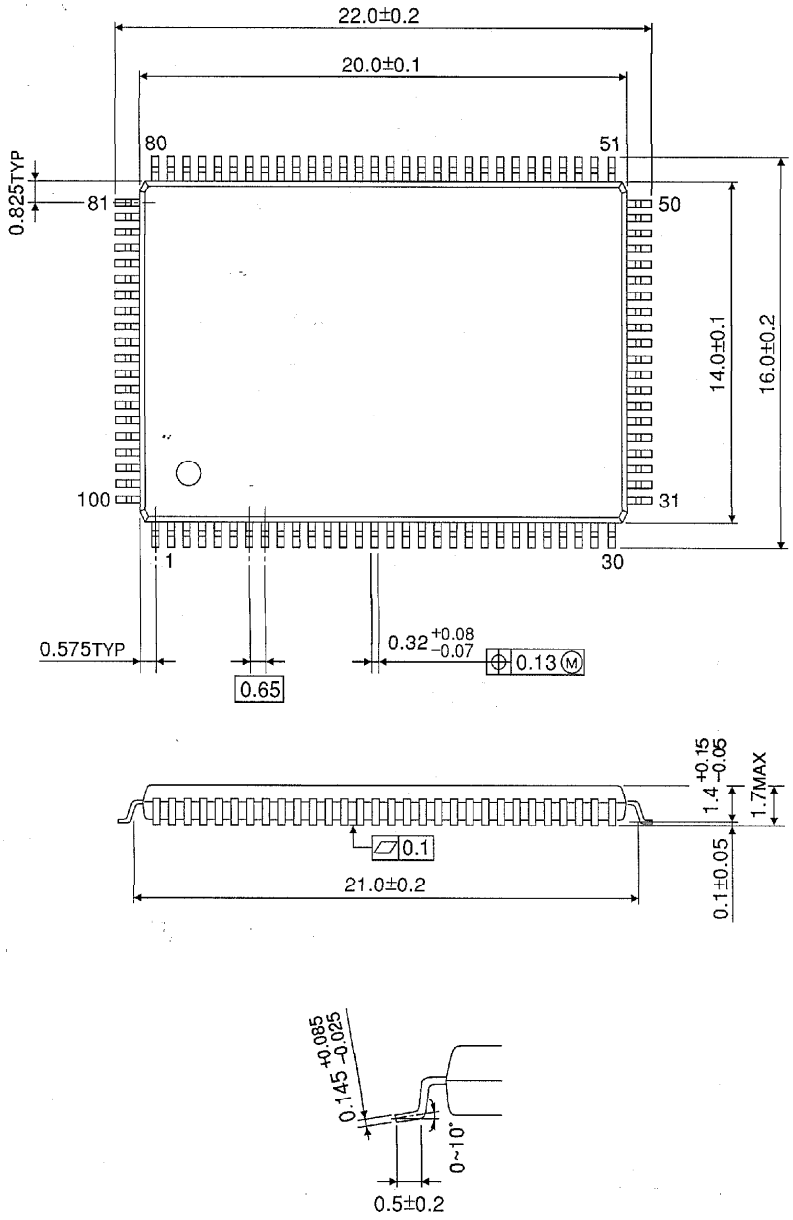
(b) t_{GQLZ}, t_{GQHZ}, t_{ZHZ}



PACKAGE DIMENSIONS

Plastic LQFP (LQFP100-P-1420-0.65K)

Unit in mm



Weight: 0.56 g (typ)