

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

## 2,097,152-WORD BY 8-BIT CMOS STATIC RAM

DESCRIPTION

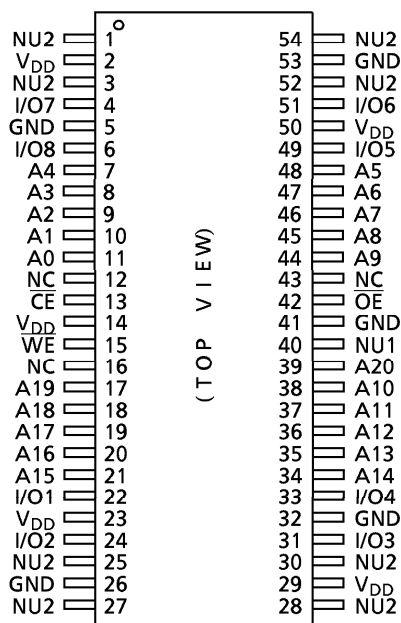
The TC55V8200FT is a 16,777,216-bit high-speed static random access memory (SRAM) organized as 2,097,152 words by 8 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable ( $\overline{CE}$ ) can be used to place the device in a low-power mode, and output enable ( $\overline{OE}$ ) provides fast memory access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55V8200FT is available in plastic 54-pin TSOP with 400mil width for high density surface assembly.

FEATURES

- Fast access time (the following are maximum values)
  - TC55V8200FT-10: 10 ns
  - TC55V8200FT-12: 12 ns
  - TC55V8200FT-15: 15 ns
- Low-power dissipation
 

| Cycle Time      | 10  | 12  | 15  | ns |
|-----------------|-----|-----|-----|----|
| Operation (max) | 430 | 400 | 370 | mA |
- Single power supply : 3.3V  $\pm$  5% (-10)  
: 3.3V  $\pm$  0.3V (-12, -15)
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using  $\overline{OE}$
- Package:  
TSOP II 54-P-400-0.80B(FT) (Weight: 0.55g typ)

Standby: 4mA (max)

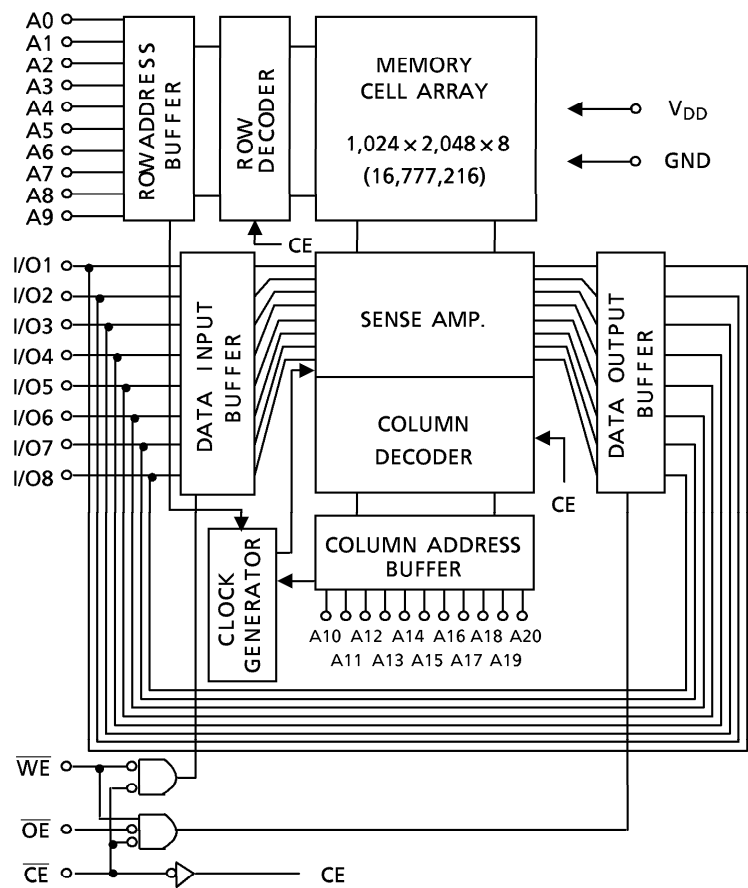
PIN ASSIGNMENTPIN NAMES

|                 |                       |
|-----------------|-----------------------|
| A0 to A20       | Address Inputs        |
| I/O1 to I/O8    | Data Inputs / Outputs |
| $\overline{CE}$ | Chip Enable Input     |
| $\overline{WE}$ | Write Enable Input    |
| $\overline{OE}$ | Output Enable Input   |
| V <sub>DD</sub> | Power (+ 3.3V)        |
| GND             | Ground                |
| NC              | No Connection         |
| NU1, NU2        | Not Usable            |

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BLOCK DIAGRAM



MAXIMUM RATINGS

| SYMBOL              | RATING                        | VALUE                             | UNIT |
|---------------------|-------------------------------|-----------------------------------|------|
| V <sub>DD</sub>     | Power Supply Voltage          | - 0.5 to 4.6                      | V    |
| V <sub>IN</sub>     | Input Terminal Voltage        | - 0.5* to 4.6                     | V    |
| V <sub>I/O</sub>    | Input/Output Terminal Voltage | - 0.5* to V <sub>DD</sub> + 0.5** | V    |
| P <sub>D</sub>      | Power Dissipation             | 1.8                               | W    |
| T <sub>solder</sub> | Soldering Temperature (10 s)  | 260                               | °C   |
| T <sub>strg</sub>   | Storage Temperature           | - 65 to 150                       | °C   |
| T <sub>opr</sub>    | Operating Temperature         | - 10 to 85                        | °C   |

\* : -1.5V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)  
\*\* : V<sub>DD</sub>+1.5V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

| SYMBOL          | PARAMETER            | MIN      | TYP   | MAX                     | UNIT |
|-----------------|----------------------|----------|-------|-------------------------|------|
| V <sub>DD</sub> | Power Supply Voltage | -10      | 3.135 | 3.465                   | V    |
|                 |                      | -12, -15 | 3.0   | 3.6                     |      |
| V <sub>IH</sub> | Input High Voltage   | 2.0      | -     | V <sub>DD</sub> + 0.3** | V    |
| V <sub>IL</sub> | Input Low Voltage    | - 0.3*   | -     | 0.8                     | V    |

\* : -1.0V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)  
\*\* : V<sub>DD</sub>+1.0V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)

**DC CHARACTERISTICS** ( $T_a = 0^\circ \text{ to } 70^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$  : -10,  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$  : -12,-15)

| SYMBOL       | PARAMETER                                 | TEST CONDITION                                                                                                       | MIN                       | TYP | MAX | UNIT          |
|--------------|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------|---------------------------|-----|-----|---------------|
| $I_{IL}$     | Input Leakage Current<br>(Except NU1 pin) | $V_{IN} = 0 \text{ to } V_{DD}$                                                                                      | -1                        | -   | 1   | $\mu\text{A}$ |
| $I_{LO}$     | Output Leakage Current                    | $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$<br>$V_{OUT} = 0 \text{ to } V_{DD}$ | -1                        | -   | 1   | $\mu\text{A}$ |
| $I_{I(NU1)}$ | Input Current<br>(NU1 pin)                | $V_{IN} = 0 \text{ to } 0.8\text{V}$                                                                                 | -1                        | -   | 20  | $\mu\text{A}$ |
|              |                                           | $V_{IN} = 0 \text{ to } 0.2\text{V}$                                                                                 | -1                        | -   | 1   |               |
| $V_{OH}$     | Output High Voltage                       | $I_{OH} = -2\text{mA}$                                                                                               | 2.4                       | -   | -   | V             |
|              |                                           | $I_{OH} = -100\mu\text{A}$                                                                                           | $V_{DD} - 0.2$            | -   | -   |               |
| $V_{OL}$     | Output Low Voltage                        | $I_{OL} = 2\text{mA}$                                                                                                | -                         | -   | 0.4 |               |
|              |                                           | $I_{OL} = 100\mu\text{A}$                                                                                            | -                         | -   | 0.2 |               |
| $I_{DDO}$    | Operating Current                         | $\overline{CE} = V_{IL}$ , $I_{out} = 0\text{mA}$<br>$\overline{OE} = V_{IH}$                                        | $t_{cycle} = 10\text{ns}$ | -   | 430 | mA            |
|              |                                           |                                                                                                                      | $t_{cycle} = 12\text{ns}$ | -   | 400 |               |
|              |                                           | Other Inputs = $V_{DD} - 0.2\text{V}$ or $0.2\text{V}$                                                               | $t_{cycle} = 15\text{ns}$ | -   | 370 |               |
| $I_{DDS1}$   | Standby Current                           | $\overline{CE} = V_{IH}$ , Other Inputs = $V_{IH}$ or $V_{IL}$                                                       | -                         | -   | 105 | mA            |
| $I_{DDS2}$   |                                           | $\overline{CE} = V_{DD} - 0.2\text{V}$<br>Other Inputs = $V_{DD} - 0.2\text{V}$ or $0.2\text{V}$                     | -                         | -   | 4   |               |

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

| SYMBOL    | PARAMETER                | TEST CONDITION         | MAX | UNIT |
|-----------|--------------------------|------------------------|-----|------|
| $C_{IN}$  | Input Capacitance        | $V_{IN} = \text{GND}$  | 6   | pF   |
| $C_{I/O}$ | Input/Output Capacitance | $V_{I/O} = \text{GND}$ | 8   | pF   |

Note: This parameter is periodically sampled and is not 100% tested.

**OPERATING MODE**

| MODE            | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O1 to I/O8   | POWER     |
|-----------------|-----------------|-----------------|-----------------|----------------|-----------|
| Read            | L               | L               | H               | Output         | $I_{DDO}$ |
| Write           | L               | X               | L               | Input          | $I_{DDO}$ |
| Outputs Disable | L               | H               | H               | High Impedance | $I_{DDO}$ |
| Standby         | H               | X               | X               | High Impedance | $I_{DDS}$ |

X : Don't care

Note: The NU1 and NU2 pins must be left unconnected or tied to GND or a voltage level of less than 0.8 V.  
You must not apply a voltage of more than 0.8 V to the NU1 and NU2.

**AC CHARACTERISTICS** ( $T_a = 0^\circ \text{ to } 70^\circ\text{C}$  <sup>(Note 1)</sup>,  $V_{DD} = 3.3\text{V} \pm 5\%$ :-10,  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ :-12,-15)  
**READ CYCLE**

| SYMBOL    | PARAMETER                                 | TC55V8200FT-10 |     | TC55V8200FT-12 |     | TC55V8200FT-15 |     | UNIT |
|-----------|-------------------------------------------|----------------|-----|----------------|-----|----------------|-----|------|
|           |                                           | MIN            | MAX | MIN            | MAX | MIN            | MAX |      |
| $t_{RC}$  | Read Cycle Time                           | 10             | –   | 12             | –   | 15             | –   | ns   |
| $t_{ACC}$ | Address Access Time                       | –              | 10  | –              | 12  | –              | 15  |      |
| $t_{CO}$  | Chip Enable Access Time                   | –              | 10  | –              | 12  | –              | 15  |      |
| $t_{OE}$  | Output Enable Access Time                 | –              | 5   | –              | 6   | –              | 8   |      |
| $t_{OH}$  | Output Data Hold Time from Address Change | 3              | –   | 3              | –   | 3              | –   |      |
| $t_{COE}$ | Output Enable Time from Chip Enable       | 3              | –   | 3              | –   | 3              | –   |      |
| $t_{OEE}$ | Output Enable Time from Output Enable     | 1              | –   | 1              | –   | 1              | –   |      |
| $t_{COD}$ | Output Disable Time from Chip Enable      | –              | 6   | –              | 7   | –              | 8   |      |
| $t_{ODO}$ | Output Disable Time from Output Enable    | –              | 6   | –              | 7   | –              | 8   |      |

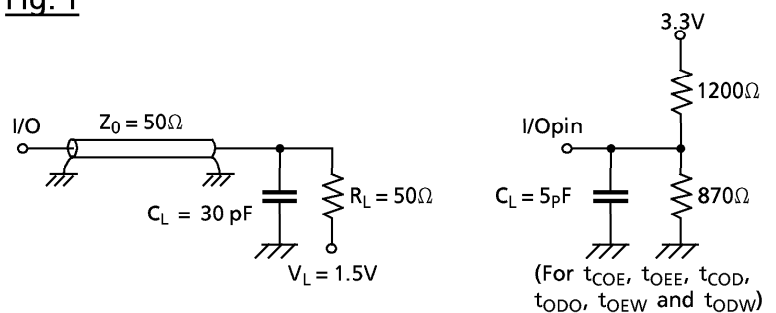
**WRITE CYCLE**

| SYMBOL    | PARAMETER                             | TC55V8200FT-10 |     | TC55V8200FT-12 |     | TC55V8200FT-15 |     | UNIT |
|-----------|---------------------------------------|----------------|-----|----------------|-----|----------------|-----|------|
|           |                                       | MIN            | MAX | MIN            | MAX | MIN            | MAX |      |
| $t_{WC}$  | Write Cycle Time                      | 10             | –   | 12             | –   | 15             | –   | ns   |
| $t_{WP}$  | Write Pulse Width                     | 7              | –   | 8              | –   | 10             | –   |      |
| $t_{CW}$  | Chip Enable to End of Write           | 8.5            | –   | 9              | –   | 11             | –   |      |
| $t_{AW}$  | Address Valid to End of Write         | 8.5            | –   | 9              | –   | 11             | –   |      |
| $t_{AS}$  | Address Setup Time                    | 0              | –   | 0              | –   | 0              | –   |      |
| $t_{WR}$  | Write Recovery Time                   | 0              | –   | 0              | –   | 0              | –   |      |
| $t_{DS}$  | Data Setup Time                       | 6              | –   | 7              | –   | 8              | –   |      |
| $t_{DH}$  | Data Hold Time                        | 0              | –   | 0              | –   | 0              | –   |      |
| $t_{OEW}$ | Output Enable Time from Write Enable  | 1              | –   | 1              | –   | 1              | –   |      |
| $t_{ODW}$ | Output Disable Time from Write Enable | –              | 6   | –              | 7   | –              | 8   |      |

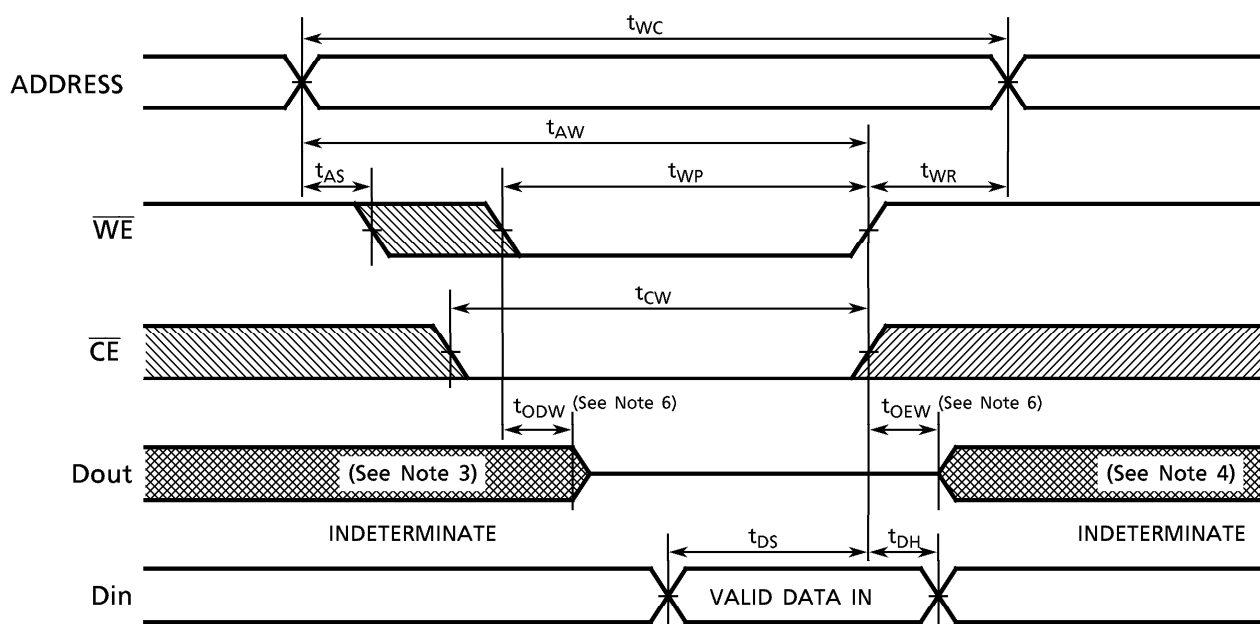
**AC TEST CONDITIONS**

|                                           |           |
|-------------------------------------------|-----------|
| Input Pulse Level                         | 3.0V/0.0V |
| Input Pulse Rise and Fall Time            | 2ns       |
| Input Timing Measurement Reference Level  | 1.5V      |
| Output Timing Measurement Reference Level | 1.5V      |
| Output Load                               | Fig. 1    |

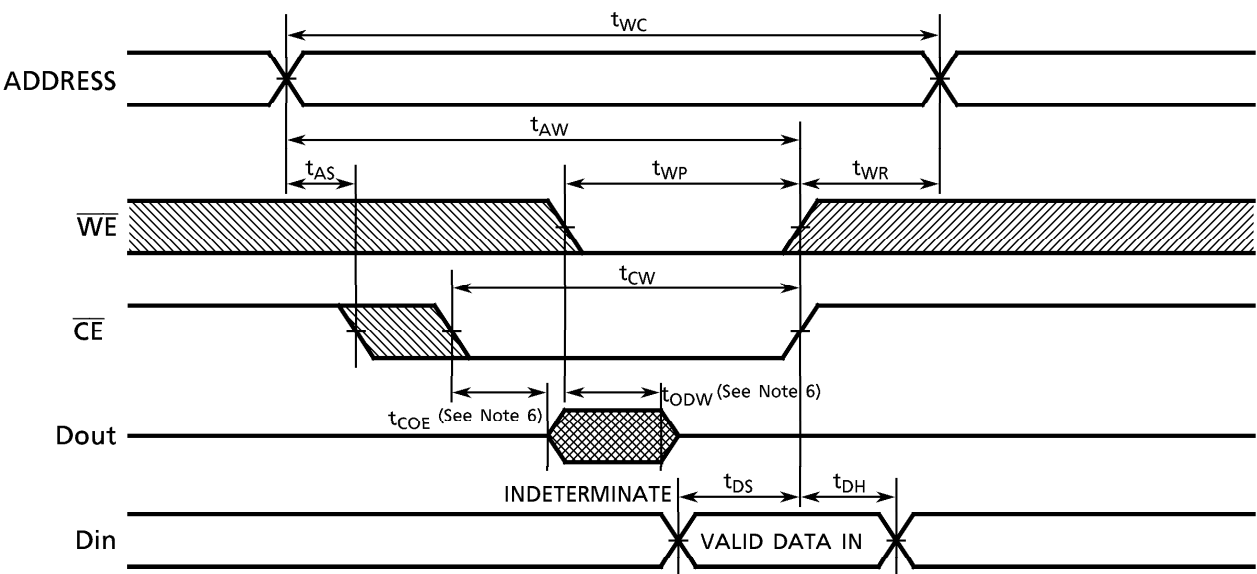
**Fig. 1**



**READ CYCLE** (See Note 2)



WRITE CYCLE 2 ( $\overline{\text{CE}}$  CONTROLLED) (See Note 5)



Note: (1) Operating temperature ( $T_a$ ) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2)  $\overline{WE}$  remains HIGH for the Read Cycle.

(3) If  $\overline{CE}$  goes LOW coincident with or after  $\overline{WE}$  goes LOW, the outputs will remain at high impedance.

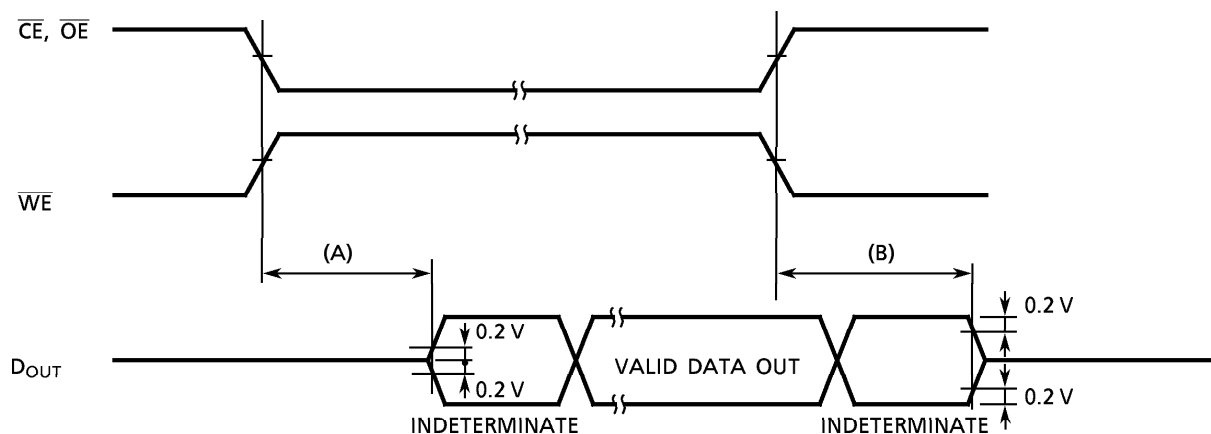
(4) If  $\overline{CE}$  goes HIGH coincident with or before  $\overline{WE}$  goes HIGH, the outputs will remain at high impedance.

(5) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A)  $t_{COE}, t_{OEE}, t_{OE\overline{W}}$  ..... Output Enable Time

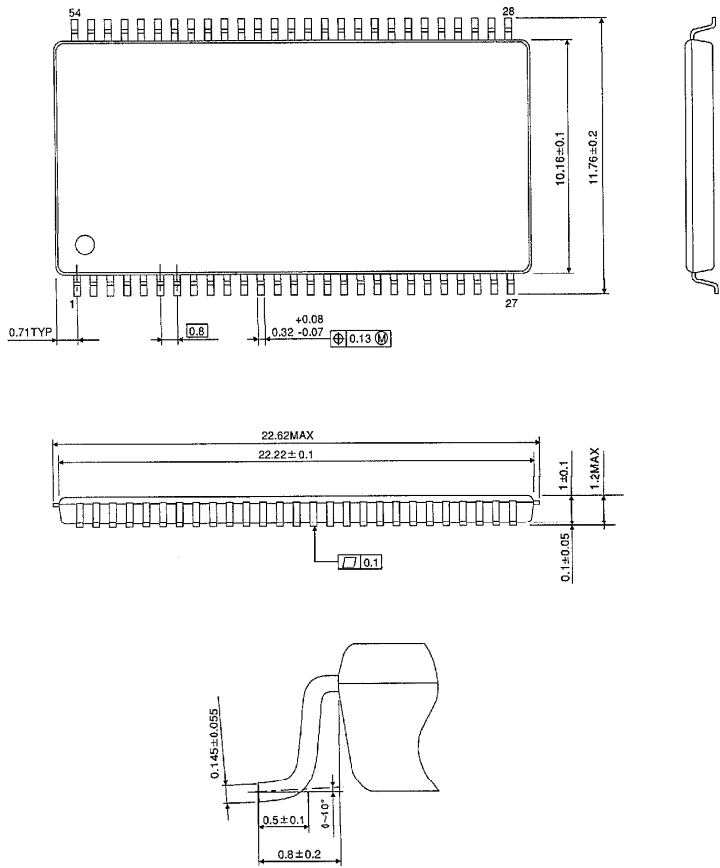
(B)  $t_{COD}, t_{ODO}, t_{OD\overline{W}}$  ..... Output Disable Time



PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 54-P-400-0.80B)

Unit in mm



Weight : 0.55g (Typ)