

TC74AC174P, TC74AC174F, TC74AC174FN, TC74AC174FT

HEX D – TYPE FLIP FLOP WITH CLEAR

The TC74AC174 is an advanced high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

When the $\overline{\text{CLR}}$ input is held low, the Q output are in the low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

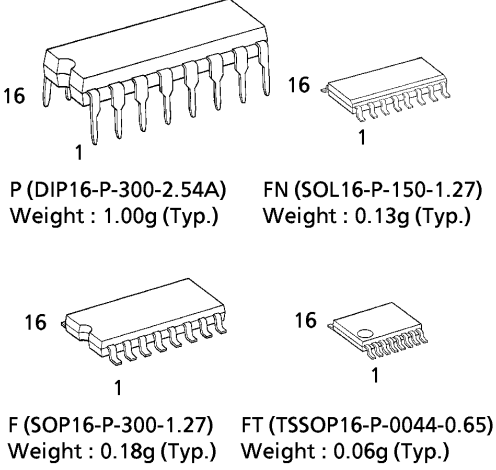
- High Speed..... $f_{\text{MAX}} = 180\text{MHz}(\text{typ.})$
at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^{\circ}\text{C}$
- High Noise Immunity..... $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}} (\text{Min.})$
- Symmetrical Output Impedance... $|I_{\text{OH}}| = I_{\text{OL}} = 24\text{mA}(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F174

TRUTH TABLE

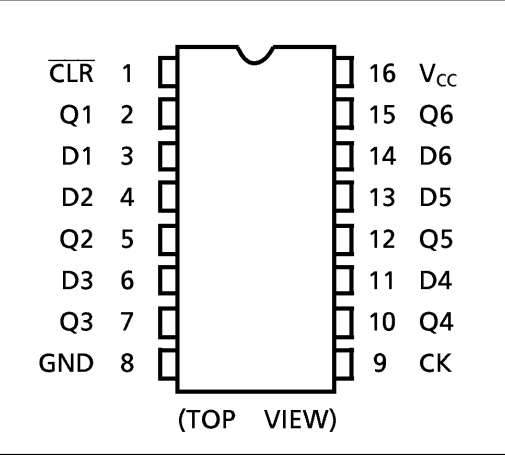
INPUTS			OUTPUTS	FUNCTION
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	CLEAR
H	L		L	—
H	H		H	—
H	X		Q_n	NO CHANGE

X : Don't Care

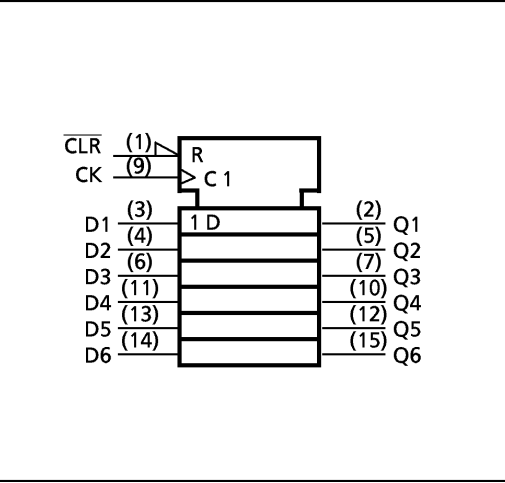
(Note) The JEDEC SOP (FN) is not available in Japan.



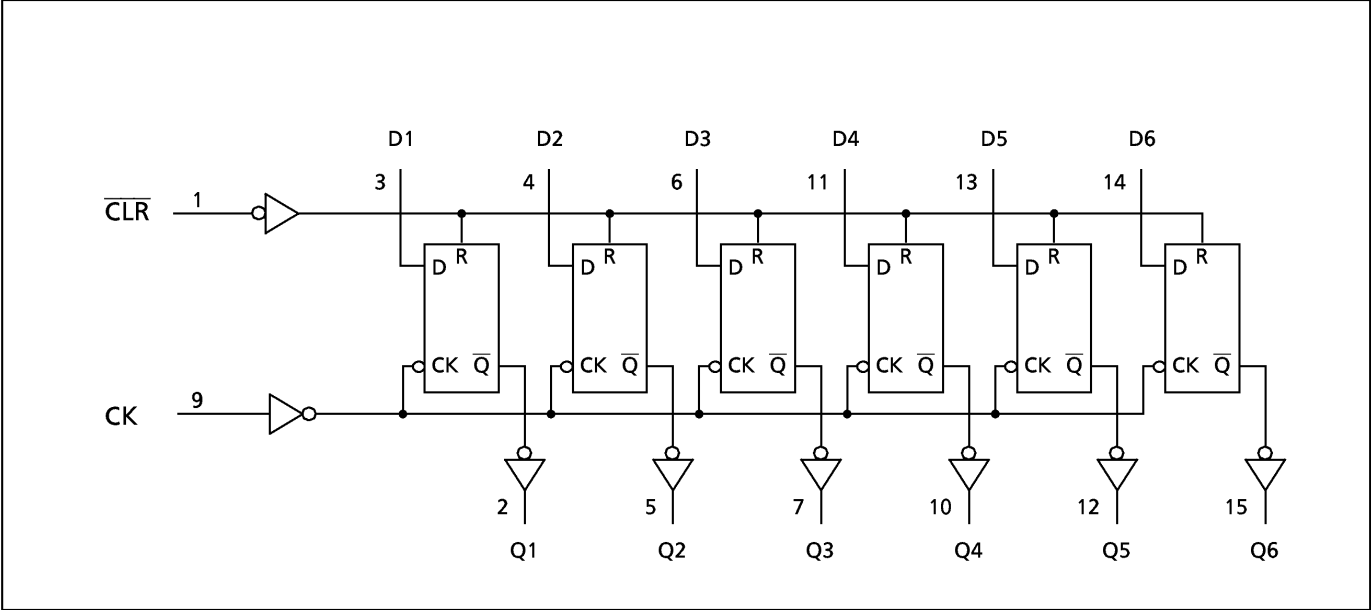
PIN ASSIGNMENT



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 150	mA
Power Dissipation	P_D	500 (DIP)*/ 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	dt/dV	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3\text{V}$) $0 \sim 20$ ($V_{CC} = 5 \pm 0.5\text{V}$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V _{IL}			2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I _{OH} = -4mA	3.0	2.58	—	—	2.48	—	
			I _{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I _{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 12mA	3.0	—	—	0.36	—	0.44	
			I _{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I _{OL} = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	8.0	—	80.0	

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = -40~85°C	UNIT
			V _{CC} (V)	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _W (L) t _W (H)		3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	ns
Minimum Pulse Width (CLR)	t _W (L)		3.3 ± 0.3 5.0 ± 0.5	7.0 5.0	7.0 5.0	
Minimum Set - up Time	t _s		3.3 ± 0.3 5.0 ± 0.5	7.0 4.0	7.0 4.0	
Minimum Hold Time	t _h		3.3 ± 0.3 5.0 ± 0.5	1.0 1.0	1.0 1.0	
Minimum Removal Time (CLR)	t _{rem}		3.3 ± 0.3 5.0 ± 0.5	6.0 3.5	6.0 3.5	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK—Q)	t _{pLH} t _{pHL}		3.3 ± 0.3	—	8.5	14.4	1.0	16.6	ns
			5.0 ± 0.5	—	6.7	9.6	1.0	11.0	
Propagation Delay Time ($\overline{\text{CLR}}$ —Q)	t _{pHL}		3.3 ± 0.3	—	8.2	13.9	1.0	16.0	ns
			5.0 ± 0.5	—	6.3	9.0	1.0	10.4	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	60	110	—	60	—	MHz
			5.0 ± 0.5	90	150	—	90	—	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	74	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

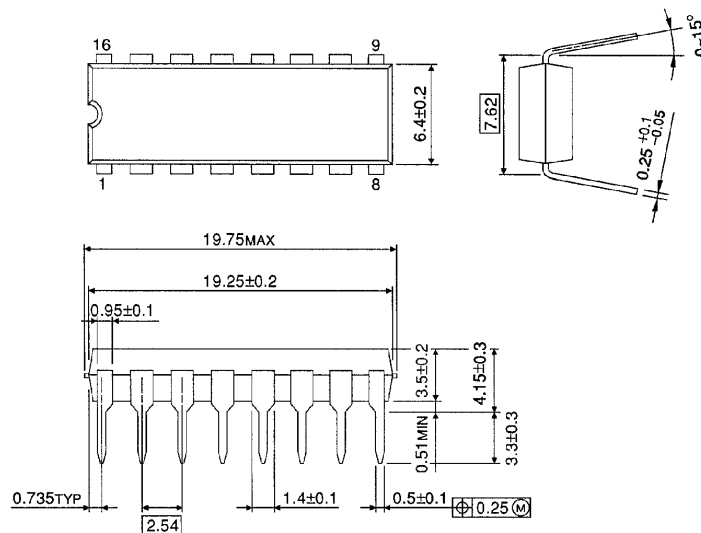
$$I_{\text{CC}}(\text{opr.}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}} / 6 \text{ (per F/F)}$$

And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation

$$C_{\text{PD}}(\text{total}) = 34 + 40 \cdot n$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

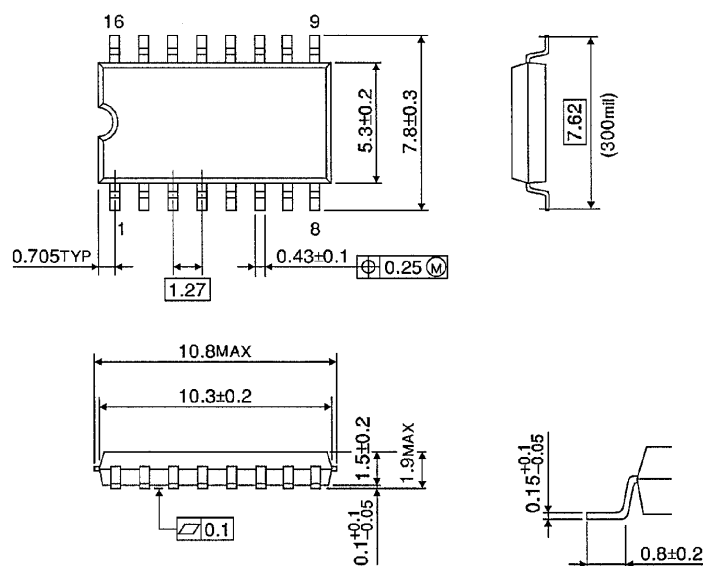
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

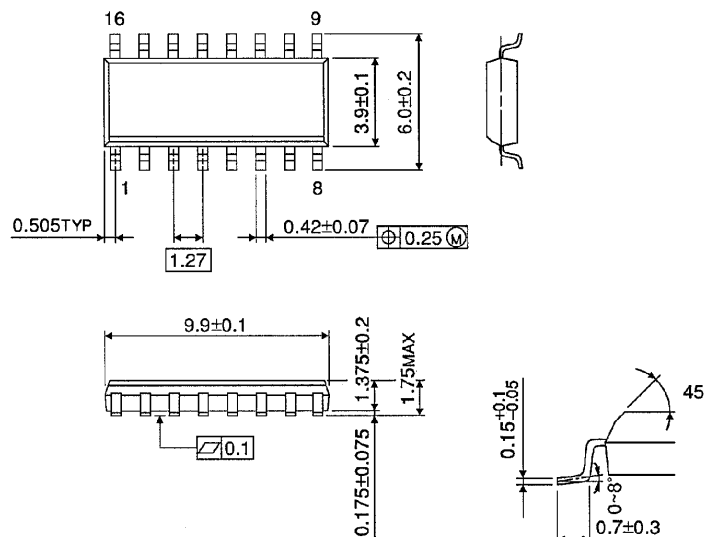


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm

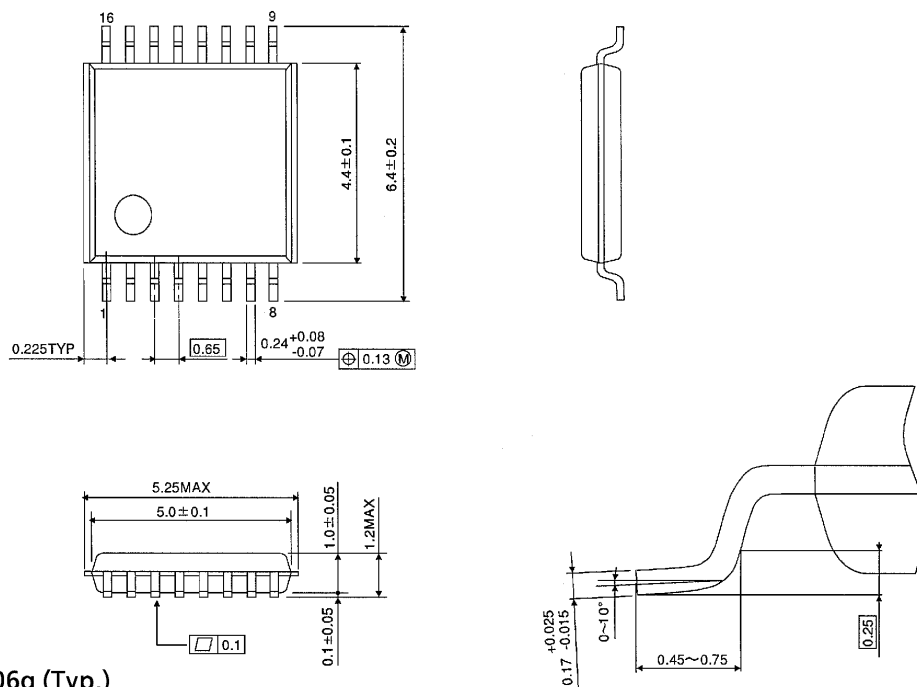
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)

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000707EBA

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