

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC279AP, TC74HC279AF

QUAD $\bar{S}$ - $\bar{R}$ LATCH

The TC74HC279A is a high speed CMOS QUAD S - R LATCH fabricated with silicon gate C²MOS technology.

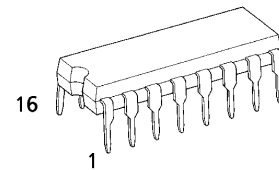
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Each latch has an independent Q output and Set and Reset inputs. $\bar{S}$ and $\bar{R}$ are active low. When $\bar{S}$ input is low, the Q output goes high and when $\bar{R}$ input is low, the Q output goes low. When both $\bar{S}$ and $\bar{R}$ are low, $\bar{S}$ takes precedence resulting Q=low. When both of $\bar{S}$ and $\bar{R}$ are held high, Q output doesn't change.

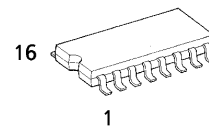
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed..... $t_{pd} = 12\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 2\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS279

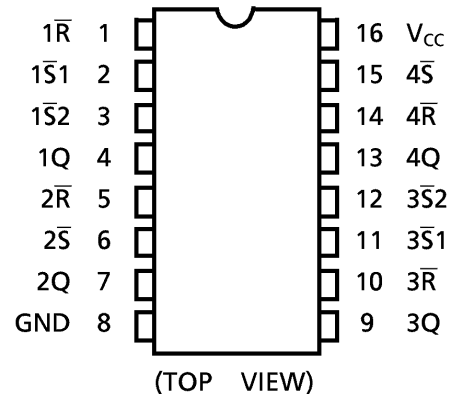


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



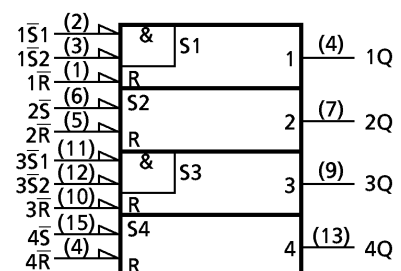
TRUTH TABLE

INPUTS		OUTPUTS
S #	$\bar{R}$	Q
H	H	Qn
L	H	H
H	L	L
L	L	H

NOTE :

Qn -- The level of Q before the indicated input condition were established.
-- For latches with doubles $\bar{S}$ input.
H=Both $\bar{S}$ input high
L=One of both inputs low

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V
			4.5	3.15	—	—	3.15	—	
			6.0	4.20	—	—	4.20	—	
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V
			4.5	—	—	1.35	—	1.35	
			6.0	—	—	1.80	—	1.80	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	V
				4.5	4.4	4.5	—	4.4	
		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$		6.0	5.9	6.0	—	5.9	
				4.5	4.18	4.31	—	4.13	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	V
				4.5	—	0.0	0.1	—	
		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 5.2 \text{ mA}$		6.0	—	0.0	0.1	—	
				4.5	—	0.17	0.26	—	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$		6.0	—	—	± 0.1	—	μA
				6.0	—	—	2.0	—	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$		6.0	—	—	2.0	—	20.0

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time ($\bar{S}1, \bar{S}2 - Q$)	t_{PLH} t_{PHL}		—	12	22	
Propagation Delay Time ($\bar{S} - Q$)	t_{PLH} t_{PHL}		—	9	17	
Propagation Delay Time ($\bar{R} - Q$)	t_{PLH} t_{PHL}		—	11	20	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

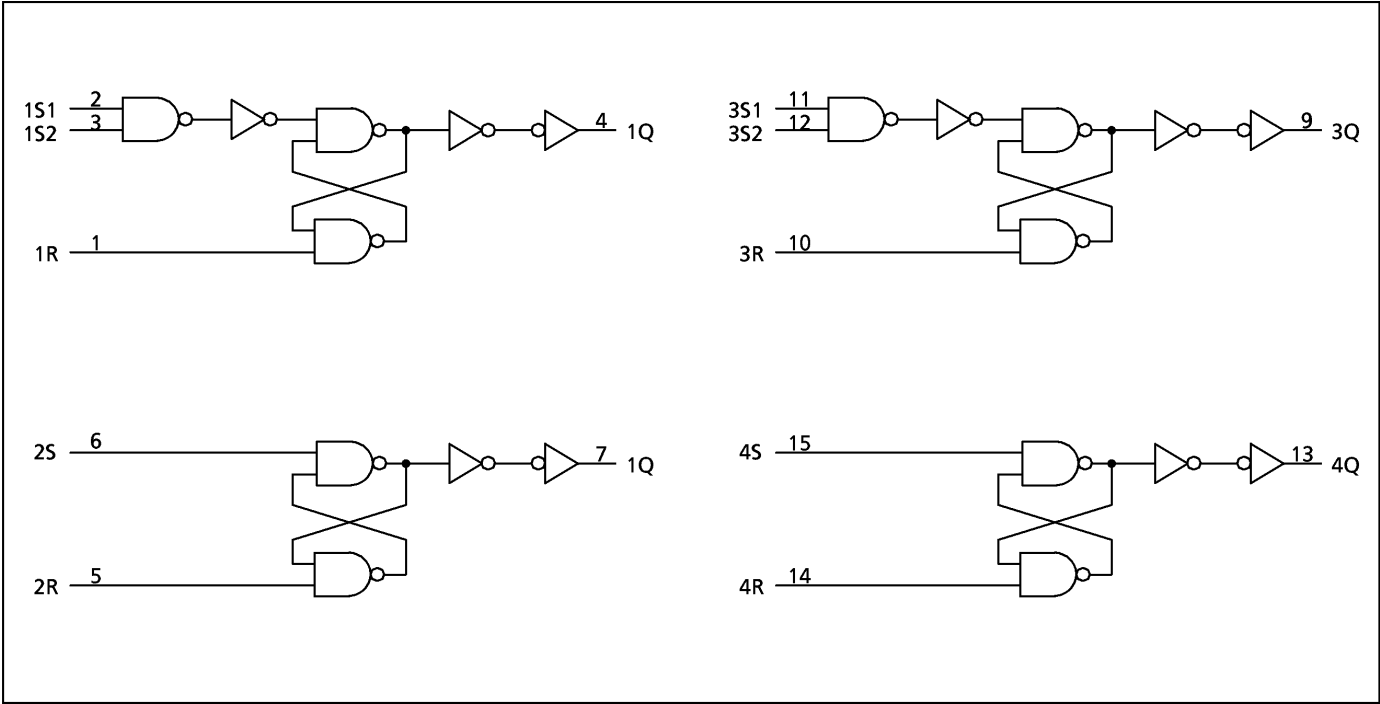
PARAMETER	SYMBOL	TEST CONDITION	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
			$V_{CC}(\text{V})$	MIN.	TYP.	MAX.	MIN.	MAX.
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time ($\bar{S}1, \bar{S}2 - Q$)	t_{PLH} t_{PHL}		2.0	—	45	130	—	165
			4.5	—	15	26	—	33
			6.0	—	13	22	—	28
Propagation Delay Time ($\bar{S} - Q$)	t_{PLH} t_{PHL}		2.0	—	38	100	—	125
			4.5	—	12	20	—	25
			6.0	—	10	17	—	21
Propagation Delay Time ($\bar{R} - Q$)	t_{PLH} t_{PHL}		2.0	—	42	120	—	150
			4.5	—	14	24	—	30
			6.0	—	12	20	—	26
Input Capacitance	C_{IN}			—	5	10	—	10
Power Dissipation Capacitance	$C_{PD}(1)$			—	18	—	—	—

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

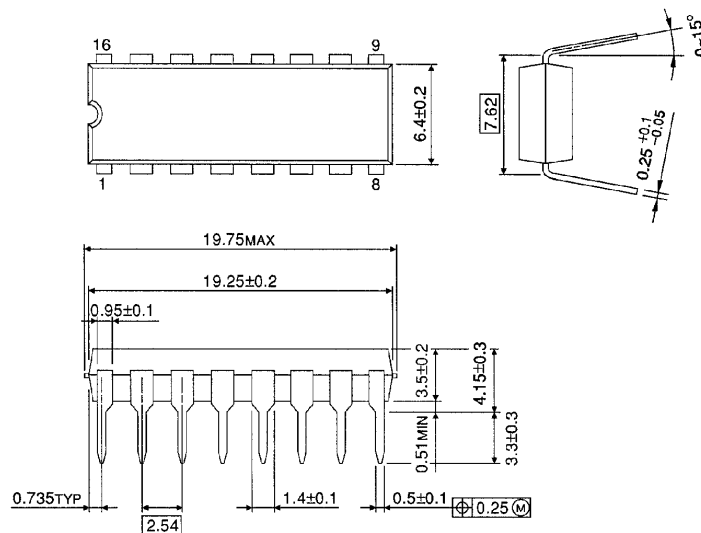
$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per circuit)}$$

SYSTEM DIAGRAM



DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

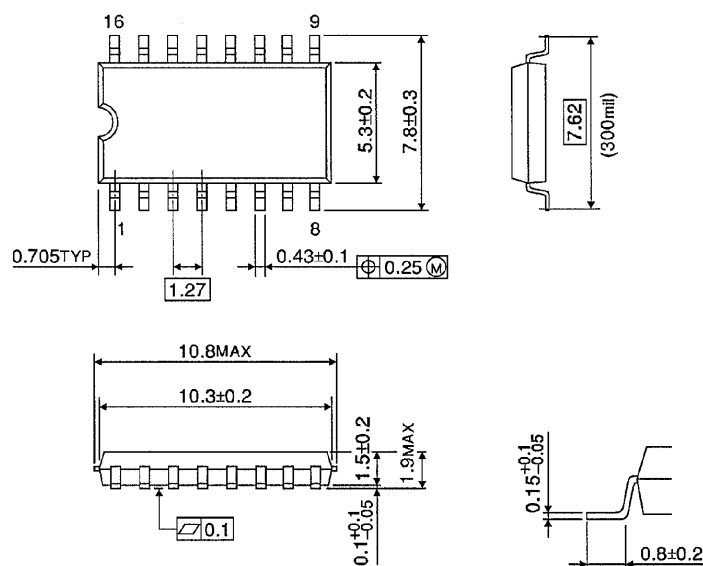
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)

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