

TC74LVX86F, TC74LVX86FN, TC74LVX86FT

Quad Exclusive OR Gate

The TC74LVX86F/ FN/ FT is a high-speed CMOS exclusive OR gate fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

The internal circuit includes an output buffer, which provides high noise immunity and stable output.

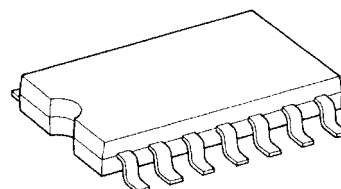
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High-speed: $t_{pd} = 5.8 \text{ ns (typ.)}$ ($V_{CC} = 3.3 \text{ V}$)
- Low power dissipation: $I_{CC} = 2 \text{ } \mu\text{A (max)}$ ($T_a = 25^\circ\text{C}$)
- Input voltage level: $V_{IL} = 0.8 \text{ V (max)}$ ($V_{CC} = 3 \text{ V}$)
 $V_{IH} = 2.0 \text{ V (min)}$ ($V_{CC} = 3 \text{ V}$)
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Low noise: $V_{OLP} = 0.5 \text{ V (max)}$
- Pin and function compatible with 74HC86

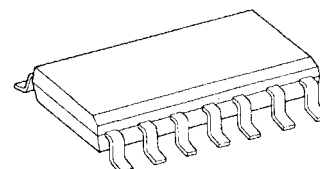
Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74LVX86F



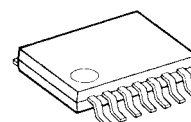
SOP14-P-300-1.27

TC74LVX86FN



SOL14-P-150-1.27

TC74LVX86FT



TSSOP14-P-0044-0.65

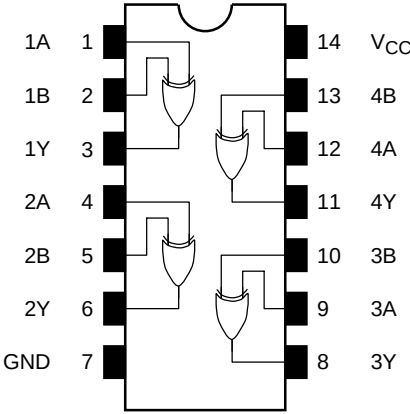
Weight

SOP14-P-300-1.27: 0.18 g (typ.)

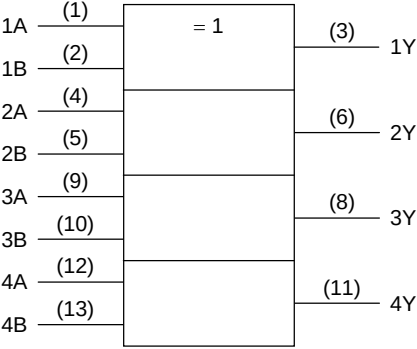
SOL14-P-150-1.27: 0.12 g (typ.)

TSSOP14-P-0044-0.65: 0.06 g (typ.)

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	−0.5 to 7.0	V
DC input voltage	V _{IN}	−0.5 to 7.0	V
DC output voltage	V _{OUT}	−0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	−20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	±25	mA
DC V _{CC} /ground current	I _{CC}	±50	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	−65 to 150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 3.6	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature	T _{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Electrical Characteristics
DC Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C				Ta = -40 to 85°C		Unit
					V _{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	H-level	V _{IH}	—	2.0	1.5	—	—	1.5	—	V	
				3.0	2.0	—	—	2.0	—		
				3.6	2.4	—	—	2.4	—		
	L-level	V _{IL}	—	2.0	—	—	0.5	—	0.5		
				3.0	—	—	0.8	—	0.8		
				3.6	—	—	0.8	—	0.8		
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V
			I _{OH} = -50 μA	3.0	2.9	3.0	—	2.9	—		
			I _{OH} = -4 mA	3.0	2.58	—	—	2.48	—		
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0	0.1	—	0.1	
			I _{OL} = 50 μA	3.0	—	0	0.1	—	0.1		
			I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44		
Input leakage current		I _{IN}	V _{IN} = 5.5 V or GND	3.6	—	—	±0.1	—	±1.0	μA	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND	3.6	—	—	2.0	—	20.0	μA	

AC Characteristics (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time	t _{pLH}	—	2.7	15	—	7.5	14.5	1.0	17.5	ns
				50	—	10.0	18.0	1.0	21.0	
	t _{pHL}		3.3 ± 0.3	15	—	5.8	9.3	1.0	11.0	
				50	—	8.3	12.8	1.0	14.5	
Output to output skew	t _{oSLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t _{oSHL}		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C _{IN}	(Note 2)			—	4	10	—	10	pF
Power dissipation capacitance	C _{PD}	(Note 3)			—	18	—	—	—	pF

Note 1: Parameter guaranteed by design.
 (t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)

Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

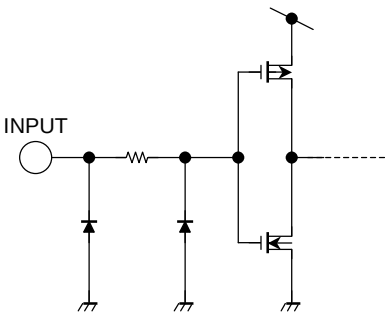
Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

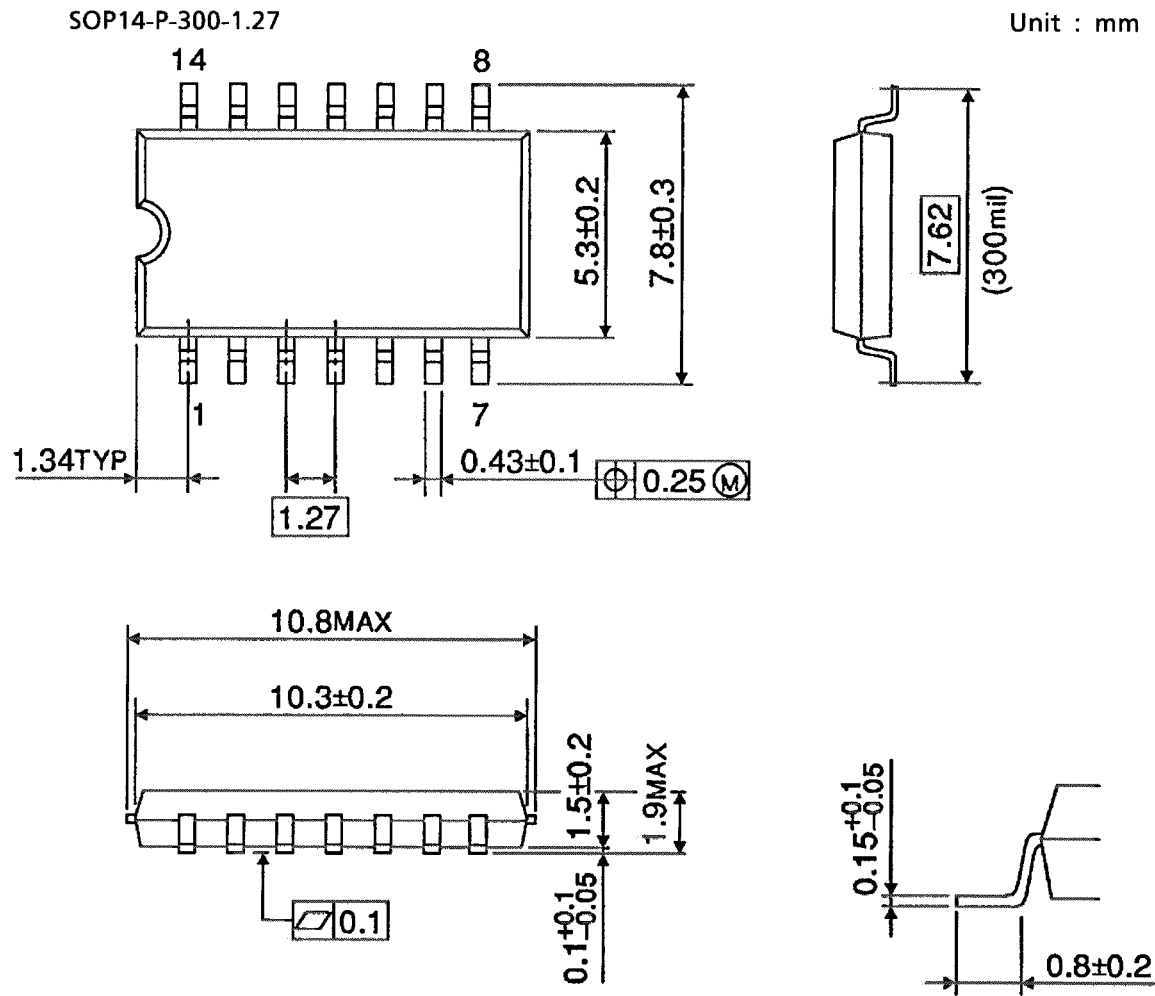
Noise Characteristics (Ta = 25°C, input: tr = tf = 3 ns, CL = 50 pF)

Characteristics		Symbol	Test Condition		Typ.	Limit	Unit
				V _{CC} (V)			
Quiet output maximum dynamic	V _{OL}	V _{OLP}	—	3.3	0.3	0.5	V
Quiet output minimum dynamic	V _{OL}	V _{OLV}	—	3.3	−0.3	−0.5	V
Minimum high level dynamic input voltage	V _{IH}	V _{IHD}	—	3.3	—	2.0	V
Maximum low level dynamic input voltage	V _{IL}	V _{ILD}	—	3.3	—	0.8	V

Input Equivalent Circuit



Package Dimensions

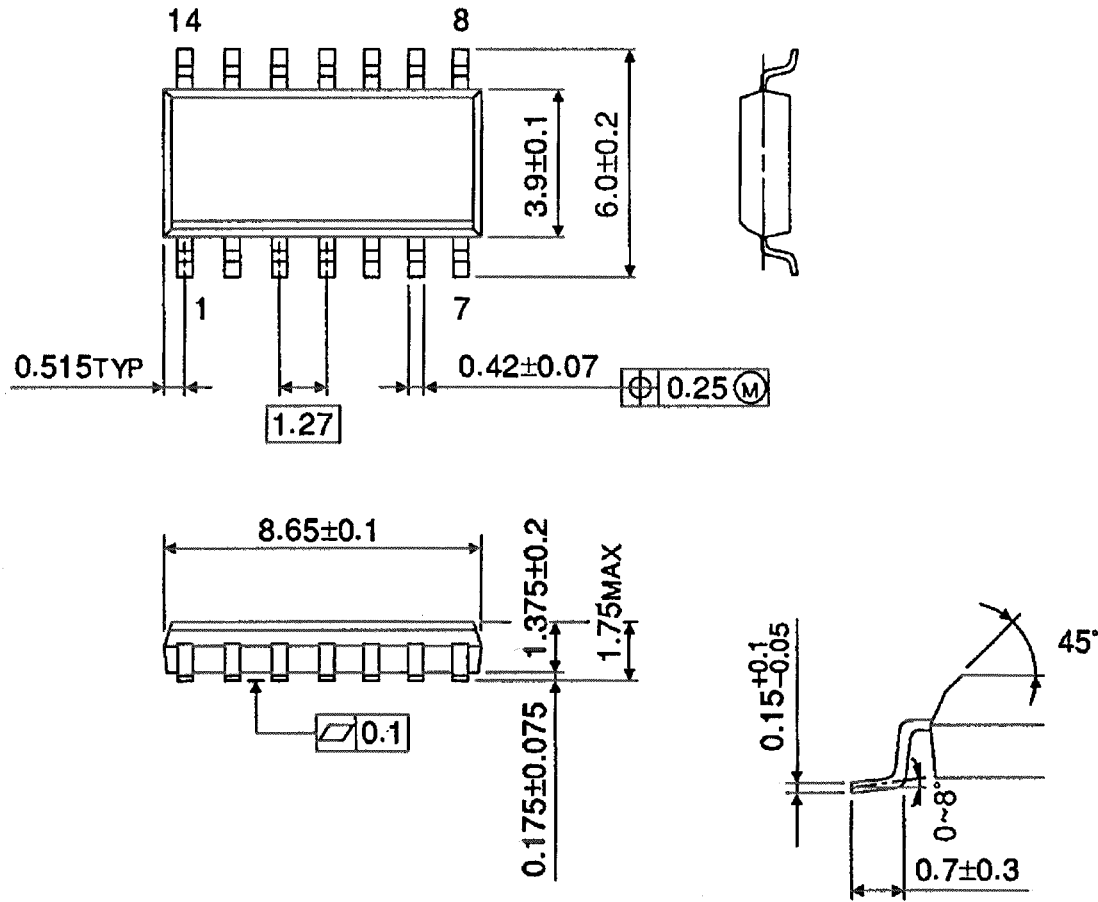


Weight: 0.18 g (typ.)

Package Dimensions

SOL14-P-150-1.27

Unit : mm

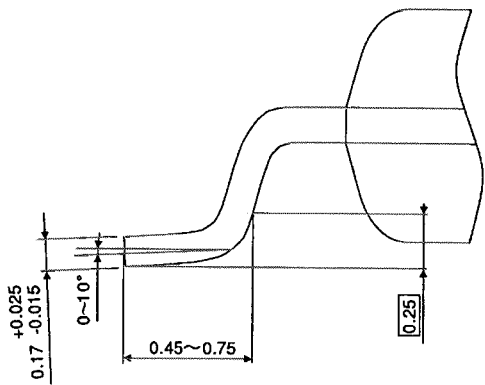
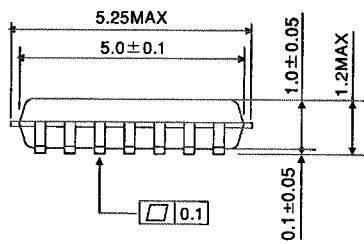
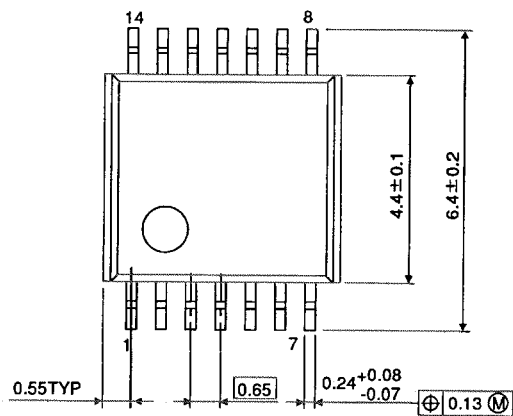


Weight: 0.12 g (typ.)

Package Dimensions

TSSOP14-P-0044-0.65

Unit : mm



Weight: 0.06 g (typ.)

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