

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC08F, TC74VHC08FN, TC74VHC08FT

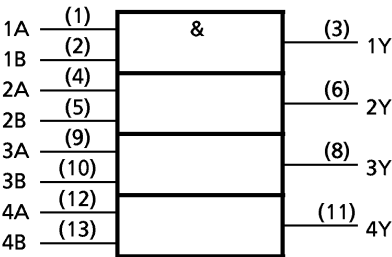
QUAD 2-INPUT AND GATE

The TC74VHC08 is an advanced high speed CMOS 2-INPUT AND GATE fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

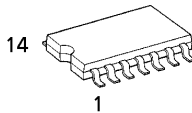
The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output. An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface from 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

- FEATURES :
- High Speed..... $t_{pd} = 4.3ns(typ.)$ at $V_{CC} = 5V$
 - Low Power Dissipation..... $I_{CC} = 2\mu A(Max.)$ at $T_a = 25^{\circ}C$
 - High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (Min.)$
 - Power Down Protection is provided on all inputs.
 - Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
 - Wide Operating Voltage Range.... $V_{CC} (opr) = 2V \sim 5.5V$
 - Low Noise $V_{OLP} = 0.8V (Max.)$
 - Pin and Function Compatible with 74ALS08

IEC LOGIC SYMBOL

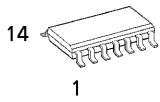


(Note) The JEDEC SOP (FN) is not available in Japan.



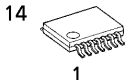
14
1

F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



14
1

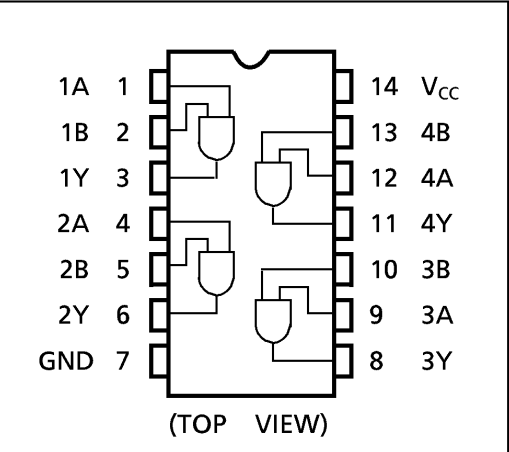
FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)



14
1

FT (TSSOP14-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT



TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	dt/dv	0~100 ($V_{CC} = 3.3 \pm 0.3\text{V}$) 0~20 ($V_{CC} = 5 \pm 0.5\text{V}$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 3.0~5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V
Low - Level Input Voltage	V_{IL}		2.0 3.0~5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$	$I_{OH} = -50\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	1.9 2.9 4.4	— — —	V
			$I_{OH} = -4\text{mA}$	3.0	2.58	—	2.48	—	
			$I_{OH} = -8\text{mA}$	4.5	3.94	—	3.80	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	— — —	0.1 0.1 0.1	V
			$I_{OL} = 4\text{mA}$	3.0	—	—	0.36	—	
			$I_{OL} = 8\text{mA}$	4.5	—	—	0.36	0.44	
Input Leakage Current	I_{IN}	$V_{IN} = 5.5\text{V or GND}$	0~5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	5.5	—	—	2.0	—	20.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

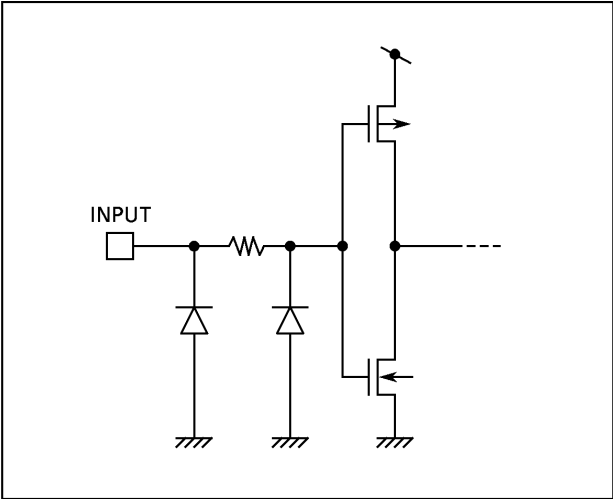
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT	
		V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.		
Propagation Delay Time	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	6.2	8.8	1.0	10.5	ns
				50	—	8.7	12.3	1.0	14.0	
			5.0 ± 0.5	15	—	4.3	5.9	1.0	7.0	
				50	—	5.8	7.9	1.0	9.0	
Input Capacitance	C _{I N}				—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 1)			—	18	—	—	—	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :
 $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4$ (per Gate)

NOISE CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

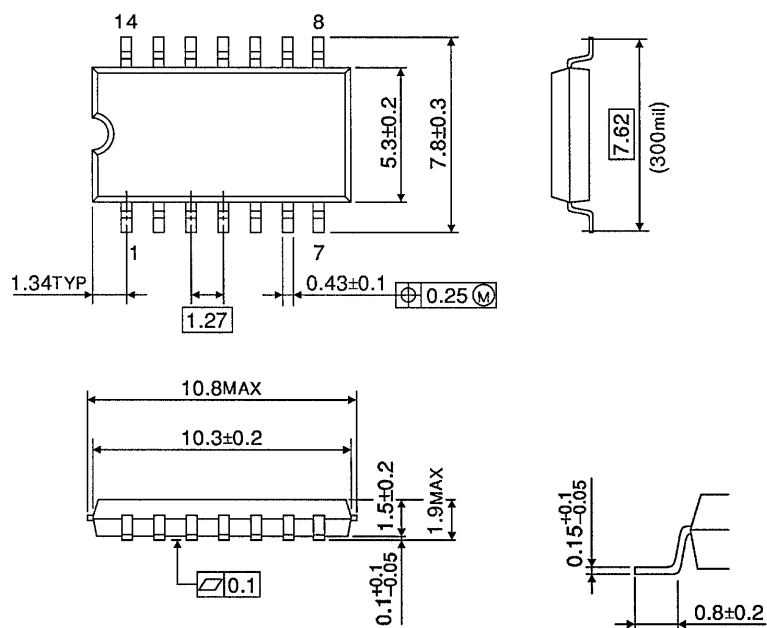
PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
				V _{CC} (V)	TYP. LIMIT	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	− 0.3	− 0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

INPUT PROTECTION CIRCUIT



SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm

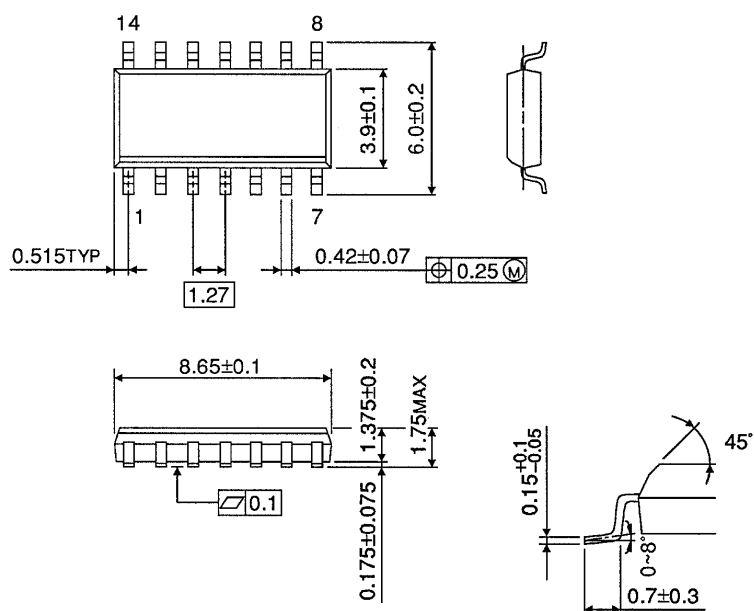


Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOP14-P-150-1.27)

Unit in mm

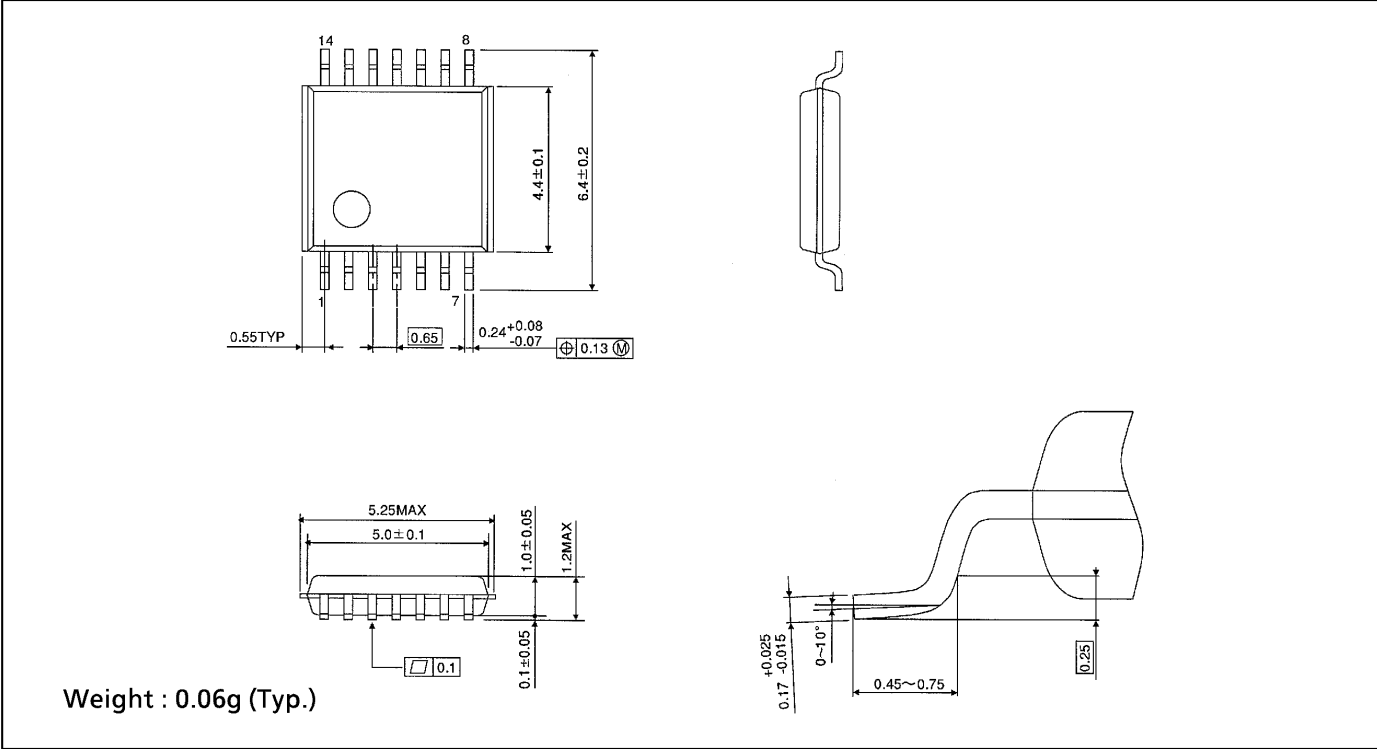
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

TSSOP 14PIN PACKAGE DIMENSIONS (TSSOP14-P-0044-0.65)

Unit in mm



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000707EBA

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