

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC574F, TC74VHC574FW, TC74VHC574FT

OCTAL D - TYPE FLIP - FLOP WITH 3 - STATE OUTPUT

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74VHC574 is advanced high speed CMOS OCTAL FLIP - FLOP with 3 - STATE OUTPUT fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

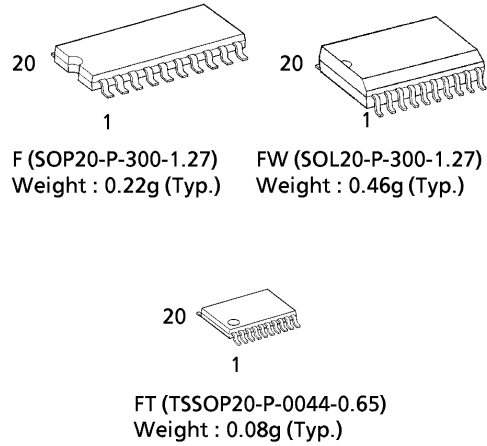
This 8 - bit D - type flip - flop is controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

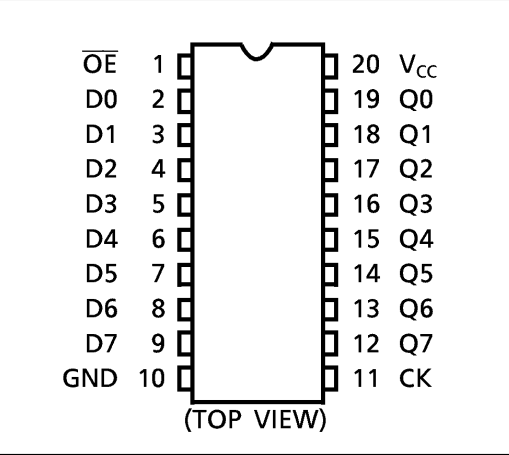
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

- High Speed..... $f_{MAX} = 180MHz(typ.)$
at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A(Max.)$ at $T_a = 25^{\circ}C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (Min.)$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Wide Operating Voltage Range.... $V_{CC} (opr) = 2V \sim 5.5V$
- Low Noise $V_{OLP} = 1.2V (Max.)$
- Pin and Function Compatible with 74ALS574



PIN ASSIGNMENT

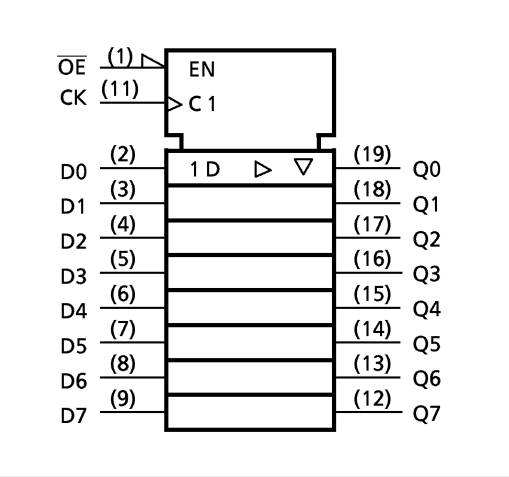


TRUTH TABLE

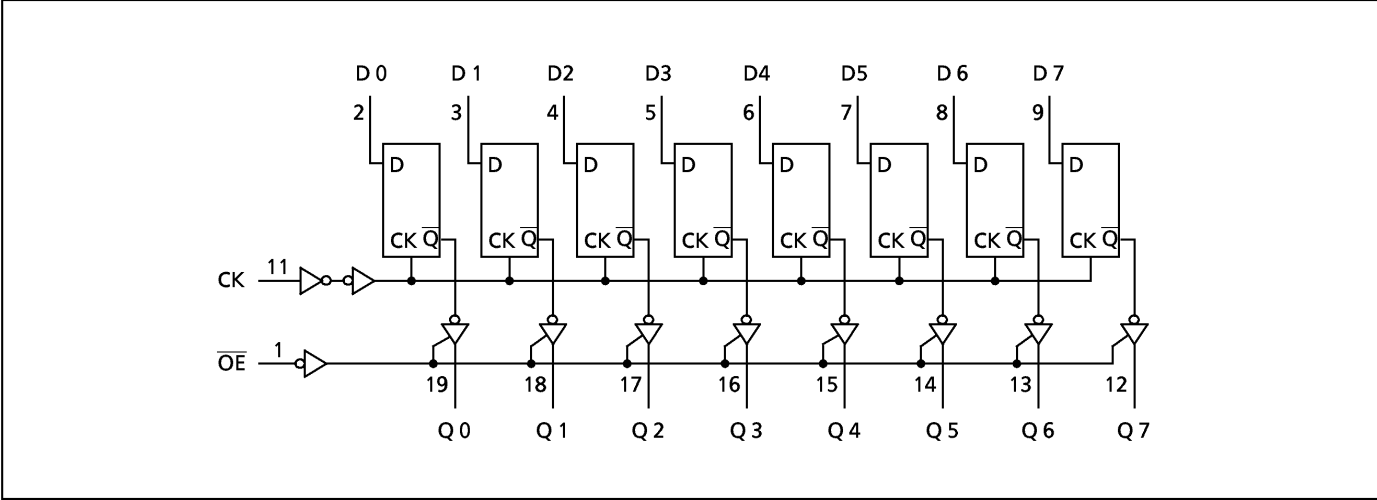
INPUTS			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	Q_n
L		L	L
L		H	H

X : Don't Care
Z : High Impedance
 Q_n : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}C$
Input Rise and Fall Time	dt / dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V _{IH}			2.0 3.0~ 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V
Low - Level Input Voltage	V _{IL}			2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I _{OH} = -4mA I _{OH} = -8mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	± 0.25	—	± 2.50	μA
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND		0~5.5	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _{W(H)} t _{W(L)}		3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Set-up Time	t _s		3.3 ± 0.3	—	3.5	3.5	
			5.0 ± 0.5	—	3.5	3.5	
Minimum Hold Time	t _h		3.3 ± 0.3	—	1.5	1.5	
			5.0 ± 0.5	—	1.5	1.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-Q)	t _{pLH} t _{pHL}		3.3 ± 0.3	15	—	8.5	13.2	1.0	15.5	ns
				50	—	11.0	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	5.6	8.6	1.0	10.0	
				50	—	7.1	10.6	1.0	12.0	
3-State Output Enable Time	t _{pZL} t _{pZH}	RL = 1kΩ	3.3 ± 0.3	15	—	8.2	12.8	1.0	15.0	
				50	—	10.7	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.9	9.0	1.0	10.5	
				50	—	7.4	11.0	1.0	12.5	
3-State Output Disable Time	t _{pL Z} t _{pHZ}	RL = 1kΩ	3.3 ± 0.3	50	—	11.0	15.0	1.0	17.0	
			5.0 ± 0.5	50	—	7.1	10.1	1.0	11.5	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	15	80	125	—	65	—	MHz
				50	50	75	—	45	—	
			5.0 ± 0.5	15	130	180	—	110	—	
				50	85	115	—	75	—	
Output to Output Skew	t _{osLH} t _{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C _{I N}				—	4	10	—	10	pF
Output Capacitance	C _{OUT}				—	6	—	—	—	
Power Dissipation Capacitance	C _{PD}	(Note 2)			—	28	—	—	—	

Note (1) Parameter guaranteed by design. $t_{\text{osLH}} = |t_{\text{pLHm}} - t_{\text{pLHn}}|$, $t_{\text{osHL}} = |t_{\text{pHLm}} - t_{\text{pHLn}}|$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC(opr.)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}} / 8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

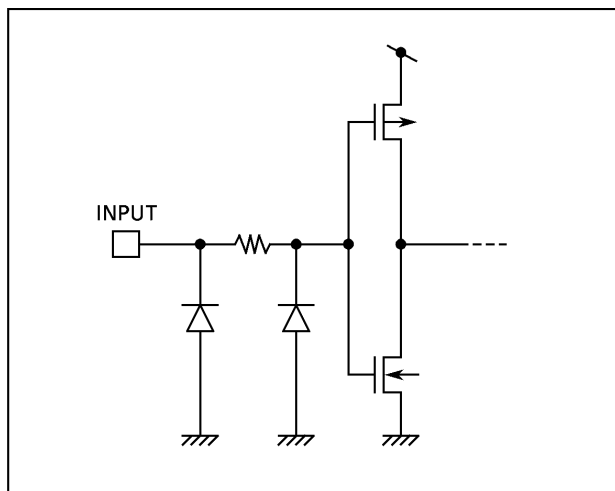
$$C_{\text{PD}} (\text{total}) = 20 + 8 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
				V _{CC} (V)	TYP. / MAX.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.8 (0.9)	1.0 (1.2)	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.8 (-0.9)	-1.0 (-1.2)	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

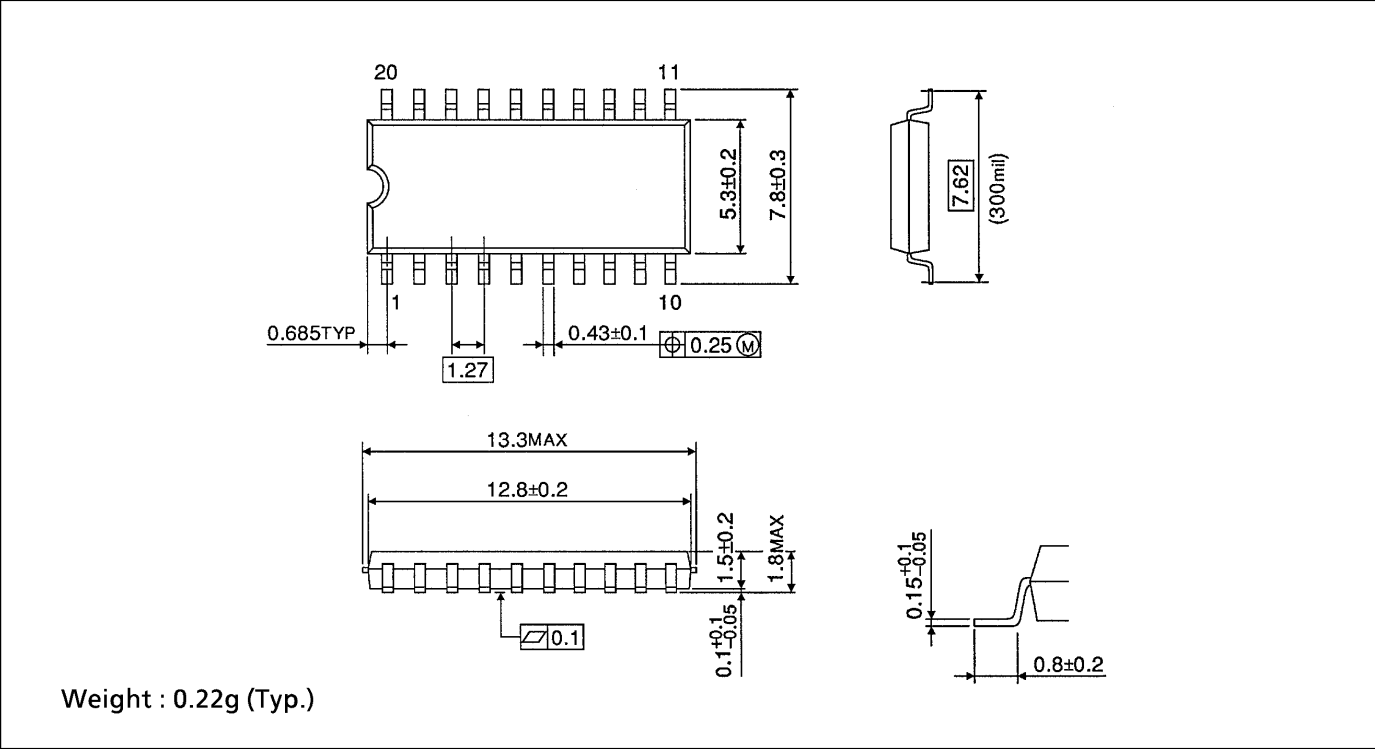
(Note) The value in () only applies to JEDEC SOP (FW) devices.

INPUT EQUIVALENT CIRCUIT



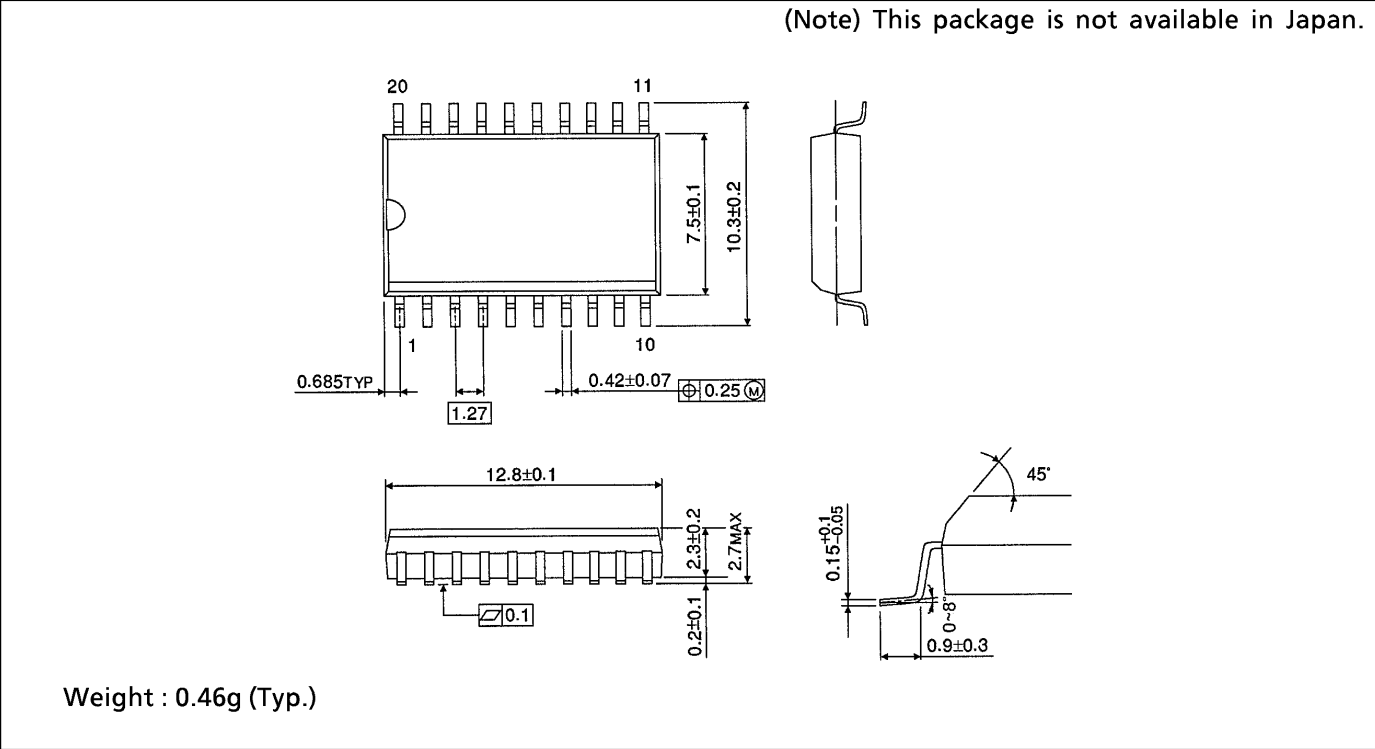
SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

Unit in mm



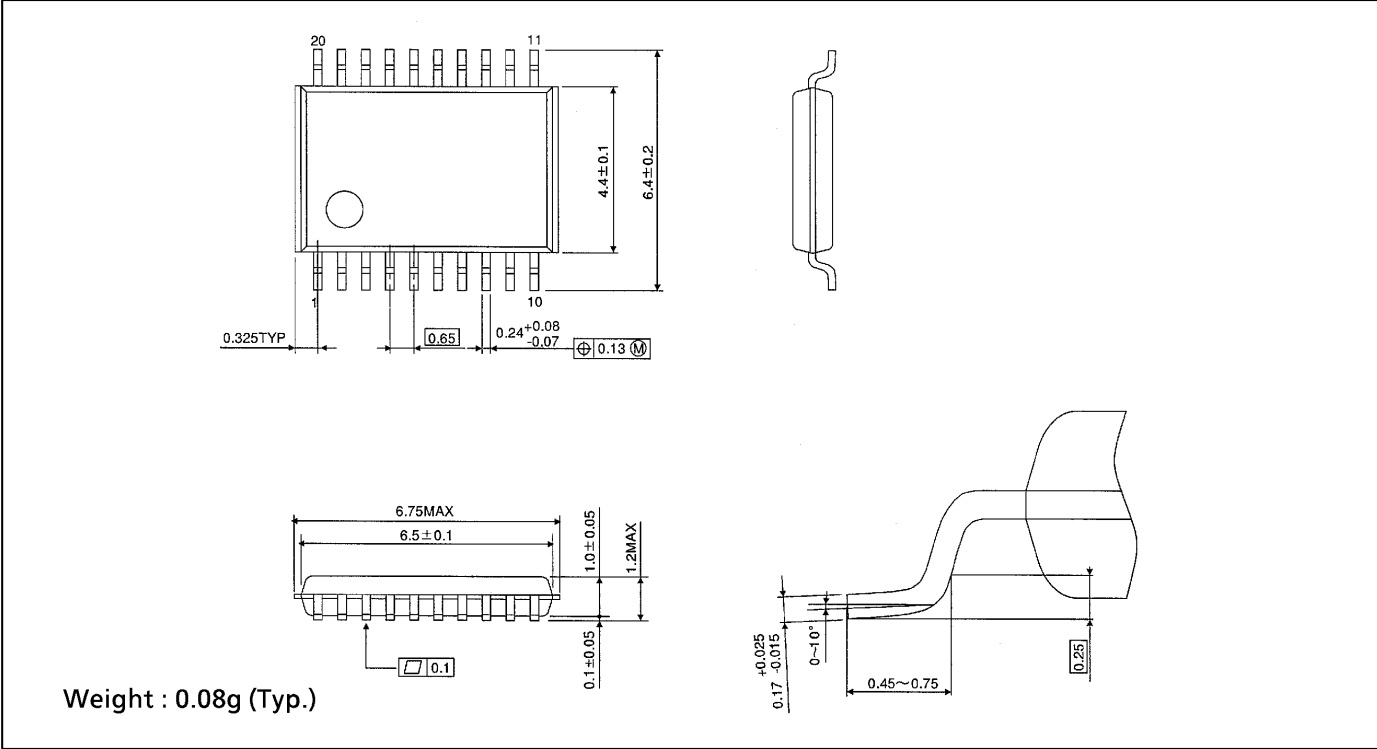
SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm



TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65)

Unit in mm



RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.