

TLP115A

High Speed, Long Distance Isolated Line Receiver

Microprocessor System Interfaces

Digital Isolation For A / D, D / A Conversion

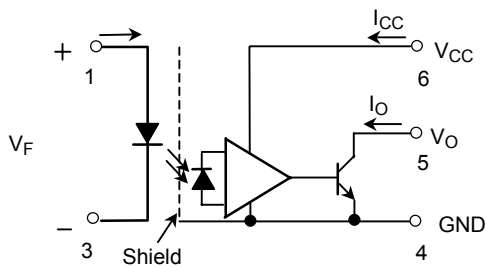
Computer-Peripheral Interfaces

Ground Loop Elimination

The TOSHIBA mini flat coupler TLP115A is a small outline coupler, suitable for surface mount assembly. TLP115A consists of a high output power GaAlAs light emitting diode, optically coupled to an integrated high gain, high speed shielded photo detector whose output is an open collector schottky clamped transistor. The shield, which shunts capacitively coupled common noise to ground, provides a guaranteed transient immunity specification of 1000V / μ s.

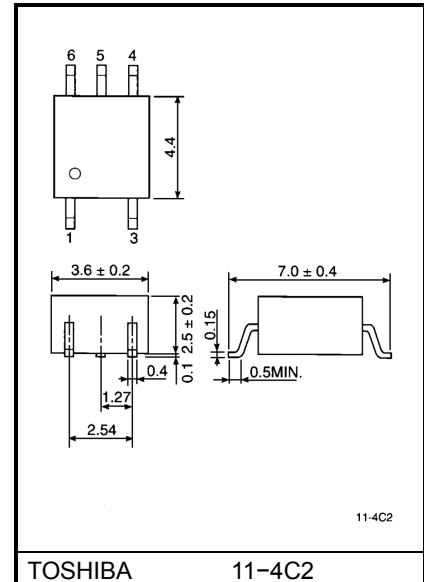
- Input current thresholds: $I_F = 5\text{mA}$ (max.)
- Switching speed: 10MBd (typ.)
- Common mode transient immunity: $\pm 1000\text{V} / \mu\text{s}$ (min.)
- Guaranteed performance over temp. : 0~70°C
- Isolation voltage: 2500Vrms (min.)
- UL recognized: UL1577, file no. E67349

Schematic



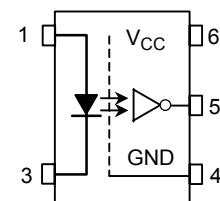
Note. A 0.1 μ F bypass capacitor must be connected between pins 4 and 6.

Unit in mm



Weight: 0.09g

Pin Configuration (top view)



- 1 : Anode
- 3 : Cathode
- 4 : GND
- 5 : V_O (Output)
- 6 : V_{CC}

Truth Table (positive logic)

Input	Output
H	L
L	H

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Note 1)	I _F	20	mA
	Pulse forward current (Note 2)	I _{FP}	40	mA
	Peak transient forward current (Note 3)	I _{FPT}	1	A
	Reverse voltage	V _R	5	V
Detector	Output current	I _O	25	mA
	Output voltage	V _O	7	V
	Supply voltage(1 minute maximum)	V _{CC}	7	V
	Output power dissipation	P _O	40	mW
Operating temperature range		T _{opr}	−40~85	°C
Storage temperature range		T _{stg}	−55~125	°C
Lead solder temperature(10 sec.)		T _{sol}	260	°C
Isolation voltage(AC, 1 min., RH≤ 60%, Note 4)		BV _S	2500	Vrms

(Note 1) Derate 0.36mA / °C above 70°C.

(Note 2) 50% duty cycle, 1ms pulse width. Derate 0.72mA / °C above 70°C.

(Note 3) Pulse width ≤ 1μs, 300pps.

Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input voltage, low level	V _{FL}	−3	0	1.0	V
Input current, high level	I _{FH}	6.3	8	20	mA
Supply voltage	V _{CC}	4.5	5	5.5	V
Fan out (TTL load, each channel)	N	—	—	8	—
Operating temperature	T _{opr}	0	—	70	°C

Electrical Characteristics (unless otherwise specified, Ta = 0~70°C, V_{CC} = 4.5 ~ 5.5V, V_{FL} ≤ 1.0V)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Forward voltage	V _F	I _F = 10mA, Ta = 25°C	1.2	1.4	1.7	V
Forward voltage temperature coefficient	V _F / Ta	I _F = 10mA	—	-2	—	mV / °C
Reverse current	I _R	V _R = 3V, Ta = 25°C	—	—	10	μA
Capacitance between terminals	C _T	V _F = 0, f = 1MHz, Ta = 25°C	—	30	—	pF
High level output voltage	I _{OH}	V _F = 1.0, V _O = 5.5V	—	—	250	μA
		V _F = 1.0, V _O = 5.5V, Ta = 25°C	—	0.5	10	
Low level output current	V _{OL}	I _F = 5mA I _{OL} = 13mA (sinking)	—	0.4	0.6	V
"H level output→L level output" input current	I _{FH}	I _{OL} = 13mA (sinking) V _{OL} = 0.6V	—	—	5	mA
High level supply current	I _{CCH}	V _{CC} = 5.5V, I _F = 0	—	7	15	mA
Low level supply current	I _{CCL}	V _{CC} = 5.5V, I _F = 10mA	—	12	19	mA
Input-output insulation leakage current	I _S	V _S = 3540V, t = 5s Ta = 25°C (Note 4)	—	—	100	μA
Isolation resistance	R _S	R.H. ≤ 60%, V _S = 500V DC Ta = 25°C (Note 4)	5×10 ¹⁰	10 ¹⁴	—	Ω
Stray capacitance between input to output	C _S	V _S = 0, f = 1MHz Ta = 25°C (Note 4)	—	0.8	—	pF

* All typical values are V_{CC} = 5V, Ta = 25°C.

Switching Characteristics ($V_{CC} = 5V$, $T_a = 25^\circ C$)

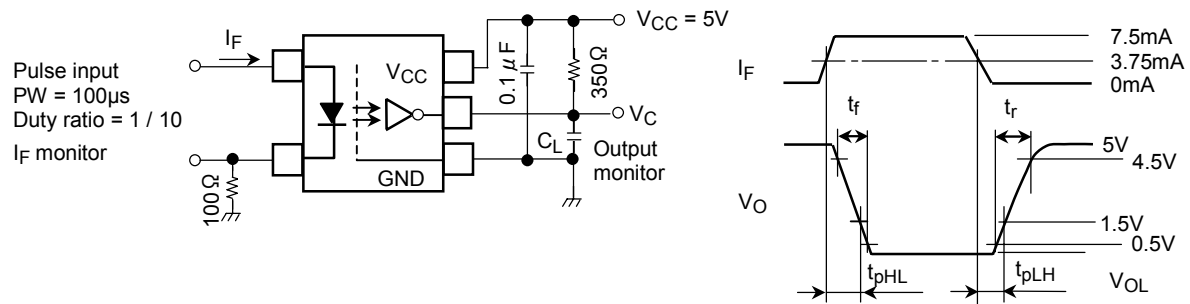
Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time (H→L)	t_{pHL}	1	$I_F = 0 \rightarrow 7.5mA$ $C_L = 15pF$, $R_L = 350\Omega$	—	60	120	ns
Propagation delay time (L→H)	t_{pLH}	1	$I_F = 7.5 \rightarrow 0mA$ $C_L = 15pF$, $R_L = 350\Omega$	—	60	120	ns
Output rise fall time(10–90%)	t_r , t_f	2	$R_L = 350$, $C_L = 15pF$ $I_F = 0 \leftrightarrow 7.5mA$	—	30	—	ns
Common mode transient immunity at high output level	CM_H	2	$I_F = 0$ mA, $V_{CM} = 400V_{p-p}$, $V_{O(MIN)}=2V$ $R_L = 350\Omega$	1000	—	—	V / μs
Common mode transient immunity at low output level	CM_L	2	$I_F = 7.5$ mA, $V_{CM} = 400V_{p-p}$ $V_{O(MAX)} = 0.8V$, $R_L = 350\Omega$	–1000	—	—	V / μs

(Note 4) Device considered a two-terminal device: Pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.

(Note 5) The V_{CC} supply voltage to each TLP115A isolator must be bypassed by 0.1 μF capacitor. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to package V_{CC} and GND pins of each device.

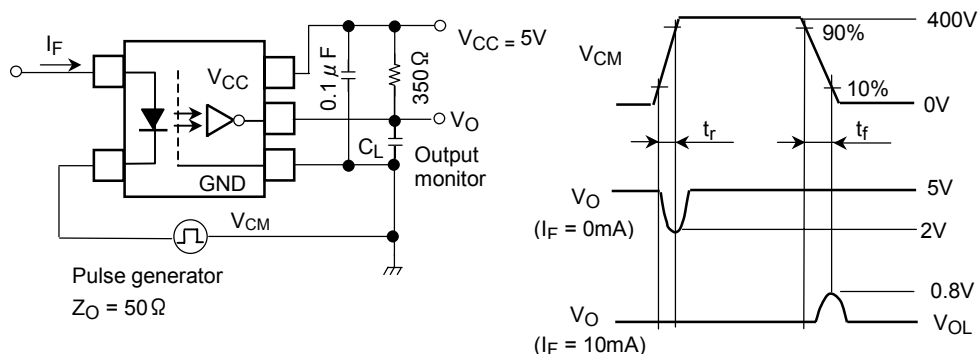
(Note 6) Maximum electrostatic discharge voltage for any pins: 180V(C = 200pF, R = 0)

Test Circuit 1: Switching Time Test Circuit



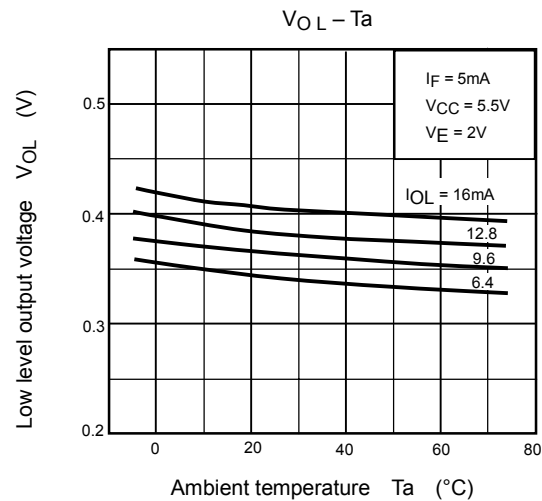
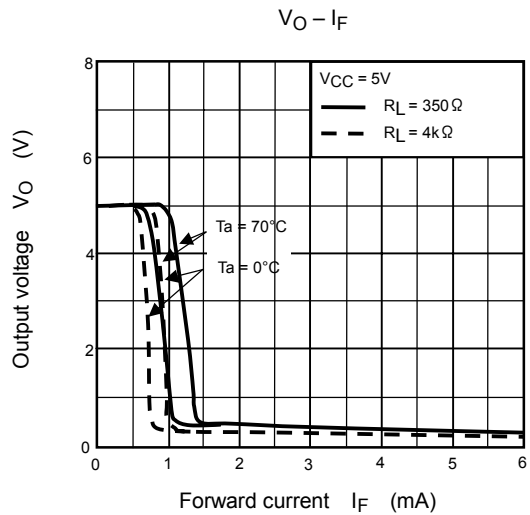
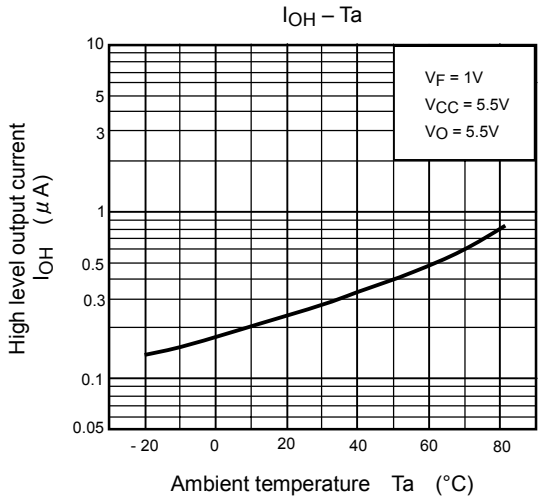
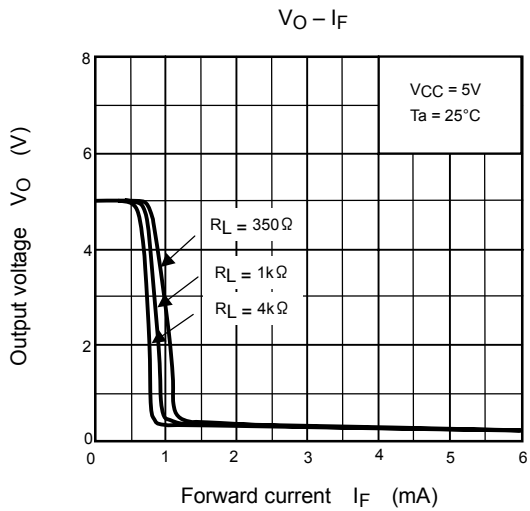
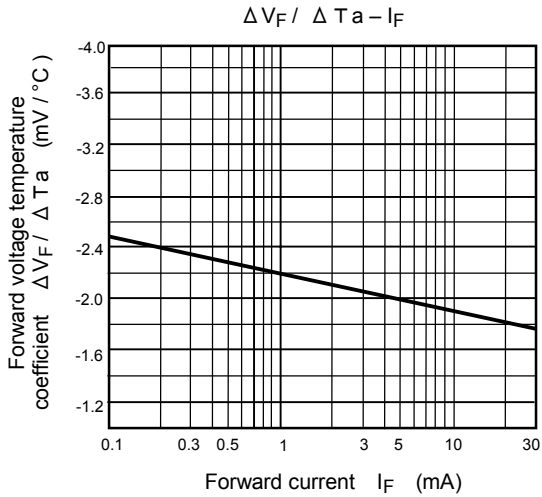
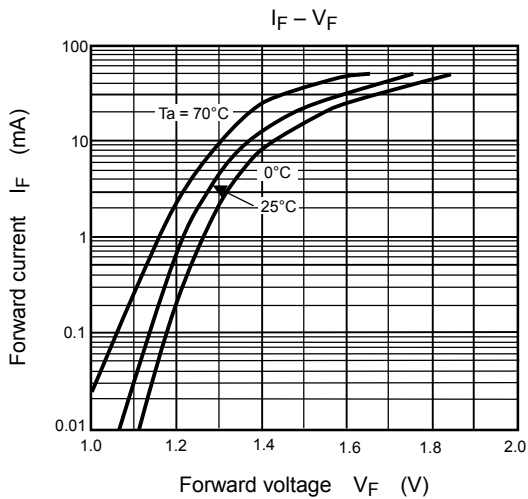
C_L is approximately 15pF which includes probe and stray wiring capacitance.

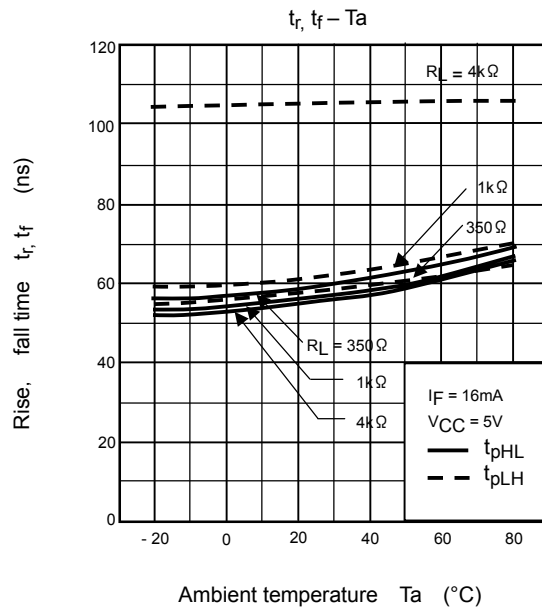
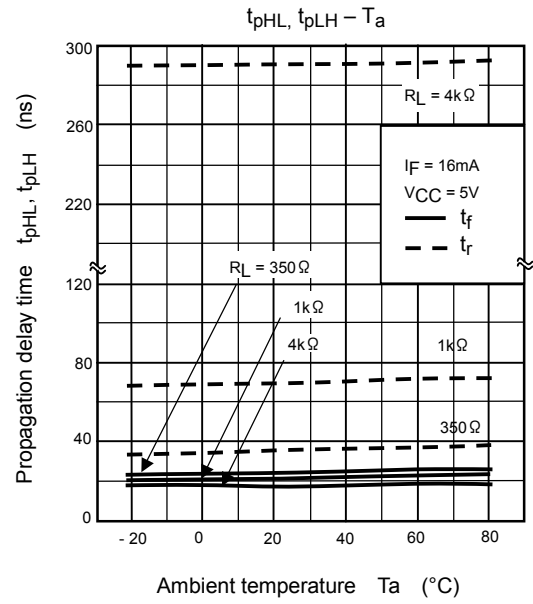
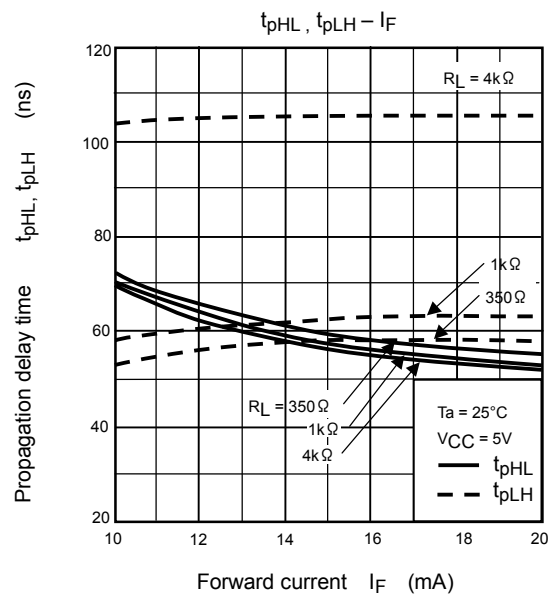
Test Circuit 2: Common Mode Transient Immunity Test Circuit



$$CM_H = \frac{320 \text{ (V)}}{t_r (\mu s)}, CM_L = \frac{320 \text{ (V)}}{t_f (\mu s)}$$

C_L is approximately 15pF which includes probe and stray wiring capacitance.





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