

Timing Processor (LINE, FRAME, SMPS) for TV Sets

General Description

This integrated circuit uses I²L bipolar technology and combines analog signal processing with digital processing. Timing signals are obtained from a Voltage-Controlled Oscillator (VCO) operating at 500 kHz by means of a cheap ceramic resonator.

A chain of dividers and appropriate logic functions are producing very accurately defined sampling pulses and the necessary timing signals. This avoids the frequency adjustment normally required with line and frame oscillators.

Features

- 500 kHz VCO and appropriate logic avoids adjustment of timing pulses
- Identical line and Switch Mode Power Supply (SMPS) frequency avoids visible interference on screen
- Multistandard capability by automatic 50/60 Hz identification
- Low power dissipation by controlling a frame thyristor (or class D output transistor stage)
- Video identification circuit
- Super sandcastle

Case: DIP 28

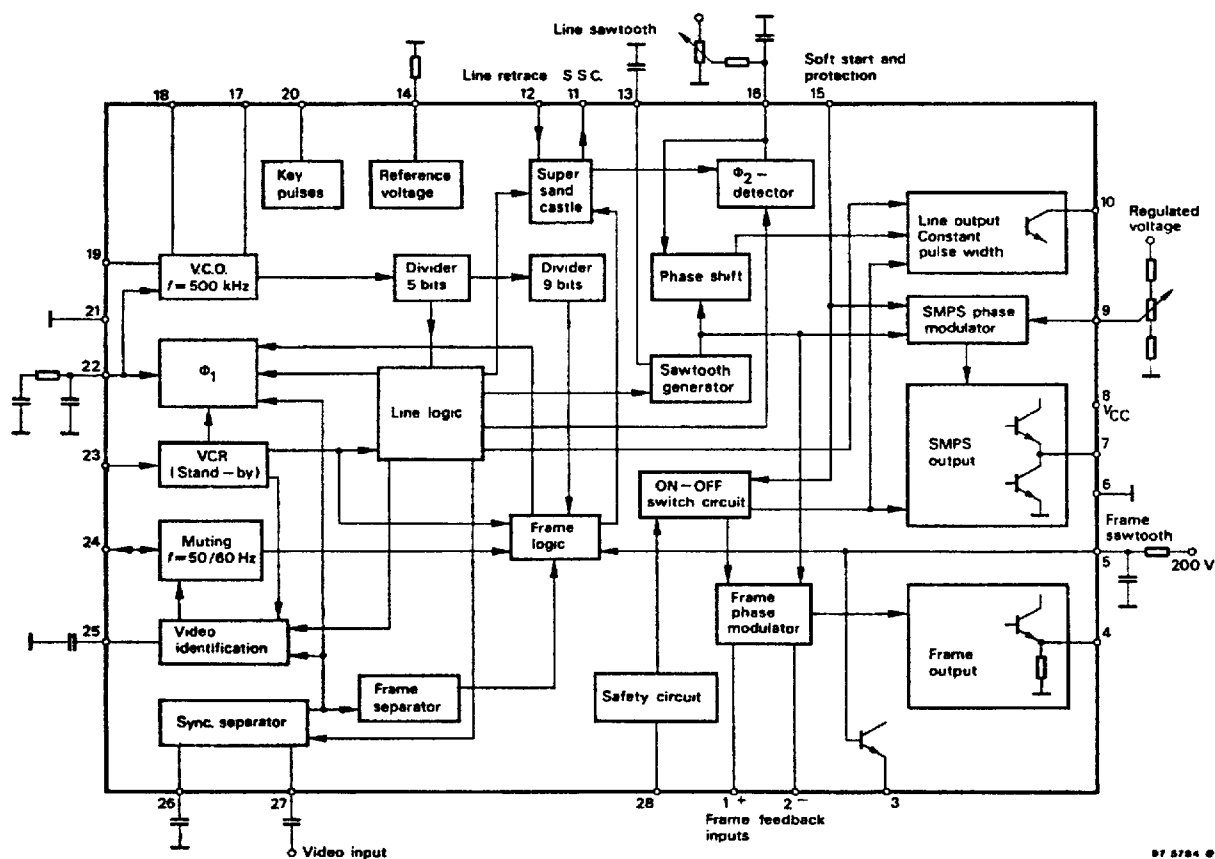


Figure 1. Block diagram

Absolute Maximum Ratings

$T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified.

Parameters	Symbol	Value	Unit
Supply voltage	Pin 8 V_S	14	V
AGC current	Pin 20 I_{20}	5	mA
Video identification current	Pin 24 I_{24}	10	mA
Line retrace current	Pin 12 $\pm I_{12}$	10	mA
Line output current	Pin 10 $+I_{10}$ $-I_{10}$	40 10	
Frame sawtooth generator	Pin 3 I_S	20	mA
Frame output current	Pin 4 I_4	100	mA
SMPS output current	Pin 7 $\pm I_7$	50	mA
Safety input current	Pin 28 I_{28}	5	mA
Safety input voltage	Pin 28 V_{28}	V_{CC}	
Ambient temperature range	T_{amb}	0 to +70	$^{\circ}\text{C}$
Storage temperature range	T_{stg}	-25 to +150	$^{\circ}\text{C}$

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	55	K/W

Electrical Characteristics

$V_S = V_{CC} = 12\text{ V}$, $T_{amb} = 25^{\circ}\text{C}$, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current	Frame, line and SMPS output without load Pin 8	I_S		60	80	mA
Sync. separator	Pins 26 and 27					
Positive video input signal, ac coupled	Source impedance $\leq 200\ \Omega$ Pin 27	V_{27}	0.2	1.8	3	V_{pp}
Negative clamping current during sync. pulse		$-I_{27}$	25	40	55	μA
Clamping current, continuously		I_{27}	3	5	9	μA
Slicing level decoupling 50 % of sync. amplitude	Negative current Pin 26	$-I_{26}$		640	1000	μA
	Positive current	I_{26}	12	25	36	μA
Pulse for keyed AGC	Pin 20					
Output current		I_0			5	mA
Output separation voltage	$I_0 = 5\text{ mA}$	V_0			0.4	V
Delay time from the key pulse leading edge to the middle of the sync. pulse		t_{d1}		3.4		μs
Delay time from the middle of the sync. pulse to the key pulse trailing		t_{d2}		4.8		μs

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Voltage control oscillator, VCO Pin 17, 18, 19						
$V_S = V_{CC} = 11\text{ V to }13\text{ V}$ Ceramic resonator type: CSB 503 B						
Operating voltage	Pin 8	V_S	5		13.2	V
Frequency control range after H. divider	Low-end	f_{low}		15.3		kHz
	High-end	f_{high}		16.1		
Control current	Pin 22	$\pm I_{22}$			10	μA
Phase detector θ_1 Pin 22						
Output current	Low loop gain	$\pm I_0$	0.35	0.5	0.65	mA
	High loop gain		1	1.5	2	
Ratio of charging and discharging current		$I_{\text{ch}}/I_{\text{dis}}$		1		
Transfer gain	Low loop gain	G_{TL}		1.2		kHz/ μs
	High loop gain	G_{TH}		3.6		
Window pulse width (only in low loop gain, video identif. is "ON")		$t_{\theta 1}$		10		μs
Delay time between middle of key pulse and θ_1 comparison edge		t_d		0		μs
VCR and STAND-BY switching input Pin 23						
Threshold voltage VCR (VCR switch is in ON position below this value)		V_T	1.6	2.1	2.6	V
Threshold voltage STAND-BY (STAND-BY switch is in ON position above this level)		V_T	3.2	4	4.8	V
Input current		$-I_1$	0.030		1	mA
Video identification, see figure 2 Pins 24 and 25						
Input current	Pin 24	I_I			10	mA
Output saturation voltage	$I_I = 5\text{ mA}$, no video signal	V_{Osat}			0.6	V
Output voltage	$f = 60\text{ Hz}$, Pin 24 $I_{\text{i(Video)}} = 2.5\text{ mA}$	V_0	5.5	6	7.5	V
Input current	$f = 50\text{ Hz}$ Pin 24	I_I			10	μA
Output current, charging the capacitor	Pin 25	I_{ch}	0.5	0.75	1	mA
Ratio between the charging and discharging current	Pin 25	$I_{\text{ch}}/I_{\text{dis}}$	1.7		4.0	
Identification sampling time	Pin 25	t_{25}	1.3		2.2	μs
Threshold voltage	Pin 25 lower to higher value (low means no video)	V_T	4	4.5	5	V
Hysteresis voltage	Pin 25	V_{hyst}		350		mV
H. ramp generator, see figure 3 Pin 13						
Saw-tooth amplitude synchronized state	peak to peak	v	3	3.5	4	V
Charge current		I_{ch}	185	200	215	μA
Saw-tooth base voltage		V_{min}			0.5	V
Discharging time		t_{dis}			4	μs
Delay time between θ_2 comparing edge and leading edge of discharging pulse		t_d		1.95		μs

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	
Super sandcastle, SSC Pin 11							
Output current		I_{11}	-10		+ 10	mA	
Output voltage levels; Burst key pulse	$I_{11} = 5 \text{ mA}$	V_{Burst}	9			V	
Horizontal blank pulse		V_{HB}	4	4.5	5		
Frame blank pulse	$I_{11} = 5 \text{ mA}$ frame out of function	V_{VB}	2	2.5	3	V	
Delay time between middle of sync. pulse (pin 27) and leading edge of burst key pulse		t_d	2.3		3	μs	
Duration of burst key pulse			3.7	4	5	μs	
Delay time	between SSC cutting level at pin 12 and line blank pulse	t_d			0.5	μs	
Frame retrace blanking duration				24		lines	
Line retrace input Pin 12							
First threshold for blanking		V_b	11		12	V	
Second threshold for ϕ_2		V_{ϕ_2}	-1	1.3	2.3	V	
Input currents:	$V_{12} = 12 \text{ V}$ $V_{12} = 5 \text{ V}$ $V_{12} = 0 \text{ V}$ $V_{12} = 1 \text{ V}$	I_{12}		550 200 -50 -1		μA μA μA mA	
Operating input voltage			-2		1	V	
Phase detector ϕ_2, Pin 16							
Charging current			I_{ch}	0.4	0.6	0.8	mA
Ratio of charging and discharging current		$I_{\text{ch}}/I_{\text{dis}}$		1			
Delay time between the comparing edges of ϕ_1 and ϕ_2 f_0 (VCO) = 500 kHz		t_d	1.5	2	2.8	μs	
Input current of internal error amplifier for ϕ_2 phase shift		I_{16}			3	μA	
Time difference between ϕ_2 comparing edge and middle of line retrace (without external phase tuning circuit)		Δt		0		μs	
Horizontal output (Open collector), Pin 10							
Output saturation voltage	$I_0 = 20 \text{ mA}$	V_0			1	V	
Output current		I_0			40	mA	
Output pulse duration	$f_0 = 500 \text{ kHz}$	t_p	24	26	28	μs	
ϕ_2 phase range	without external phase shift	t_ϕ	14	16	19	μs	
Frame logic							
Free running period video identification = 0		N		315		lines	
Search window		N	247		361	lines	
50 Hz window		N	309		315	lines	
60 Hz window		N	247		277	lines	
VCR mode window		N	247		361	lines	
Frame saw-tooth generator Pin 5							

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Saw-tooth amplitude	peak to peak	v	2	3	4	V
60 Hz internal current generator		I_0	12	14	16	μA
Discharge time	$C = 0.47 \mu\text{F}$, $\Delta V_C = 4 \text{ V}$	t_{dis}			70	μs
Delay time	between beginning of discharging and leading edge of the first main equalizing pulse which appears during internal sync. pulse	t_d		5		μs
Saw tooth base voltage	$I_3 = 0$ to 10 mA Pin 3	V_{min}	1	1.26	1.4	V
Frame feed back inputs Pins 1 and 2						
Input current		$I_{1,2}$			10	μA
Common mode range		CMR	2		10	V
Frame output, see figure 4 Pin 4						
Operating output current		$-I_0$			80	mA
Limit value		$-I_{0M}$			100	mA
Max. "ON" time		t_{on}		40		μs
Output phase range		t_{θ}	0		t_{onmax}	μs
Negative over current	limit value	I_{N0}		10		mA
Output voltage	$I_4 = -80 \text{ mA}$	V_O	10			V
Switch mode power supply, SMPS						
Input current	Pin 9	I_I			10	μA
Internal reference voltage		V_{ref}	1.2	1.26	1.35	V
SMPS Output, see figure 5 Pin 7						
Output current limit value		I_0	-50		50	mA
Output voltage	$I_0 = -20 \text{ mA}$ $I_0 = +20 \text{ mA}$	V_0	10		2	V
t_{on} time		t_{onmax}	27	28	29	μs
Position of trailing edge of SMPS pulse			3 μs before middle of H sync. pulse			
Negative over current limit value		I_{N0}			50	mA
Safety input, Pin 28						
Threshold voltage		V_T	1.15	1.26	1.37	V
Input current	$V_T = V_{\text{ref}}$	I_I			3	μA
Input voltage		$V_{28\text{max}}$			V_{CC}	
Soft starting input and SMPS - T_{ON} limitation (see figure 6), Pin 15						
Charging current	$t = 4 \mu\text{s}$	I_{ch}	70		130	μA
Ratio of charging and discharging current		$I_{\text{ch}} / I_{\text{dis}}$		1		
Charging time		t_{ch}		4		μs
Ratio of charging and discharging time		$t_{\text{ch}} / t_{\text{dis}}$		2		

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Switch-ON, Switch-OFF processing Pins 4, 7 and 10						
SMPS	frame and line V_{CC} start-ing	V_S	$5.25 + V_{hyst}$		$6.5 + V_{hyst}$	V
	V_{CC} stopping		5.25		6.25	
Hysteresis between switch on- and off level		V_{hyst}		500		mV
Voltage reference	Pin 14	V_{ref}	1.2	1.26	1.35	V

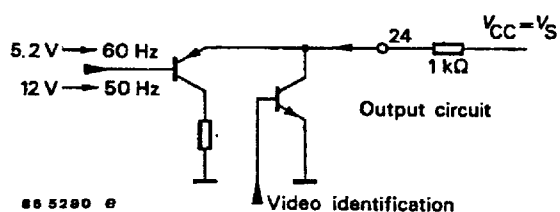


Figure 2.

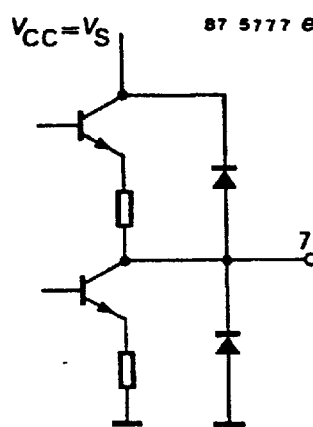


Figure 5.

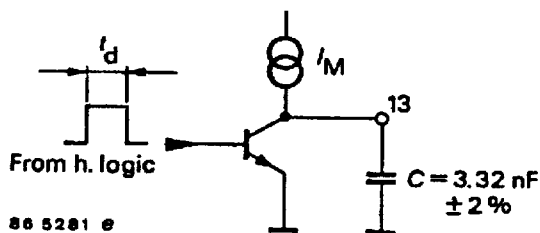


Figure 3.

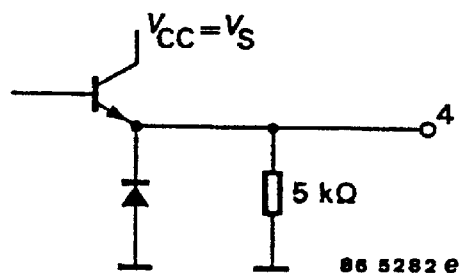


Figure 4.

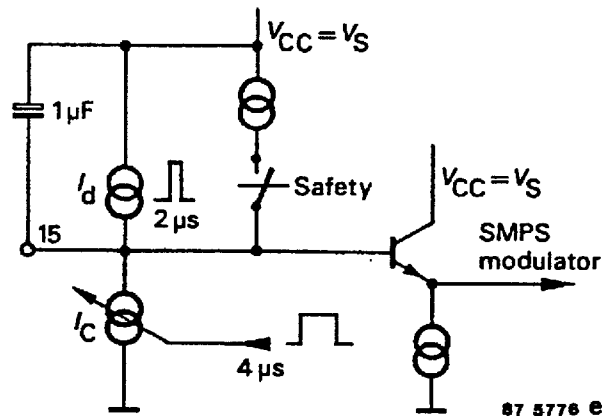


Figure 6.

I_C = charge current (I_{ch})

I_d = discharge current (I_{dis})

t_d = discharge time (t_{dis})

Application

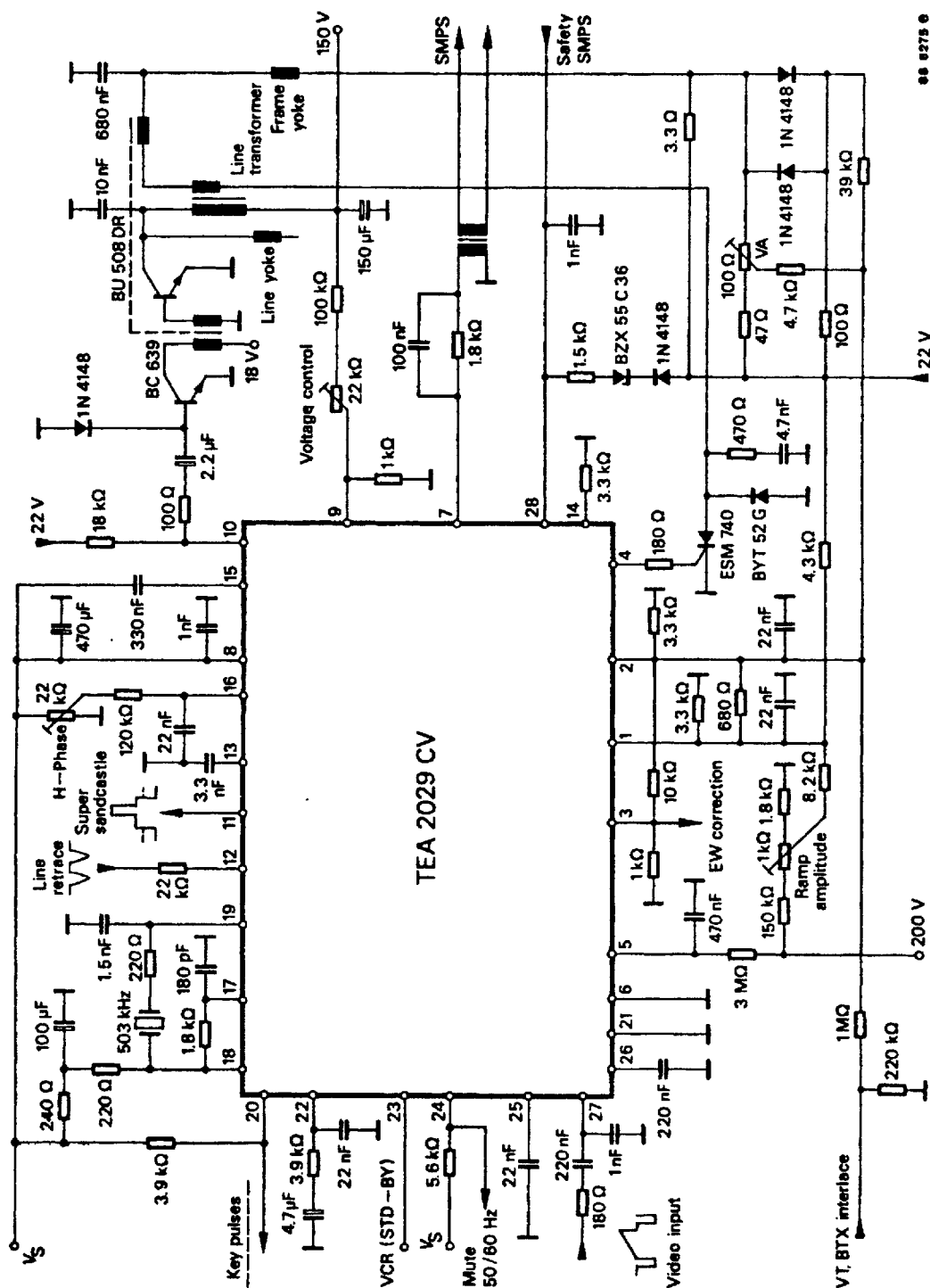


Figure 7.

TEA2029CV

Dimension in mm

Package: DIP 28

