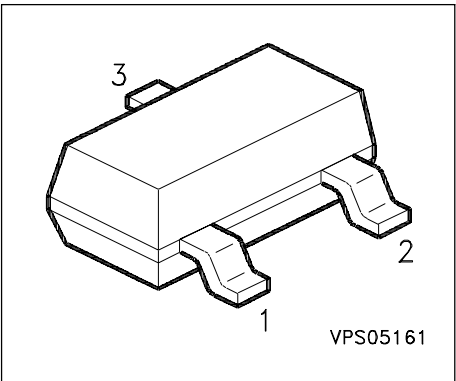
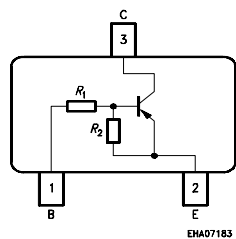


PNP Silicon Digital Transistor

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ($R_1=4.7k\Omega$, $R_2=4.7k\Omega$)



Type	Marking	Ordering Code	Pin Configuration			Package
BCR 562	XUs	Q62702-C2356	1=B	2=E	3=C	SOT-23

Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Emitter-base voltage	V_{EBO}	10	
Input on Voltage	$V_{i(on)}$	30	
DC collector current	I_C	500	mA
Total power dissipation, $T_S = 79\text{ °C}$	P_{tot}	330	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	- 65 ... + 150	

Thermal Resistance

Junction ambient ¹⁾	R_{thJA}	≤ 325	K/W
Junction - soldering point	R_{thJS}	≤ 215	

1) Package mounted on pcb 40mm x 40mm x 1.5mm / 6cm² Cu

Electrical Characteristics at $T_A=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC Characteristics

Collector-emitter breakdown voltage $I_C = 100\ \mu\text{A}$, $I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10\ \mu\text{A}$, $I_B = 0$	$V_{(BR)CBO}$	50	-	-	
Collector cutoff current $V_{CB} = 40\ \text{V}$, $I_E = 0$	I_{CBO}	-	-	100	nA
Emitter cutoff current $V_{EB} = 10\ \text{V}$, $I_C = 0$	I_{EBO}	-	-	1.61	mA
DC current gain $I_C = 50\ \text{mA}$, $V_{CE} = 5\ \text{V}$	h_{FE}	60	-	-	-
Collector-emitter saturation voltage 1) $I_C = 50\ \text{mA}$, $I_B = 2.5\ \text{mA}$	V_{CEsat}	-	-	0.3	V
Input off voltage $I_C = 100\ \mu\text{A}$, $V_{CE} = 5\ \text{V}$	$V_{i(off)}$	0.6	-	1.5	
Input on Voltage $I_C = 2\ \text{mA}$, $V_{CE} = 0.3\ \text{V}$	$V_{i(on)}$	1	-	2.2	
Input resistor	R_1	3.2	4.7	6.2	k Ω
Resistor ratio	R_1/R_2	0.9	1	1.1	-

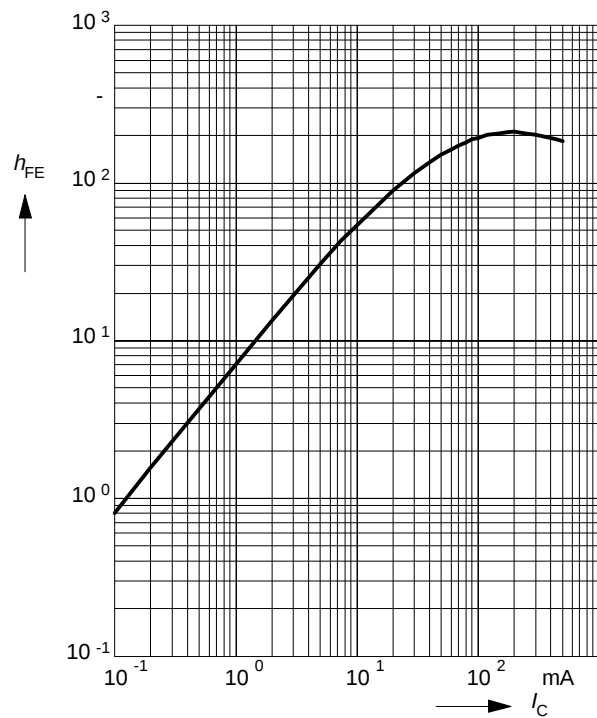
AC Characteristics

Transition frequency $I_C = 50\ \text{mA}$, $V_{CE} = 5\ \text{V}$, $f = 100\ \text{MHz}$	f_T	-	150	-	MHz
--	-------	---	-----	---	-----

1) Pulse test: $t < 300\ \mu\text{s}$; $D < 2\%$

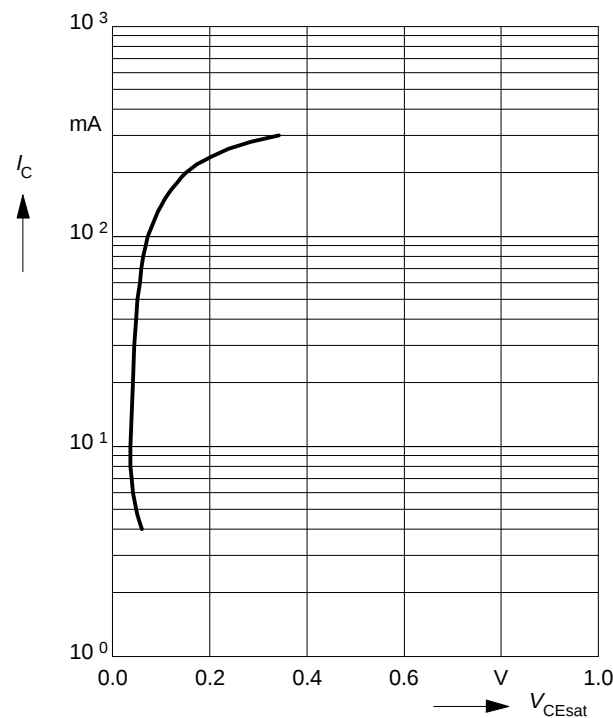
DC Current Gain $h_{FE} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)



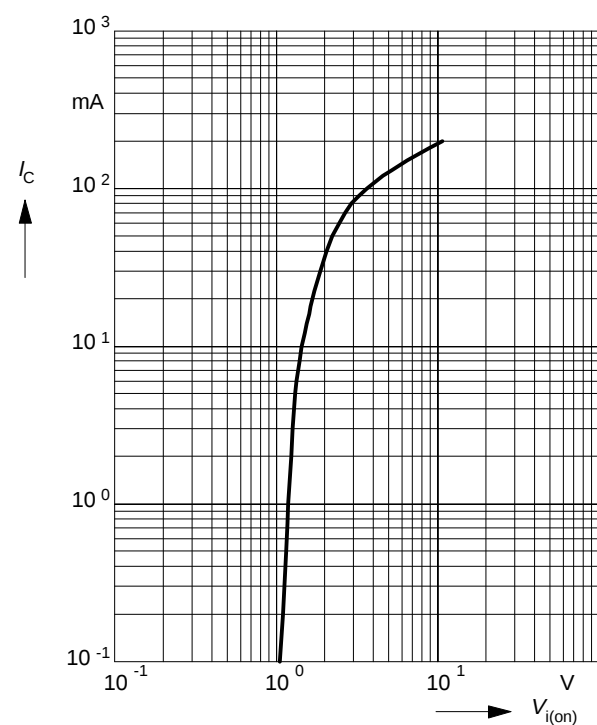
Collector-Emitter Saturation Voltage

$V_{CEsat} = f(I_C), h_{FE} = 20$



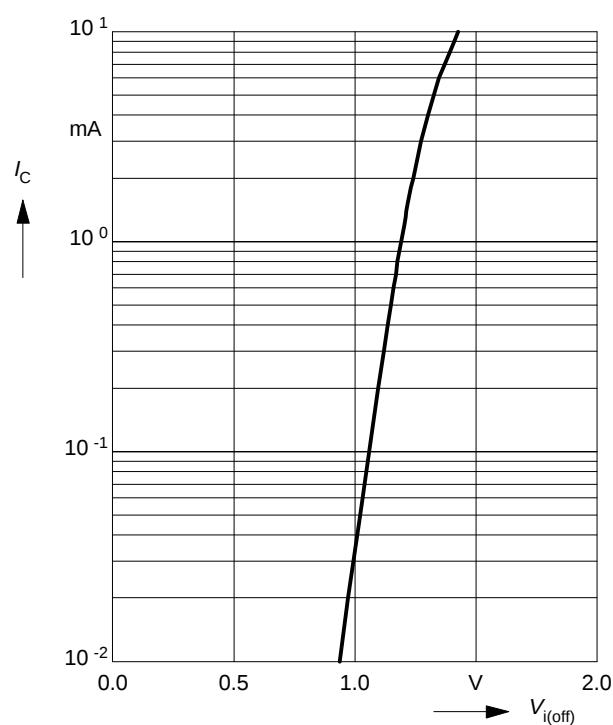
Input on Voltage $V_{i(on)} = f(I_C)$

$V_{CE} = 0.3V$ (common emitter configuration)



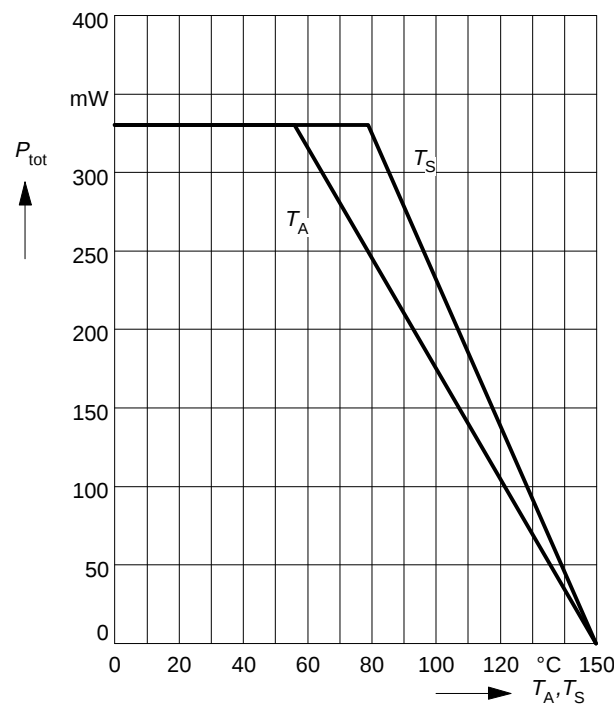
Input off voltage $V_{i(off)} = f(I_C)$

$V_{CE} = 5V$ (common emitter configuration)

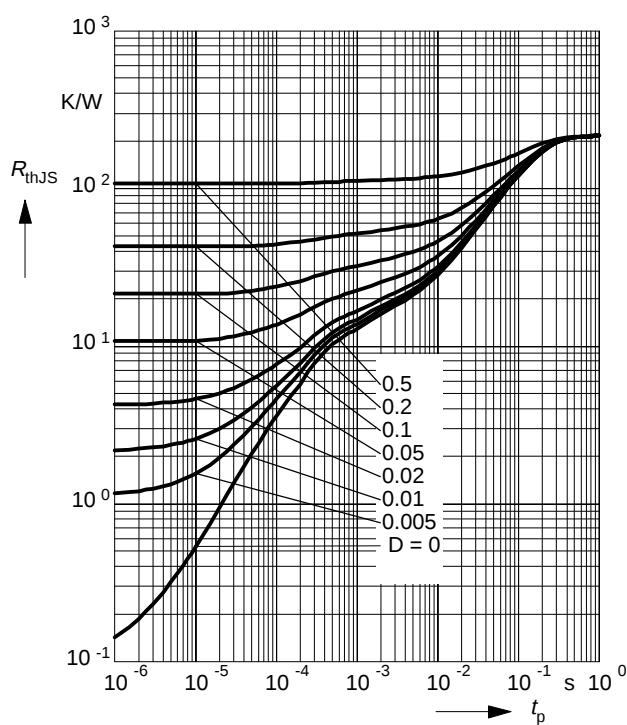


Total power dissipation $P_{\text{tot}} = f(T_A^*; T_S)$

* Package mounted on epoxy



Permissible Pulse Load $R_{\text{thJS}} = f(t_p)$



Permissible Pulse Load $P_{\text{totmax}} / P_{\text{totDC}} = f(t_p)$

