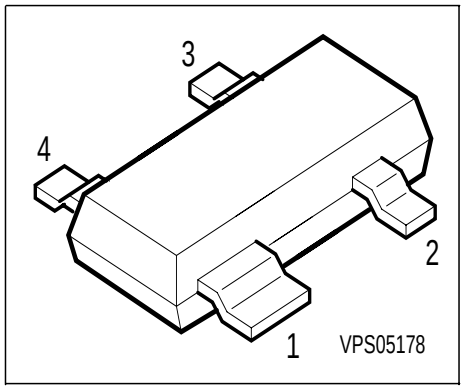
Silicon N Channel MOSFET Tetrode

Target data sheet

- Short-channel transistor with high S/C quality factor
- For low-noise, gain-controlled input stages up to 1 GHz



Type	Marking	Ordering Code	Pin Configuration				Package
BF 2000	NDs	Q62702-F1771	1 = S	2 = D	3 = G2	4 = G1	SOT-143

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	12	V
Continuos drain current	I_D	30	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Total power dissipation, T_S = 76 °C	P_{tot}	200	mW
Storage temperature	T_{stg}	- 55 ...+150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Channel - soldering point	R_{thchs}	≤370	K/W

Electrical Characteristics at T_A = 25 °C; unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Drain-source breakdown voltage I_D = 10 µA, -V_{G1S} = 4 V, - V_{G2S} = 4 V	$V_{(BR)DS}$	12	-	-	V
Gate 1 source breakdown voltage ±I_{G1S} = 10 mA, V_{G2S} = V_{DS} = 0	±$V_{(BR)G1SS}$	8	-	12	V
Gate 2 source breakdown voltage ±I_{G2S} = 10 mA, V_{G1S} = 0 V, V_{DS} = 0 V	±$V_{(BR)G2SS}$	8	-	12	
Gate 1 source leakage current ±V_{G1S} = 5 V, V_{G2S} = V_{DS} = 0	±I_{G1SS}	-	-	50	nA
Gate 2 source leakage current ±V_{G2S} = 5 V, V_{G1S} = 0 V, V_{DS} = 0 V	±I_{G2SS}	-	-	50	
Drain current V_{DS} = 5 V, V_{G1S} = 0 , V_{G2S} = 4 V	I_{DSS}	-	-	1	µA
Gate 1-source pinch-off voltage V_{DS} = 5 V, V_{G2S} = 4 V, I_D = 200 µA	$V_{G1S(p)}$	-	0.3	-	V
Gate 2-source pinch-off voltage V_{DS} = 5 V, I_D = 100 µA	$V_{G2S(p)}$	-	0.2	-	V

Electrical Characteristics at T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC characteristics					
Forward transconductance V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 kHz	g_{fs}	-	24	-	mS
Gate 1 input capacitance V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{g1ss}	-	1.2	-	pF
Gate 2 input capacitance V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{g2ss}	-	-	-	
Feedback capacitance V_{DS} = 8 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{dg1}	-	25	-	fF
Output capacitance V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{dss}	-	0.8	-	pF
Power gain V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 45 MHz	G_{ps}	28	29	-	dB
Power gain V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 800 MHz	G_{ps}	-	22	-	
Noise figure V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 45 MHz	F	-	1.1	-	
Noise figure V_{DS} = 5 V, I_D = 10 mA, V_{G2S} = 4 V, f = 800 MHz	F	-	1	-	
Gain control range V_{DS} = 8 V, VG2S = 4 ... -2V, f = 800 MHz	ΔG_{ps}	40	-	-	