

HIGH SPEED OPTOCOUPLER

FEATURES

- Surface Mountable
 - Industry Standard SOIC-8 Footprint
 - Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes
 - Isolation Voltage, 2500 V_{RMS}
 - Very High Common Mode Transient Immunity: 15000 V/ μ s at V_{CM}=1500 V Guaranteed (SFH6343)
 - High Speed: 1 Mb/s
 - TTL Compatible
 - Guaranteed AC and DC Performance Over Temperature: 0°C to 70°C
 - Open Collector Output
 - Pin Compatible with HP Optocouplers
- SFH6315—HCPL0500
SFH6316—HCPL0501
SFH6343—HCPL0453

APPLICATIONS

- Line Receivers
- Logic Ground Isolation
- Analog Signal Ground Isolation
- Replace Pulse Transformers

DESCRIPTION

The SFH6315/16/43, high speed optocouplers, each consists of a GaAlAs infrared emitting diode, optically coupled with an integrated photodetector and a high speed transistor. The photodetector is junction isolated from the transistor to reduce miller capacitance effects. The open collector output function allows circuit designers to adjust the load conditions when interfacing with different logic systems such as TTL, CMOS, etc.

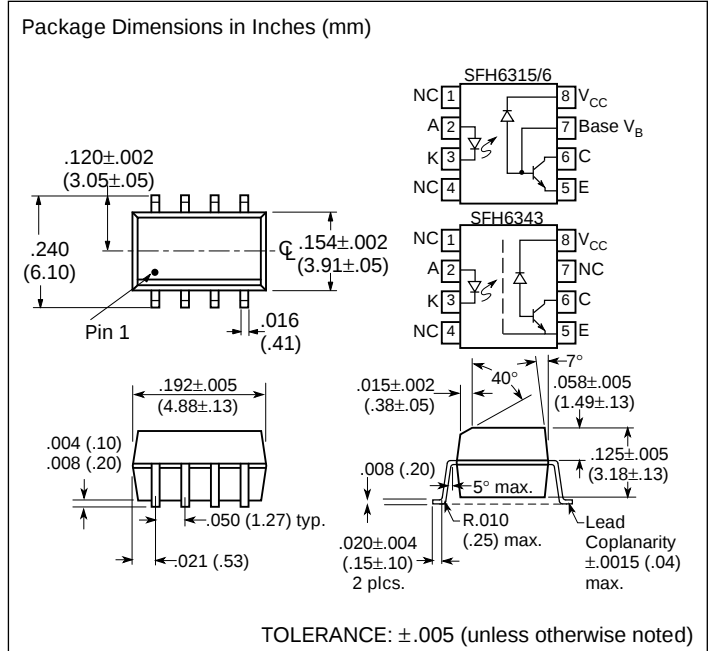
Because the SFH6343 has a Faraday shield on the detector chip, it can also reject and minimize high input to output common mode transient voltages. There is no base connection, further reducing the potential electrical noise entering the package.

The SFH6315/16/43 are packaged in industry standard SOIC-8 packages and are suitable for surface mounting.

Absolute Maximum Ratings

Emitter (GaAlAs)

Reverse Voltage.....	3 V
DC Forward Current.....	25 mA
Surge Forward Current	1 A
tp $\leq$ 1 μ s, 300 pulses/sec.	
Total Power Dissipation (T _A $\leq$ 70°C).....	45 mW



Absolute Maximum Ratings (continued)

Detector(Si Photodiode + Transistor)

Supply Voltage	-0.5 to 30 V
Output Voltage	-0.5 to $\geq$ 20 V
Output Current.....	8 mA
Total Power Dissipation (T _A $\leq$ 70°C)	100 mW

Package

Isolation Test Voltage	
between emitter and detector	2500 VAC _{RMS}
(refer to climate DIN 40046, part 2, Nov. 74)	
Pollution Degree (DIN VDE0110)	2
Creepage	$\geq$ 4 mm
Clearance	$\geq$ 4 mm
Comparative Tracking Index	
per DIN IEC 112/VDE 0303, part 1	175
Isolation Resistance	
V _{IO} =500 V, T _A =25°C, R _{ISOL} (Note 2).....	$\geq 10^{12} \Omega$
V _{IO} =500 V, T _A =100°C, R _{ISOL} (Note 2).....	$\geq 10^{11} \Omega$
Storage Temperature Range	-55°C to +150°C
Ambient Temperature Range	-55°C to +100°C
Junction Temperature.....	100°C
Soldering Temperature (t=10 sec. max.).....	260°C
Dip soldering: distance to seating plane $\geq$ 1.5 mm	

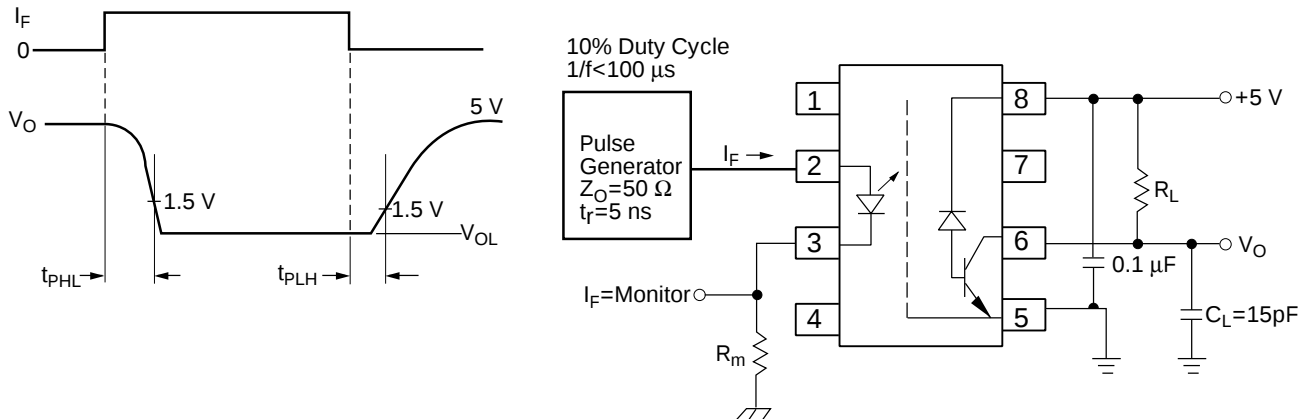
Specifications subject to change.

Electrical Characteristics

Over recommended temperature ($T_A=0^{\circ}\text{C}$ to 70°C) unless otherwise specified. See note 6. *All typical values at $T_A=25^{\circ}\text{C}$.

Parameter	Sym- bol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Note
Input Forward Voltage	V_F			1.6	1.8 1.9	V	$T_A=25^{\circ}\text{C}$	$I_F=16\text{ mA}$	
Input Reverse Current	I_R			0.5	10	μA	$V_R=3\text{ V}$		
Input Capacitance	C_{IN}			75		pF	$f=1\text{ MHz}$, $V_F=0\text{ V}$		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.7		mV/ $^{\circ}\text{C}$	$I_F=16\text{ mA}$		
Logic Low Supply Current	I_{CCL}			100		μA	$I_F=16\text{ mA}$, $V_O=\text{Open}$, $V_{CC}=15\text{ V}$		
Logic High Supply Current	I_{CCH}			0.001	1 2	μA	$T_A=25^{\circ}\text{C}$	$I_F=0\text{ mA}$, $V_O=\text{Open}$, $V_{CC}=15\text{ V}$	
Logic Low Output Voltage	V_{OL}	SFH6315		0.15	0.4 0.5	V	$T_A=25^{\circ}\text{C}$	$I_O=1.1\text{ mA}$	$I_F=16\text{ mA}$, $V_{CC}=4.5\text{ V}$
								$I_O=0.8\text{ mA}$	
		SFH6316 SFH6343		0.15	0.4 0.5	V	$T_A=25^{\circ}\text{C}$	$I_O=3.0\text{ mA}$	
								$I_O=2.4\text{ mA}$	
Logic High Output Current	I_{OH}			0.003	0.5	μA	$T_A=25^{\circ}\text{C}$	$V_O=V_{CC}=5.5\text{ V}$	$I_F=0\text{ mA}$
				0.01	1		$T_A=25^{\circ}\text{C}$	$V_O=V_{CC}=15.0\text{ V}$	
				50			$T_A=0-70^{\circ}\text{C}$	$V_O=V_{CC}=15.0\text{ V}$	
Transistor DC Current Gain	h_{FE}			150			$V_O=5\text{ V}$, $I_O=3\text{ mA}$		
Capacitance (Input-Output)	C_{I-O}			0.4		pF	$f=1\text{ MHz}$		6
Current Transfer Ratio	CTR	SFH6315	7	16	50	%	$T_A=25^{\circ}\text{C}$	$V_O=0.4\text{ V}$	$I_F=16\text{ mA}$, $V_{CC}=4.5\text{ V}$
			5	17				$V_O=0.5\text{ V}$	
		SFH6316 SFH6343	19	35	50	%	$T_A=25^{\circ}\text{C}$	$V_O=0.4\text{ V}$	
			15	36				$V_O=0.5\text{ V}$	

Figure 1. Test circuit for switching times



Switching Specifications

Over recommended temperature ($T_A=0^{\circ}\text{C}$ to 70°C), $V_{CC}=5\text{ V}$, $I_F=16\text{ mA}$ unless otherwise specified. *All typical values, $T_A=25^{\circ}\text{C}$

Parameter	Sym- bol	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t _{PHL}	SFH6315		0.5	1.5	μs	T _A =25°C	R _L =4.1 KΩ	1	4, 5
					2.0					
		SFH6316 SFH6343		0.25	0.8		T _A =25°C	R _L =1.9 KΩ		
					1.0					
Propagation Delay Time to Logic High at Output	t _{PLH}	SFH6315		0.5	1.5	μs	T _A =25°C	R _L =4.1 KΩ	1	4, 5
					2.0					
		SFH6316 SFH6343		0.5	0.8		T _A =25°C	R _L =1.9 KΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	CM _H	SFH6315		1		kV/μs	R _L =4.1 KΩ	I _F =0 mA T _A =25°C V _{CM} =10 V _{P-P}	2	3, 4, 5
		SFH6316		1			R _L =1.9 KΩ			
		SFH6343	15	30			R _L =1.9 KΩ	I _F =0 mA T _A =25°C V _{CM} =1500 V _{P-P}		
Common Mode Transient Immunity at Logic Low Level Output	CM _L	SFH6315		1		kV/μs	R _L =4.1 KΩ	I _F =16 mA T _A =25°C V _{CM} =10 V _{P-P}	2	3, 4, 5
		SFH6316		1			R _L =1.9 KΩ			
		SFH6343	15	30			R _L =1.9 KΩ	I _F =16 mA T _A =25°C V _{CM} =1500 V _{P-P}		

Notes

- Current transfer ratio in percent equals the ratio of output collector current (I_O) to the forward LED input current (I_F) times 100.
- Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
- Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse (V_{CM}) to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0\text{ V}$). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal (V_{CM} to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8\text{ V}$).
- The $1.9\text{ K}\Omega$ load represents 1 TTL unit load of 1.6 mA and the $5.6\text{ k}\Omega$ pull-up resistor.
- The $4.1\text{ K}\Omega$ load represents 1 LSTTL unit load of 0.36 mA and the $6.1\text{ k}\Omega$ pull-up resistor.
- A $0.1\text{ }\mu\text{F}$ bypass capacitor connected between pins 5 and 8 is recommended.

Figure 2. Test circuit for transient immunity and typical waveforms

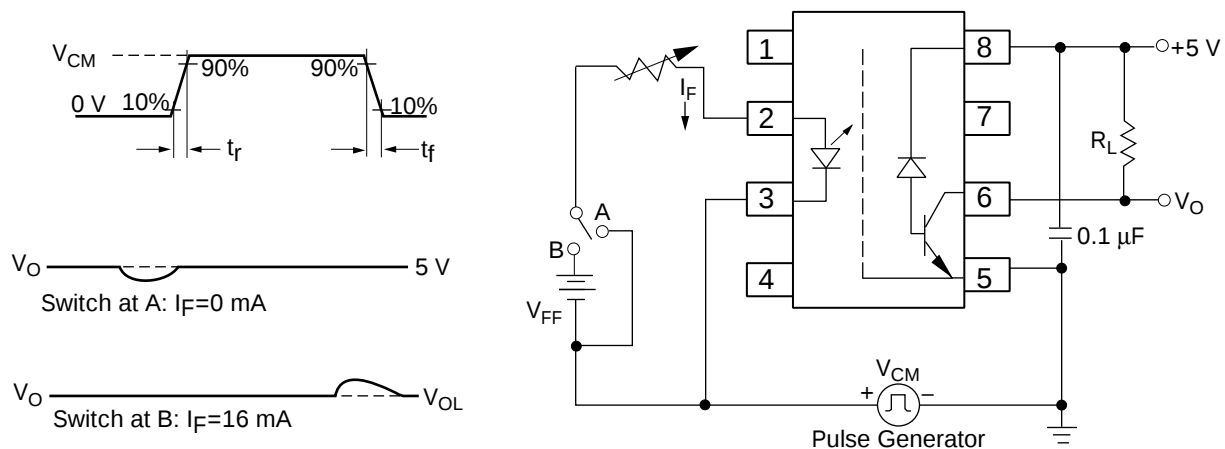


Figure 3. LED forward current vs. forward voltage

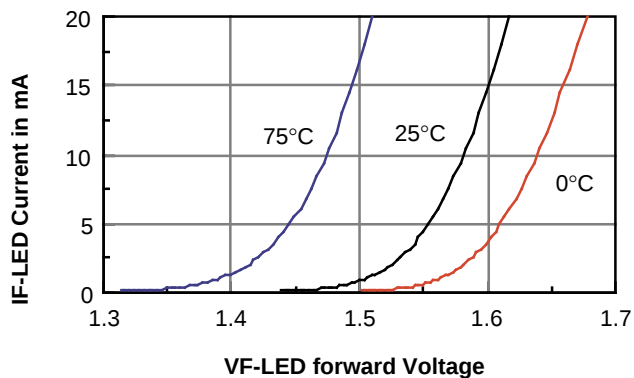


Figure 4. Permissible forward LED current vs. temperature

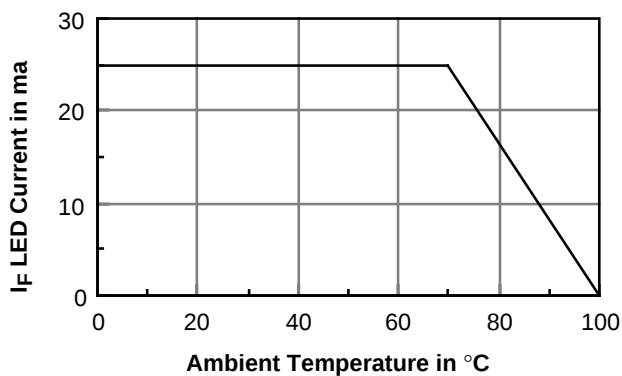


Figure 5. Permissible power dissipation vs. temp.

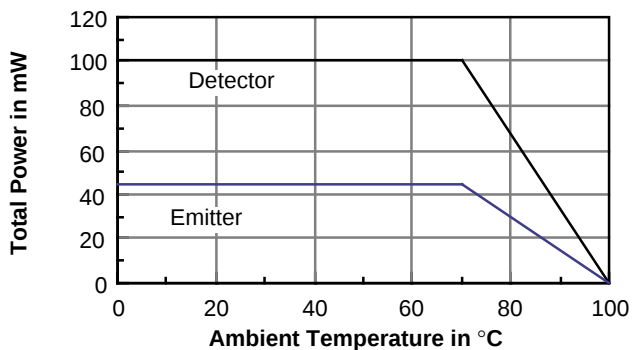


Figure 6. Output current vs. output voltage

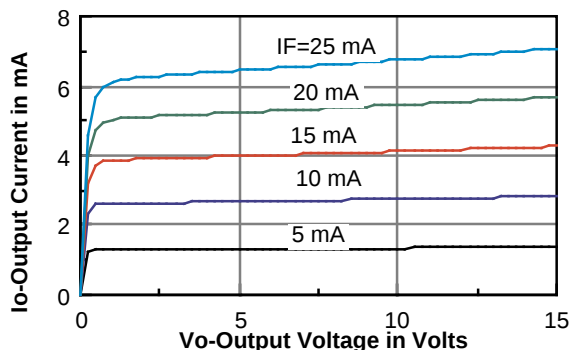


Figure 7. Output current (high) vs. temperature

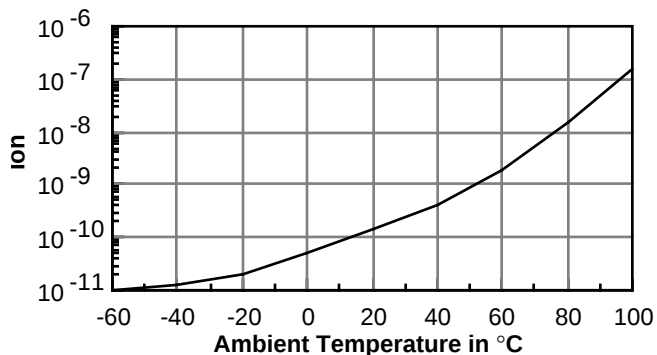


Figure 8. NCTR vs. IF

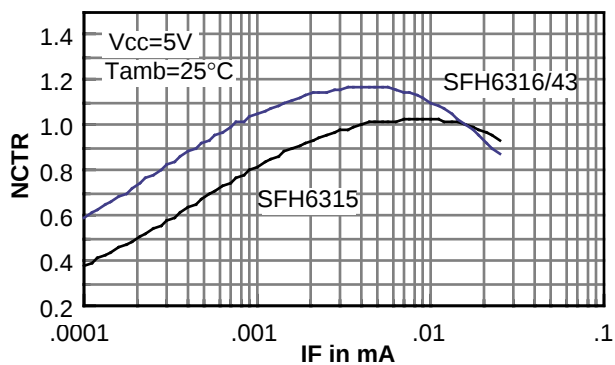


Figure 9. NCTR vs. temperature (SFH6316/43)

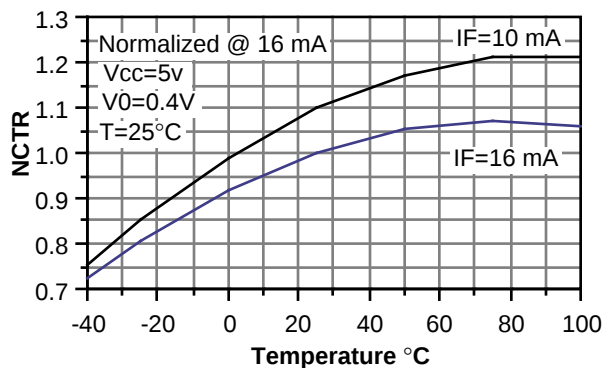


Figure 10. NCTR vs. temperature (SFH6315)

