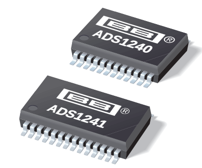
Burr-Brown Products from Texas Instruments



ADS1240
ADS1241

SBAS173A – JUNE 2001

24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 24 BITS NO MISSING CODES
- SIMULTANEOUS 50Hz AND 60Hz REJECTION (–90dB MINIMUM)
- 0.0015% INL
- 21 BITS EFFECTIVE RESOLUTION (PGA = 1), 19 BITS (PGA = 128)
- PGA GAINS FROM 1 TO 128
- SINGLE CYCLE SETTLING
- PROGRAMMABLE DATA OUTPUT RATES
- EXTERNAL DIFFERENTIAL REFERENCE OF 0.1V TO 5V
- ON-CHIP CALIBRATION
- SPI™ COMPATIBLE
- 2.7V TO 5.25V SUPPLY RANGE
- 600μW POWER CONSUMPTION
- UP TO EIGHT INPUT CHANNELS
- UP TO EIGHT DATA I/O

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- LIQUID/GAS CHROMATOGRAPHY
- BLOOD ANALYSIS
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTATION
- WEIGHT SCALES

SPI is a registered trademark of Motorola.

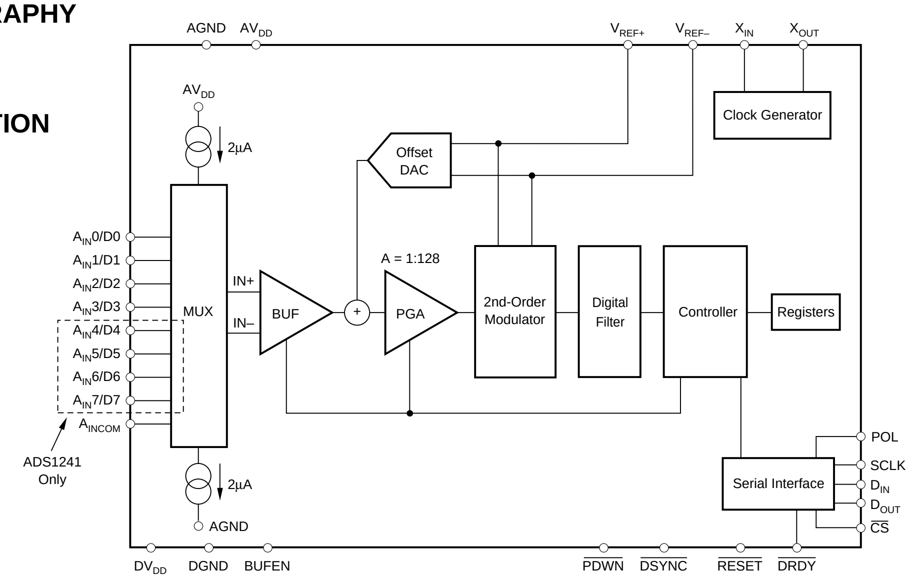
DESCRIPTION

The ADS1240 and ADS1241 are precision, wide dynamic range, delta-sigma, Analog-to-Digital (A/D) converters with 24-bit resolution operating from 2.7V to 5.25V supplies. The delta-sigma, A/D converter provides up to 24 bits of no missing code performance and effective resolution of 21 bits.

The input channels are multiplexed. Internal buffering can be selected to provide a very high input impedance for direct connection to transducers or low-level voltage signals. Burnout current sources are provided that allow for the detection of an open or shorted sensor. An 8-bit Digital-to-Analog (D/A) converter provides an offset correction with a range of 50% of the FSR (Full-Scale Range).

The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 with an effective resolution of 19 bits at a gain of 128. The A/D conversion is accomplished with a second-order delta-sigma modulator and programmable FIR filter that provides a simultaneous 50Hz and 60Hz notch. The reference input is differential and can be used for ratiometric conversion.

The serial interface is SPI compatible. Up to eight bits of data I/O are also provided that can be used for input or output. The ADS1240 and ADS1241 are designed for high-resolution measurement applications in smart transmitters, industrial process control, weight scales, chromatography, and portable instrumentation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to GND	–0.3V to +6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
A_{IN}	GND –0.5V to AV_{DD} + 0.5V
Digital Input Voltage to GND	–0.3V to DV_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to DV_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–60°C to +100°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
ADS1240E	SSOP-24	dB	–40 to +85	ADS1240E	ADS1240E	Rails
"	"	"	"	"	ADS1240E/1K	Tape and Reel
ADS1241E	SSOP-28	dB	–40 to +85	ADS1241E	ADS1241E	Rails
"	"	"	"	"	ADS1241E/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "ADS1240E/1K" will get a single 1000-piece Tape and Reel.

DIGITAL CHARACTERISTICS: T_{MIN} to T_{MAX}, DV_{DD} 2.7V to 5.25V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input/Output					
Logic Family			CMOS		
Logic Level: V_{IH}		0.8 • DV_{DD}		DV_{DD}	V
V_{IL}		DGND		0.2 • DV_{DD}	V
V_{OH}	I_{OH} = 1mA	DV_{DD} – 0.4			V
V_{OL}	I_{OL} = 1mA	DGND		DGND + 0.4	V
Input Leakage: I_{IH}	$V_I = DV_{DD}$			10	µA
I_{IL}	$V_I = 0$	–10			µA
Master Clock Rate: f_{OSC}		1		5	MHz
Master Clock Period: t_{OSC}	$1/f_{OSC}$	200		1000	ns

ELECTRICAL CHARACTERISTICS: AV_{DD} = 5V

All specifications T_{MIN} to T_{MAX}, AV_{DD} = +5V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, f_{DATA} = 15Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1240 ADS1241 MIN	TYP	MAX	UNITS
ANALOG INPUT ($A_{IN}0$ – $A_{IN}7$, A_{INCOM})					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 0.05		AV_{DD} – 1.5	V
Full-Scale Input Range	(In+) – (In–), See Block Diagram, RANGE = 0			$\pm V_{REF}$/PGA	V
	RANGE = 1			$\pm V_{REF}$/(2 • PGA)	V
Differential Input Impedance	Buffer OFF		5/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
f_{DATA} = 3.75Hz	–3dB		1.65		Hz
f_{DATA} = 7.50Hz	–3dB		3.44		Hz
f_{DATA} = 15.00Hz	–3dB		14.6		Hz
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator OFF, T = 25°C		5		pA
Burnout Current Sources			2		µA
OFFSET DAC					
Offset DAC Range	RANGE = 0		$\pm V_{REF}$/(2 • PGA)		V
	RANGE = 1		$\pm V_{REF}$/(4 • PGA)		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±10		%
Offset DAC Gain Error Drift			1		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
No Missing Codes				24	Bits
Integral Non-Linearity	End Point Fit			±0.0015	% of FS
Offset Error (1)			7.5		ppm of FS
Offset Drift (1)			0.02		ppm of FS/°C
Gain Error (1)			0.005		%
Gain Error Drift (1)			0.5		ppm/°C
Common-Mode Rejection	at DC	100			dB
	f_{CM} = 60Hz, f_{DATA} = 15Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 15Hz		120		dB
Normal-Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 15Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 15Hz		100		dB
Output Noise			See Typical Characteristics		
Power-Supply Rejection	at DC, dB = –20 log($\Delta V_{OUT}/\Delta V_{DD}$) (2)	80	95		dB
VOLTAGE REFERENCE INPUT					
Reference Input Range	REF IN+, REF IN–	0		AV_{DD}	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–), RANGE = 0	0.1	2.5	2.6	V
	RANGE = 1	0.1		AV_{DD}	V
Common-Mode Rejection	at DC		120		dB
Common-Mode Rejection	f_{VREFCM} = 60Hz, f_{DATA} = 15Hz		120		dB
Bias Current (3)	V_{REF} = 2.5V		1.3		µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	AV_{DD}	4.75		5.25	V
Analog Current	$\overline{PDWN}$ = 0, or SLEEP		1		nA
	PGA = 1, Buffer OFF		160	250	µA
	PGA = 128, Buffer OFF		470	675	µA
	PGA = 1, Buffer ON		210	300	µA
	PGA = 128, Buffer ON		880	1275	µA
Digital Current	Normal Mode, DV_{DD} = 5V		80	125	µA
	SLEEP Mode, DV_{DD} = 5V		60		µA
	Read Data Continuous Mode, DV_{DD} = 5V		230		µA
	$\overline{PDWN}$		0.5		nA
Power Dissipation	PGA = 1, Buffer OFF, DV_{DD} = 5V		1.2	1.9	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Calibration can minimize these errors. (2) ΔV_{OUT} is a change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

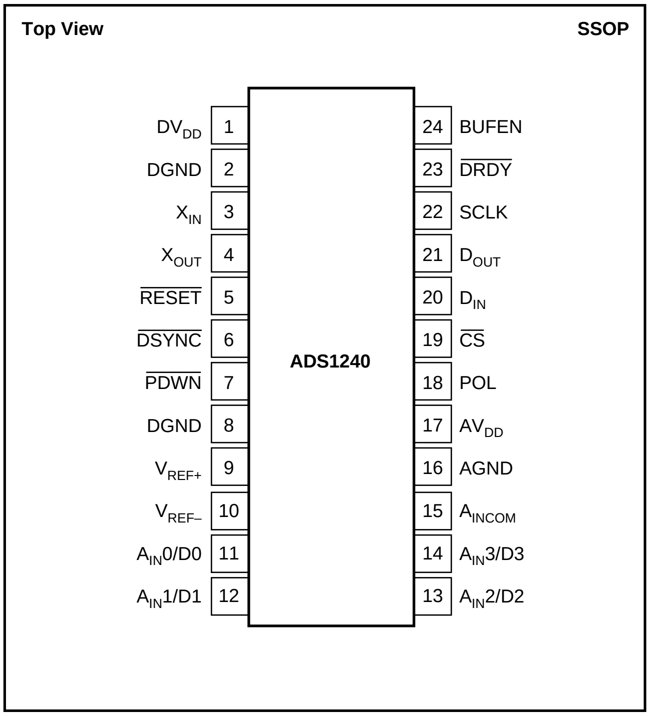
ELECTRICAL CHARACTERISTICS: AV_{DD} = 3V

All specifications T_{MIN} to T_{MAX}, AV_{DD} = +3V, DV_{DD} = +2.7V to 5.25V, f_{MOD} = 19.2kHz, PGA = 1, Buffer ON, f_{DATA} = 15Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +1.25V, unless otherwise specified.

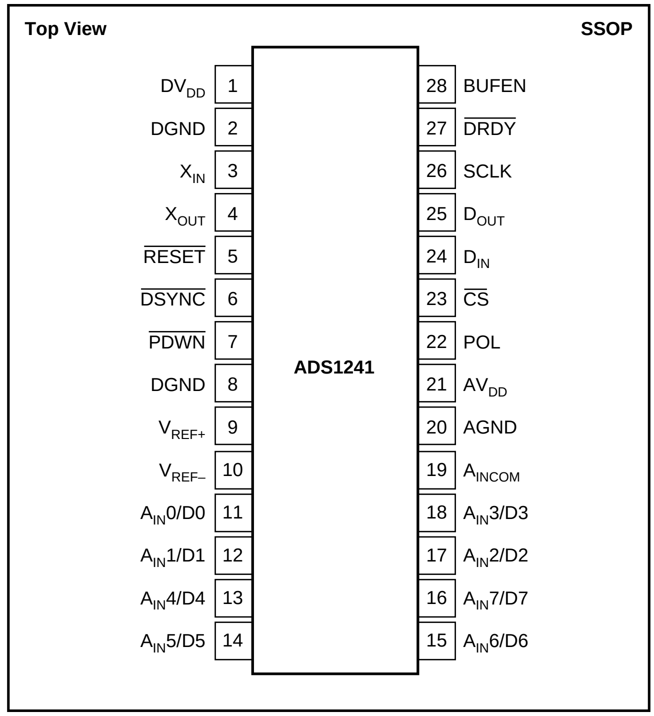
PARAMETER	CONDITIONS	ADS1240 ADS1241 MIN	TYP	MAX	UNITS
ANALOG INPUT ($A_{IN}0$ – $A_{IN}7$, A_{INCOM})					
Analog Input Range	Buffer OFF	AGND – 0.1		AV_{DD} + 0.1	V
	Buffer ON	AGND + 0.05		AV_{DD} – 1.5	V
Full-Scale Input Voltage Range	(In+) – (In–) See Block Diagram, RANGE = 0			$\pm V_{REF}$/PGA	V
	RANGE = 1			$\pm V_{REF}$/(2 • PGA)	V
Input Impedance	Buffer OFF		5/PGA		MΩ
Input Current	Buffer ON		0.5		nA
Bandwidth					
f_{DATA} = 3.75Hz	–3dB		1.65		Hz
f_{DATA} = 7.50Hz	–3dB		3.44		Hz
f_{DATA} = 15.00Hz	–3dB		14.6		Hz
Programmable Gain Amplifier	User-Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator OFF, T = 25°C		5		pA
Burnout Current Sources			2		µA
OFFSET DAC					
Offset DAC Range	RANGE = 0		$\pm V_{REF}$/(2 • PGA)		V
	RANGE = 1		$\pm V_{REF}$/(4 • PGA)		V
Offset DAC Monotonicity		8			Bits
Offset DAC Gain Error			±10		%
Offset DAC Gain Error Drift			2		ppm/°C
SYSTEM PERFORMANCE					
Resolution		24			Bits
No Missing Codes				24	Bits
Integral Non-Linearity	End Point Fit			±0.0015	% of FS
Offset Error(1)			15		ppm of FS
Offset Drift(1)			0.04		ppm of FS/°C
Gain Error(1)			0.01		%
Gain Error Drift(1)			1.0		ppm/°C
Common-Mode Rejection	at DC	100			dB
	f_{CM} = 60Hz, f_{DATA} = 15Hz		130		dB
	f_{CM} = 50Hz, f_{DATA} = 15Hz		120		dB
Normal-Mode Rejection	f_{SIG} = 50Hz, f_{DATA} = 15Hz		100		dB
	f_{SIG} = 60Hz, f_{DATA} = 15Hz		100		dB
Output Noise			See Typical Characteristics		
Power-Supply Rejection	at DC, dB = –20 log($\Delta V_{OUT}/\Delta V_{DD}$)(2)	75	90		dB
VOLTAGE REFERENCE INPUT					
Reference Input Range	REF IN+, REF IN–	0		AV_{DD}	V
V_{REF}	V_{REF} ≡ (REF IN+) – (REF IN–), RANGE = 0	0.1	1.25	1.30	V
	RANGE = 1	0.1	2.5	2.6	V
Common-Mode Rejection	at DC		120		dB
Common-Mode Rejection	f_{VREFCM} = 60Hz, f_{DATA} = 15Hz		120		dB
Bias Current(3)	V_{REF} = 1.25		0.65		µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	AV_{DD}	2.7		3.3	V
Analog Current	$\overline{PDWN}$ = 0, or SLEEP		1		nA
	PGA = 1, Buffer OFF		140	225	µA
	PGA = 128, Buffer OFF		410	600	µA
	PGA = 1, Buffer ON		190	275	µA
	PGA = 128, Buffer ON		820	1225	µA
Digital Current	Normal Mode, DV_{DD} = 3V		50	100	µA
	SLEEP Mode, DV_{DD} = 3V		75		µA
	Read Data Continuous Mode, DV_{DD} = 3V		113		µA
	$\overline{PDWN}$ = 0		0.5		nA
Power Dissipation	PGA = 1, Buffer OFF, DV_{DD} = 3V		0.6	1.2	mW
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–60		+100	°C

NOTES: (1) Calibration can minimize these errors. (2) ΔV_{OUT} is a change in digital result. (3) 12pF switched capacitor at f_{SAMP} clock frequency.

PIN CONFIGURATION (ADS1240)



PIN CONFIGURATION (ADS1241)



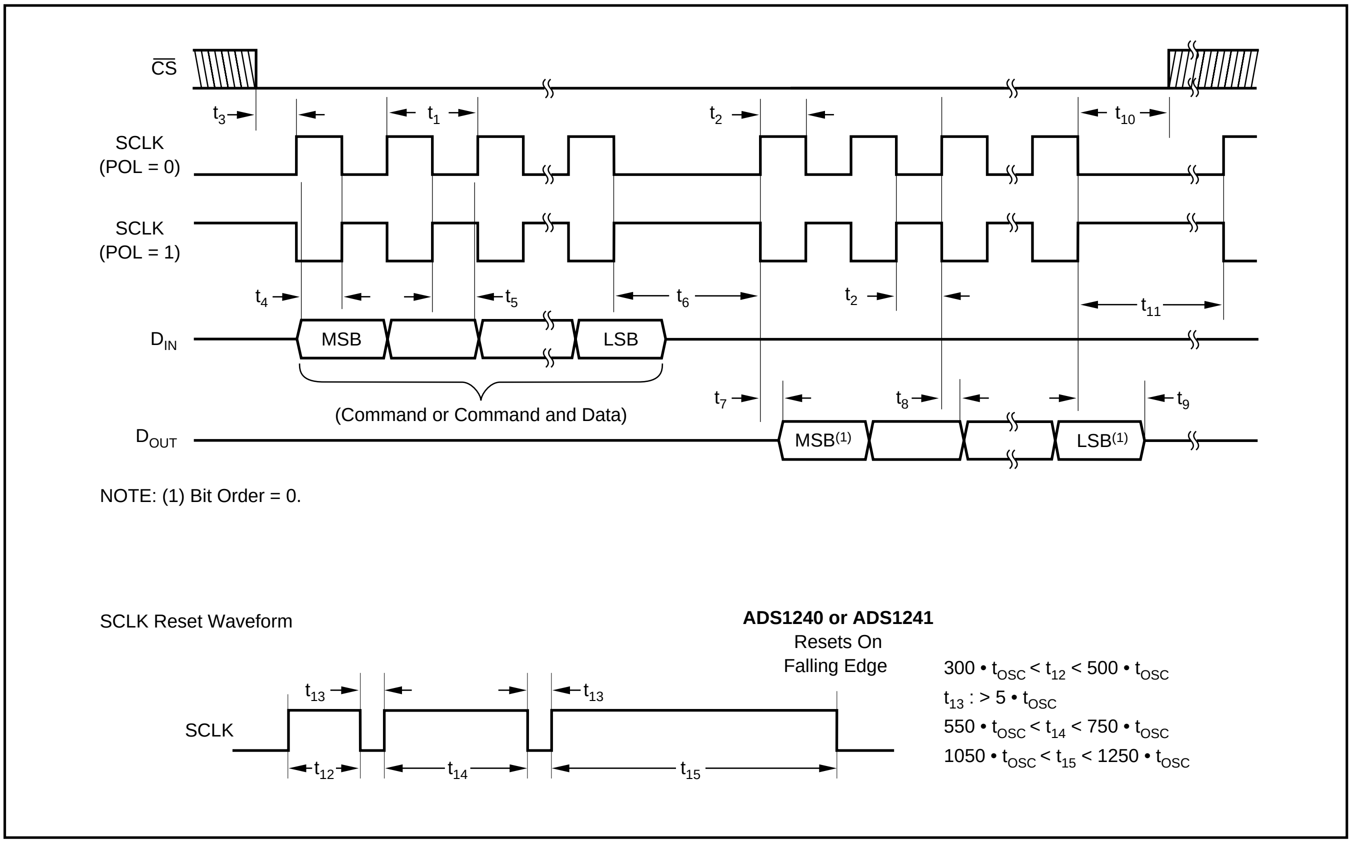
PIN DESCRIPTIONS (ADS1240)

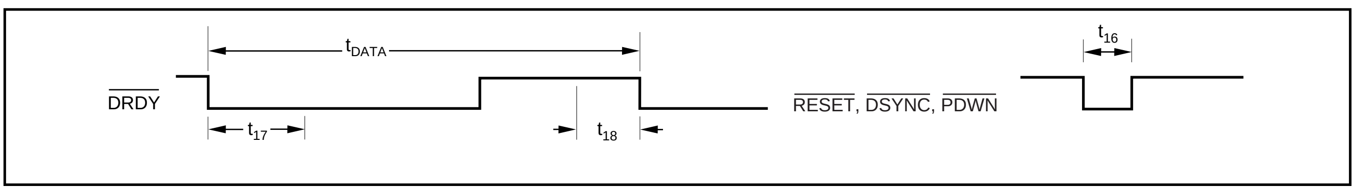
PIN NUMBER	NAME	DESCRIPTION
1	DV$_{DD}$	Digital Power Supply
2	DGND	Digital Ground
3	X$_{IN}$	Clock Input
4	X$_{OUT}$	Clock Output, used with crystal or ceramic resonator.
5	$\overline{\text{RESET}}$	Active LOW, resets the entire device.
6	$\overline{\text{DSYNC}}$	Synchronization Control.
7	$\overline{\text{PDWN}}$	Active LOW. Power Down. The power down function shuts down the analog and digital circuits.
8	DGND	Digital Ground
9	V$_{REF+}$	Positive Differential Reference Input
10	V$_{REF-}$	Negative Differential Reference Input
11	A$_{IN}$0/D0	Analog Input 0/Data I/O 0
12	A$_{IN}$1/D1	Analog Input 1/Data I/O 1
13	A$_{IN}$2/D2	Analog Input 2/Data I/O 2
14	A$_{IN}$3/D3	Analog Input 3/Data I/O 3
15	A$_{INCOM}$	Analog Input Common
16	AGND	Analog Ground
17	AV$_{DD}$	Analog Power Supply
18	POL	Serial Clock Polarity
19	$\overline{\text{CS}}$	Active LOW, Chip Select
20	D$_{IN}$	Serial Data Input, Schmitt Trigger
21	D$_{OUT}$	Serial Data Output
22	SCLK	Serial Clock, Schmitt Trigger
23	$\overline{\text{DRDY}}$	Active LOW, Data Ready
24	BUFEN	Buffer Enable

PIN DESCRIPTIONS (ADS1241)

PIN NUMBER	NAME	DESCRIPTION
1	DV$_{DD}$	Digital Power Supply
2	DGND	Digital Ground
3	X$_{IN}$	Clock Input
4	X$_{OUT}$	Clock Output, used with crystal or ceramic resonator.
5	$\overline{\text{RESET}}$	Active LOW, entire device.
6	$\overline{\text{DSYNC}}$	Synchronization Control.
7	$\overline{\text{PDWN}}$	Active LOW. Power Down. The power down function shuts down the analog and digital circuits.
8	DGND	Digital Ground
9	V$_{REF+}$	Positive Differential Reference Input
10	V$_{REF-}$	Negative Differential Reference Input
11	A$_{IN}$0/D0	Analog Input 0/Data I/O 0
12	A$_{IN}$1/D1	Analog Input 1/Data I/O 1
13	A$_{IN}$4/D4	Analog Input 4/Data I/O 4
14	A$_{IN}$5/D5	Analog Input 5/Data I/O 5
15	A$_{IN}$6/D6	Analog Input 6/Data I/O 6
16	A$_{IN}$7/D7	Analog Input 7/Data I/O 7
17	A$_{IN}$2/D2	Analog Input 2/Data I/O 2
18	A$_{IN}$3/D3	Analog Input 3/Data I/O 3
19	A$_{INCOM}$	Analog Input Common, connect to AGND if unused.
20	AGND	Analog Ground
21	AV$_{DD}$	Analog Power Supply
22	POL	Serial Clock Polarity
23	$\overline{\text{CS}}$	Active LOW, Chip Select
24	D$_{IN}$	Serial Data Input, Schmitt Trigger
25	D$_{OUT}$	Serial Data Output
26	SCLK	Serial Clock, Schmitt Trigger
27	$\overline{\text{DRDY}}$	Active LOW, Data Ready
28	BUFEN	Buffer Enable

TIMING CHARACTERISTICS





TIMING CHARACTERISTICS TABLES

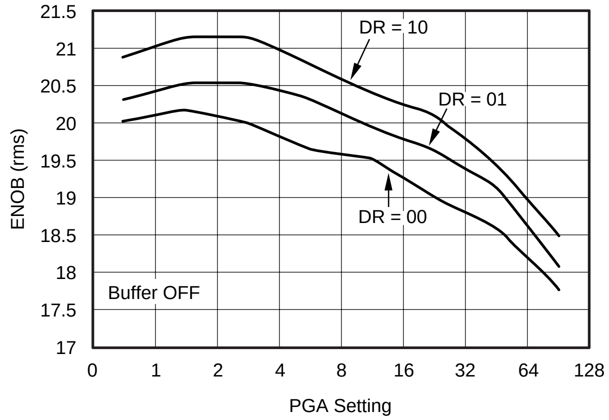
SPEC	DESCRIPTION	MIN	MAX	UNITS
t_1	SCLK Period	4		t_{OSC} Periods
			3	$\overline{\text{DRDY}}$ Periods
t_2	SCLK Pulse Width, HIGH and LOW	200		ns
t_3	$\overline{\text{CS}}$ low to first SCLK Edge; Setup Time(2)	0		ns
t_4	D_{IN} Valid to SCLK Edge; Setup Time	50		ns
t_5	Valid D_{IN} to SCLK Edge; Hold Time	50		ns
t_6	Delay between last SCLK edge for D_{IN} and first SCLK edge for D_{OUT}:			
	RDATA, RDATAC, RREG, WREG	50		t_{OSC} Periods
t_7(1)	SCLK Edge to Valid New D_{OUT}		50	ns
t_8(1)	SCLK Edge to D_{OUT}, Hold Time	0		ns
t_9	Last SCLK Edge to D_{OUT} Tri-State	6	10	t_{OSC} Periods
	NOTE: D_{OUT} goes tri-state immediately when $\overline{\text{CS}}$ goes HIGH.			
t_{10}	$\overline{\text{CS}}$ LOW time after final SCLK edge.	0		ns
t_{11}	Final SCLK edge of one command until first edge SCLK of next command:			
	RREG, WREG $\overline{\text{DSYNC}}$, SLEEP, $\overline{\text{RESET}}$, RDATA, RDATAC, STOPC	4		t_{OSC} Periods
	SELFGCAL, SELFOCAL, SYSOCAL, SYSGCAL	2		$\overline{\text{DRDY}}$ Periods
	SELFCAL	4		$\overline{\text{DRDY}}$ Periods
	$\overline{\text{RESET}}$ (also SCLK Reset or $\overline{\text{RESET}}$ Pin)	16		t_{OSC} Periods
t_{16}	Pulse Width	4		t_{OSC} Periods
t_{17}	Allowed analog input change for next valid conversion		5000	t_{OSC} Periods
t_{18}	DOR update, DOR data not valid	4		t_{OSC} Periods

NOTE: (1) Load = 20pF || 10kΩ to DGND. (2) $\overline{\text{CS}}$ may be tied LOW.

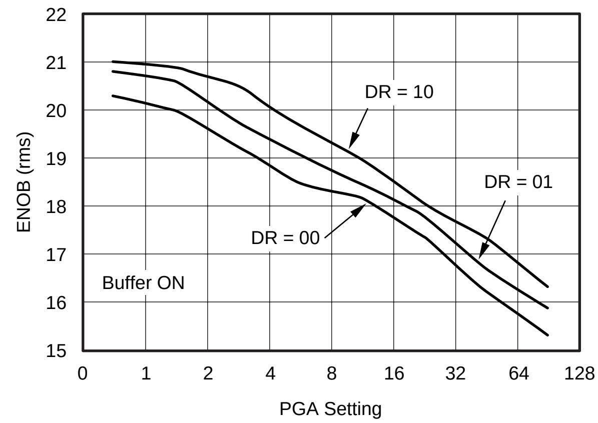
TYPICAL CHARACTERISTICS

All specifications, AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, f_{DATA} = 15Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

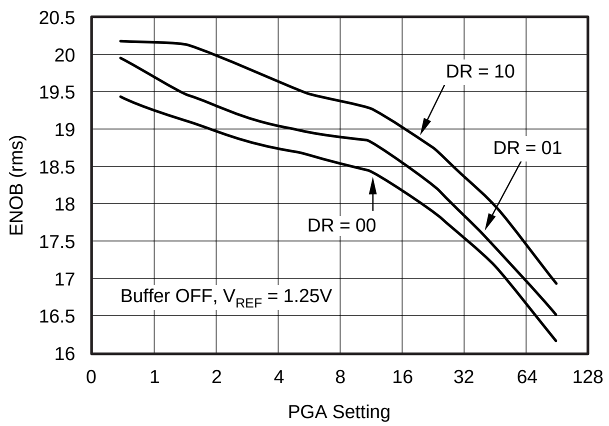
EFFECTIVE NUMBER OF BITS vs PGA SETTING



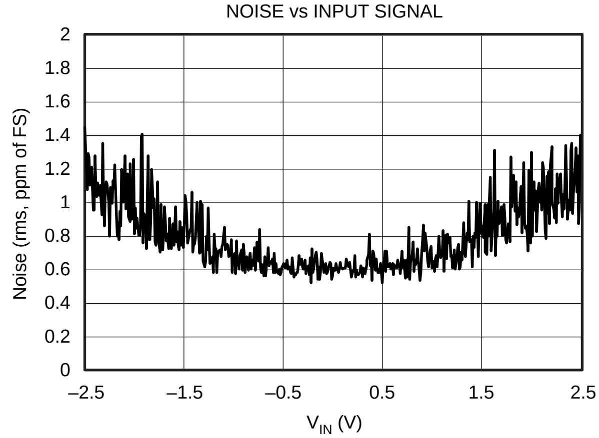
EFFECTIVE NUMBER OF BITS vs PGA SETTING



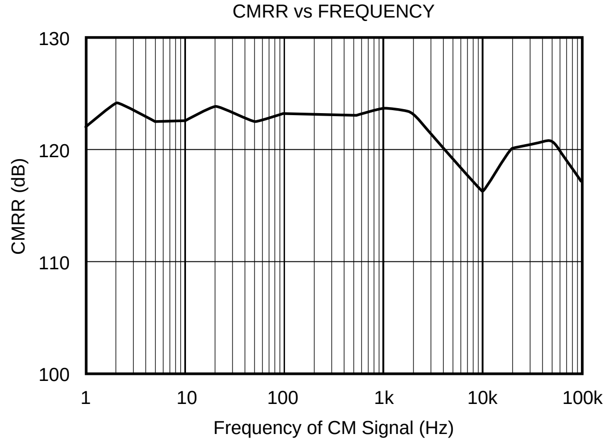
EFFECTIVE NUMBER OF BITS vs PGA SETTING



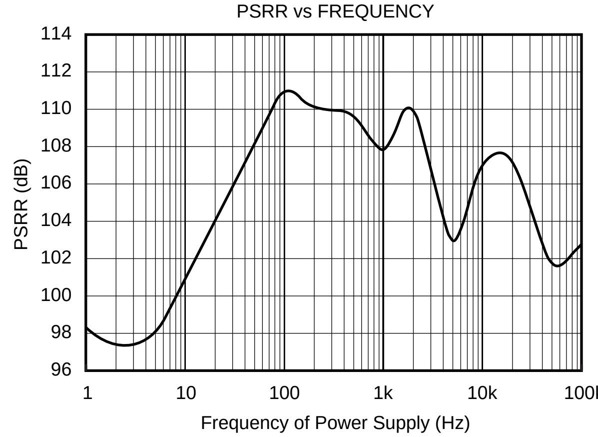
NOISE vs INPUT SIGNAL



CMRR vs FREQUENCY

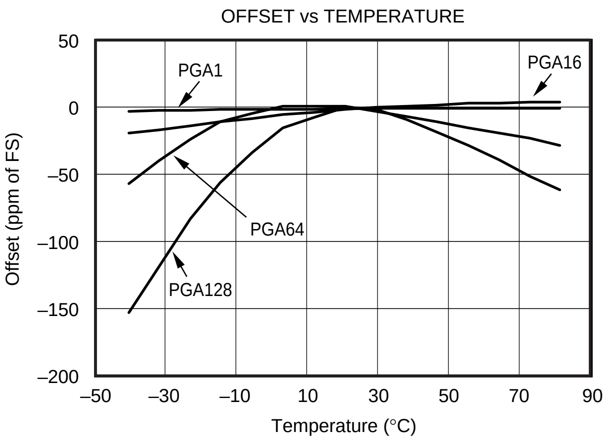


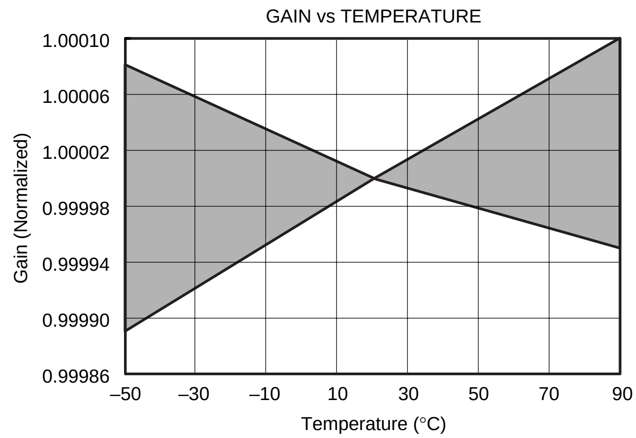
PSRR vs FREQUENCY

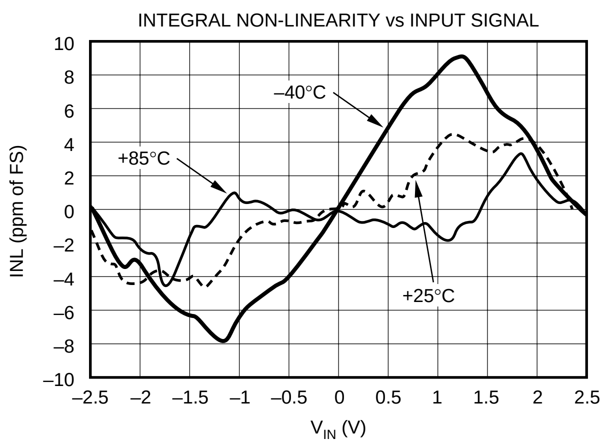


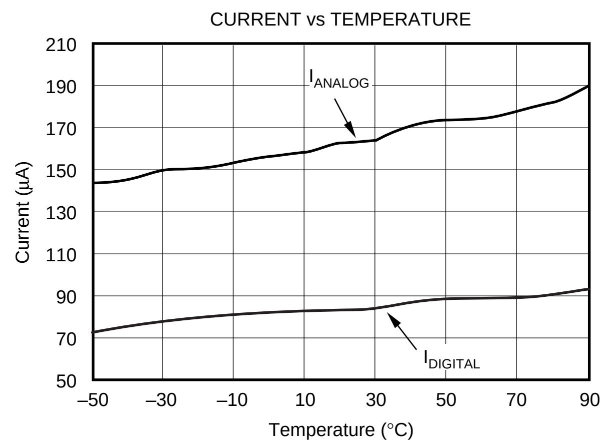
TYPICAL CHARACTERISTICS (Cont.)

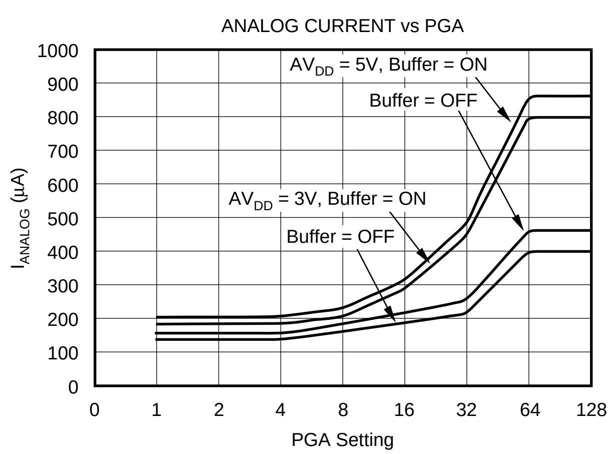
All specifications, AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, f_{DATA} = 15Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.

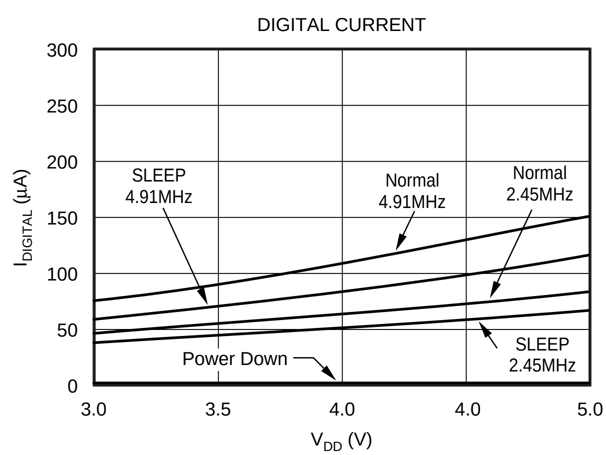






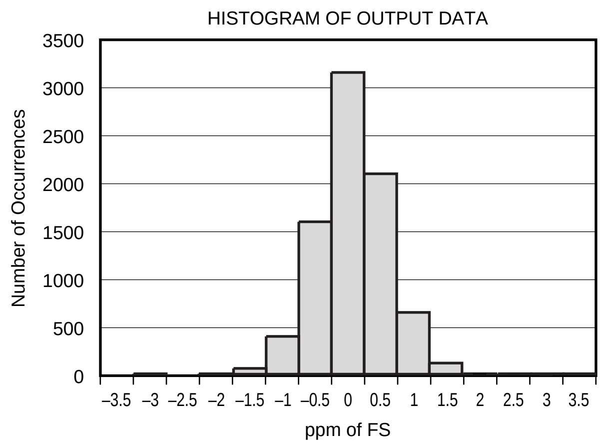


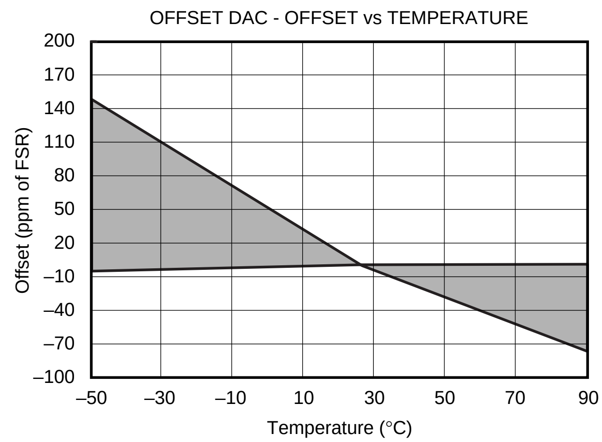


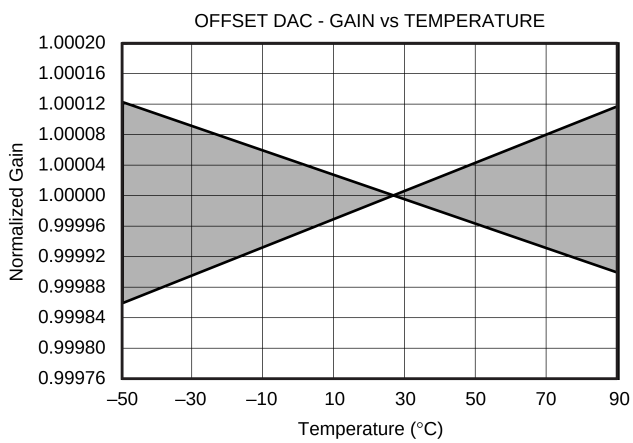


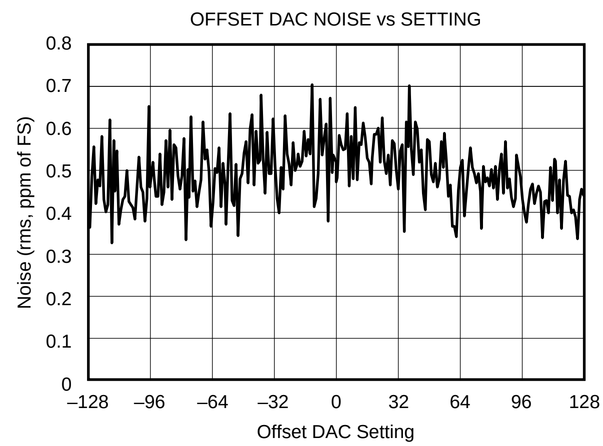
TYPICAL CHARACTERISTICS (Cont.)

All specifications, AV_{DD} = +5V, DV_{DD} = +5V, f_{OSC} = 2.4576MHz, PGA = 1, f_{DATA} = 15Hz, V_{REF} ≡ (REF IN+) – (REF IN–) = +2.5V, unless otherwise specified.









OVERVIEW

INPUT MULTIPLEXER

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown in Figure 1. For Example, if $A_{IN}0$ is selected as the positive differential input channel, any other channel can be selected as the negative differential input channel. Under this method, it is possible to have up to eight fully differential input channels for the ADS1241, and four differential input pins for the ADS1240.

In addition, current sources are supplied that will source or sink current to detect open or short circuits on the input pins.

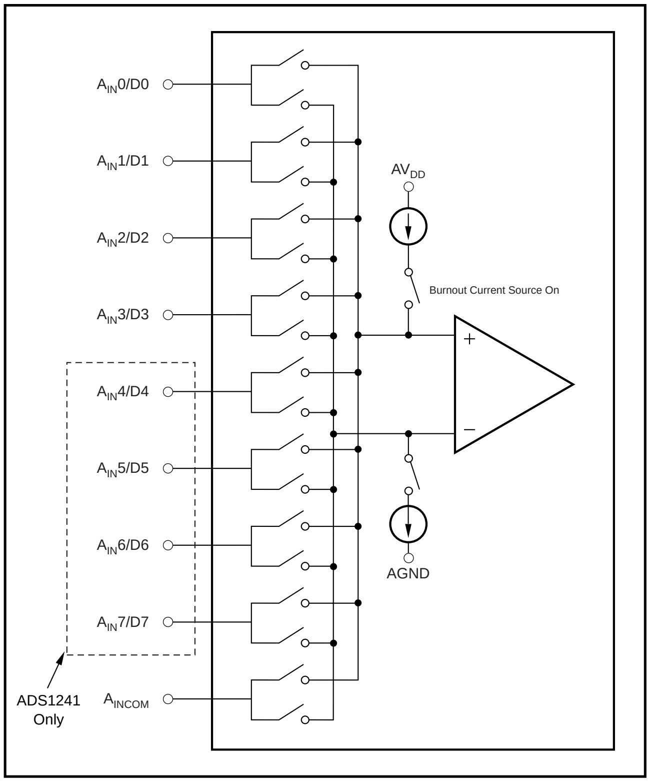


FIGURE 1. Input Multiplexer Configuration.

BURNOUT CURRENT SOURCES

When the Burnout bit is set in the ACR configuration register, two current sources are enabled. The current source on the positive input channel sources approximately 2µA of current. The current source on the negative input channel sinks approximately 2µA. This allows for the detection of an open circuit (full-scale reading) or short circuit (0V differential reading) on the selected input differential pair.

INPUT BUFFER

The input impedance of the ADS1240 and ADS1241 without the buffer is 5MΩ/PGA. With the buffer enabled the input voltage range is reduced, and the analog power-supply current is higher. The buffer is controlled by ANDing the state of the buffer pin with the state of the BUFFER bit in the ACR register.

PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can actually improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 5V full-scale signal, the A/D converter can resolve up to 1µV. With a PGA of 128 and a full-scale signal of 40mV, the A/D converter can resolve up to 75nV. With a PGA of 1, this would require a 26-bit A/D converter to resolve up to 75nV. AV_{DD} current increases with higher PGA settings.

PGA OFFSET DAC

The input to the PGA can be shifted by half the full-scale input range of the PGA using the ODAC (Offset DAC) register. The ODAC register is an 8-bit value; the MSB is the sign and the seven LSBs provide the magnitude of the offset. Using the offset DAC does not reduce the performance of the A/D converter.

MODULATOR

The modulator is a single-loop second-order system. The modulator runs at a clock speed (f_{MOD}) that is derived from the external clock (f_{OSC}). The frequency division is determined by the SPEED bit in the SETUP register, as shown in Table I. For the same DATA RATE Bit selection, the noise performance will be the same regardless of output rate.

f_{OSC}	SPEED BIT	f_{MOD}	DATA RATE 00	DATA RATE 01	DATA RATE 10	1st NOTCH FREQ.
2.4576MHz	0	19,200Hz	15Hz	7.5Hz	3.75Hz	50/60Hz
	1	9,600Hz	7.5Hz	3.75Hz	1.875Hz	25/30Hz
4.9152MHz	0	38,400Hz	30Hz	15Hz	7.5Hz	100/120Hz
	1	19,200Hz	15Hz	7.5Hz	3.75Hz	50/60Hz

TABLE I. Output Configuration.

CALIBRATION

The offset and gain errors in the ADS1240 and ADS1241, or the complete system, can be minimized with calibration. Internal calibration of the ADS1240 and ADS1241 is called self calibration. This is handled with three commands. One command does both offset and gain calibration. There is also a gain calibration command and an offset calibration command. Each calibration process takes two t_{DATA} periods to complete. Therefore, it takes four t_{DATA} periods to complete both an offset and gain calibration.

For system calibration, the appropriate signal must be applied to the differential inputs. The system offset command requires a "zero" input differential signal. It then computes an offset that will nullify offset in the differential system. The system gain command requires a positive "full-scale" input signal. It then computes a value to nullify gain errors in the system. Each of these calibrations will take two t_{DATA} periods to complete.

Calibration should be performed after power on, a change in temperature, or a change of the PGA. The RANGE bit (ACR bit 2) must be zero during calibration. For operation with a reference voltage greater than (AV_{DD} – 1.5) volts, the buffer must also be turned off during calibration.

Calibration will remove the effects of the ODAC, therefore, changes to the ODAC register must be done after calibration, otherwise the calibration will remove the effects of the offset.

At the completion of calibration, the $\overline{DRDY}$ signal goes low which indicates the calibration is finished and valid data is available.

DIGITAL FILTER

The ADS1240 and ADS1241 have a 1279 taps modified linear phase digital filter on board that a user can configure various output data rates. When a 2.4576MHz crystal is used, the device can be programmed to an output data rate of 15Hz, 7.5Hz, or 3.75Hz. Under these conditions, the digital filter rejects both 50Hz and 60Hz interference down to at least –90dB of full-scale input. Figure 2 shows the various conditions that the user can configure ADS1240 and ADS1241 on-board digital filter to perform various data output rates to get different line rejection frequencies.

If a different data output rate is desired, a different crystal frequency can be used. However, the rejection frequencies will shift accordingly. For example, 3.6864MHz CLK with default register condition will have:

(3.6864MHz/2.4576MHz) • 15Hz = 22.5Hz of data output rate

and the first and second notch will be:

1.5 • (50Hz and 60Hz) = 75Hz and 90Hz

EXTERNAL VOLTAGE REFERENCE

The ADS1240 and ADS1241 require an external voltage reference. The selection for the voltage reference value is made through the ACR register.

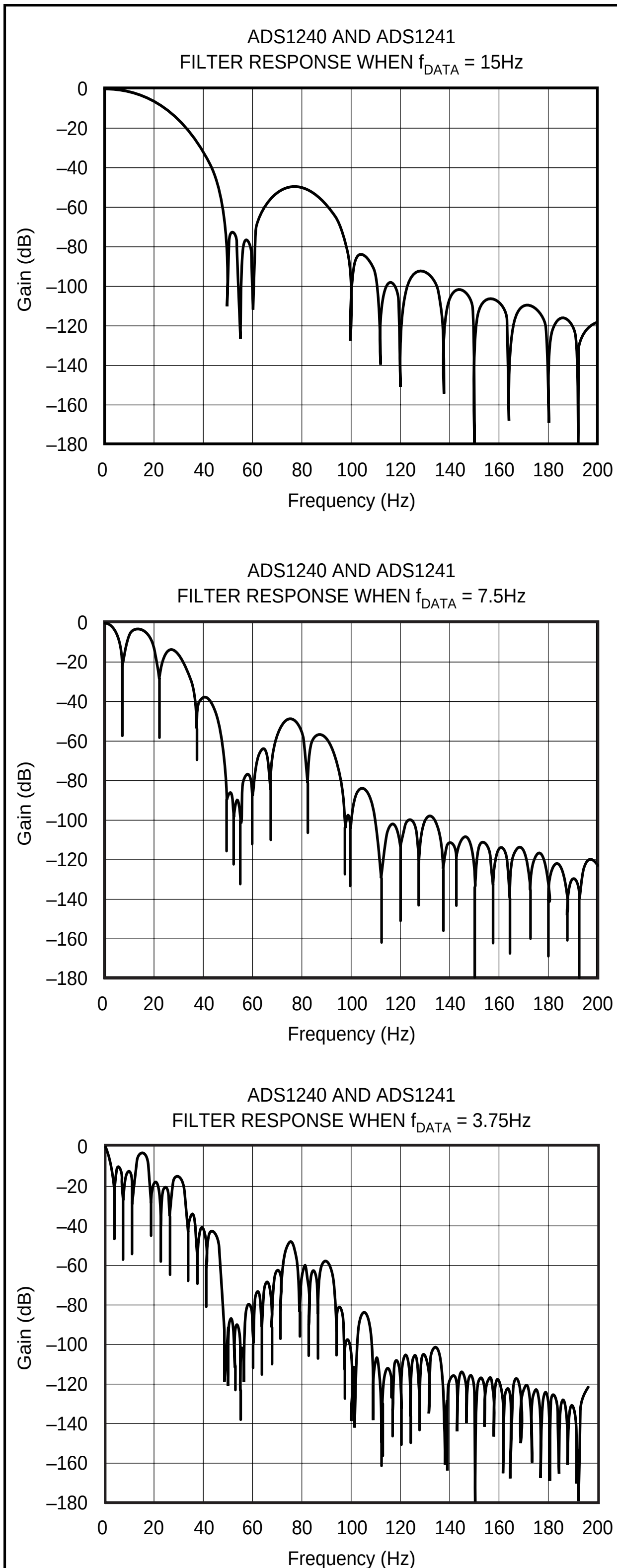
The external voltage reference is differential and is represented by the voltage difference between the pins: $+V_{REF}$ and $-V_{REF}$. The absolute voltage on either pin, $+V_{REF}$ or $-V_{REF}$, can range from AGND to AV_{DD}. However, the following limitations apply:

For AV_{DD} = 5.0V and RANGE = 0 in the ACR, the differential V_{REF} must not exceed 2.5V.

For AV_{DD} = 5.0V and RANGE = 1 in the ACR, the differential V_{REF} must not exceed 5V.

For AV_{DD} = 3.0V and RANGE = 0 in the ACR, the differential V_{REF} must not exceed 1.25V.

For AV_{DD} = 3.0V and RANGE = 1 in the ACR, the differential V_{REF} must not exceed 2.5V.



f_{OSC} = 2.4576MHz, SPEED = 0 or f_{OSC} = 4.9152MHz, SPEED = 1

DATA OUTPUT RATE	–3dB BANDWIDTH	50Hz	60Hz	100Hz	120Hz
15Hz	14.6Hz	–95dB	–93dB	–107dB	–109dB
7.5Hz	3.44Hz	–109dB	–99dB	–109dB	–108dB
3.75	1.65Hz	–108dB	–111dB	–112dB	–109dB

FIGURE 2. Filter Frequency Responses.

CLOCK GENERATOR

The clock source for the ADS1240 and ADS1241 can be provided from a crystal, ceramic resonator, oscillator, or external clock. When the clock source is a crystal or ceramic resonator, external capacitors must be provided to ensure start-up and stable clock frequency. This is shown in Figure 3 and Table II.

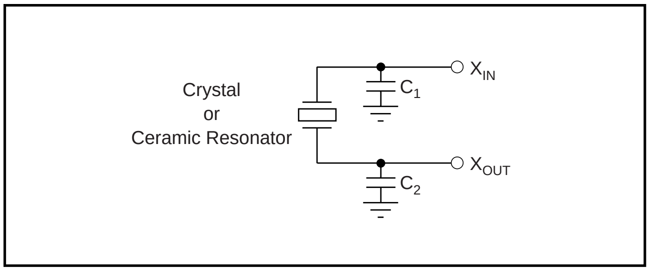


FIGURE 3. Crystal or Ceramic Resonator Connection.

CLOCK SOURCE	FREQUENCY	C_1	C_2	PART NUMBER
Crystal	2.4576	0-20pF	0-20pF	ECS, ECSD 2.45 - 32
Crystal	4.9152	0-20pF	0-20pF	ECS, ECSL 4.91
Crystal	4.9152	0-20pF	0-20pF	ECS, ECSD 4.91
Crystal	4.9152	0-20pF	0-20pF	CTS, MP 042 4M9182

TABLE II. Typical Clock Sources.

DATA I/O INTERFACE

The ADS1240 has four pins and the ADS1241 has eight pins that serve a dual purpose as both analog inputs and data I/O. These pins are powered from AV_{DD} and are configured through the IOCON, DIR, and DIO registers. These pins can be individually configured as either analog inputs or data I/O.

The IOCON register defines the pin as either an analog input or data I/O. The default power-up state is an analog input. If the pin is configured as an analog input in the IOCON register, the DIR and DIO registers have no effect on the state of the pin.

If the pin is configured as data I/O in the IOCON register, then DIR and DIO are used to control the state of the pin. The DIR register controls the direction of the data pin, either as an input or output. If the pin is configured as an input in the DIR register, then the corresponding DIO register bit reflects the state of the pin. If the pin is configured as an output in the DIR register, then the corresponding DIO register bit value determines the state of the output pin (0 = AGND, 1 = AV_{DD}).

It is still possible to perform A/D conversions on a pin configured as data I/O. This may be useful as a test mode, where the data I/O pin is driven and an A/D conversion is done on the pin.

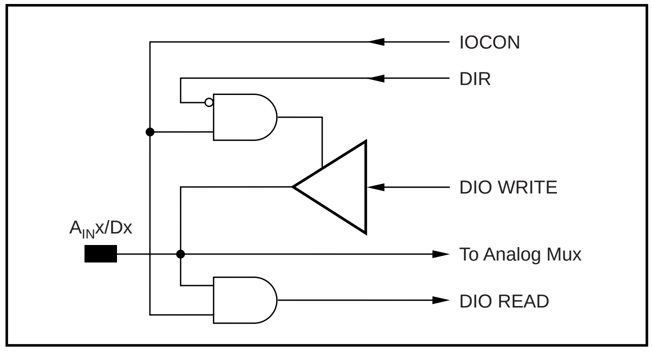


FIGURE 4. Analog/Data Interface Pin.

SERIAL INTERFACE

The serial interface is a standard four-wire SPI compatible (D_{IN}, D_{OUT}, SCLK, and $\overline{\text{CS}}$). The ADS1240 and ADS1241 also offer the flexibility to select the polarity of the serial clock through the POL pin. The serial interface can be clocked up to $f_{OSC}/4$. If $\overline{\text{CS}}$ goes HIGH the serial interface is reset. when $\overline{\text{CS}}$ goes LOW, a new command is expected. Serial communications can occur independent of $\overline{\text{DRDY}}$. $\overline{\text{DRDY}}$ only indicates the validity of data in the data output register.

$\overline{\text{DSYNC}}$ OPERATION

$\overline{\text{DSYNC}}$ is used to provide precise synchronization of the A/D conversion with an external event. Synchronization can be achieved either through the $\overline{\text{DSYNC}}$ pin or the $\overline{\text{DSYNC}}$ command. When the $\overline{\text{DSYNC}}$ pin is used, the filter counter is reset on the falling edge of $\overline{\text{DSYNC}}$. The modulator is held in reset until $\overline{\text{DSYNC}}$ is taken HIGH. Synchronization occurs on the next rising edge of the system clock after $\overline{\text{DSYNC}}$ is taken HIGH.

When the $\overline{\text{DSYNC}}$ command is sent, the filter counter is reset on the edge of the last SCLK on the $\overline{\text{DSYNC}}$ command. The modulator is held in $\overline{\text{RESET}}$ until the next edge of SCLK is detected. Synchronization occurs on the next rising edge of the system clock after the first SCLK after the $\overline{\text{DSYNC}}$ command.

POWER-UP—SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry was designed to accommodate digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically.

MEMORY

Sixteen registers directly control the various functions of the ADS1240 and ADS1241 can be directly read or written to. Collectively, the registers contain all the information needed to configure the part, such as data format, MUX settings, cal settings, data rate, etc.

RESET

There are three methods of reset. The $\overline{\text{RESET}}$ pin, SCLK pattern, and the RESET command. They all perform the same function.

ADS1240 AND ADS1241 REGISTER BANKS

The operation of the device is set up through individual registers. Collectively, the registers contain all the information needed to configure the part, such as data format, mux settings, cal settings, data rate, etc. The set of the 16 registers are shown in Table III.

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00_H	SETUP	ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0
01_H	MUX	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02_H	ACR	$\overline{DRDY}$	U/$\overline{B}$	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0
03_H	ODAC	SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0
04_H	DIO	DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
05_H	DIR	DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
06_H	IOCON	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
07_H	OCR0	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
08_H	OCR1	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
09_H	OCR2	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
$0A_H$	FSR0	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
$0B_H$	FSR1	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
$0C_H$	FSR2	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
$0D_H$	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
$0E_H$	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
$0F_H$	DOR0	DOR07	DOR16	FSR21	DOR04	DOR03	DOR02	DOR01	DOR00

TABLE III. Registers.

DETAILED REGISTER DEFINITIONS

SETUP (Address 00_H) Setup Register
Reset Value = iiii0000

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0

bit 7-4 Factory Programmed Bits

bit 3 BOCS: Burnout Current Source
0 = Disabled (default)
1 = Enabled

bit 2-0 PGA2: PGA1: PGA0: Programmable Gain Amplifier Gain Selection
000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

MUX (Address 01_H) Multiplexer Control Register
Reset Value = 01_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

bit 7-4 PSEL3: PSEL2: PSEL1: PSEL0: Positive Channel Select
0000 = $A_{IN}0$ (default)
0001 = $A_{IN}1$
0010 = $A_{IN}2$
0011 = $A_{IN}3$
0100 = $A_{IN}4$
0101 = $A_{IN}5$
0110 = $A_{IN}6$
0111 = $A_{IN}7$
1xxx = AINCOM (except when all bits are 1's)
1111 = Reserved

bit 3-0 NSEL3: NSEL2: NSEL1: NSEL0: Negative Channel Select
0000 = $A_{IN}0$
0001 = $A_{IN}1$ (default)
0010 = $A_{IN}2$
0011 = $A_{IN}3$
0100 = $A_{IN}4$
0101 = $A_{IN}5$
0110 = $A_{IN}6$
0111 = $A_{IN}7$
1xxx = AINCOM (except when all bits are 1's)
1111 = Reserved

ACR (Address 02_H) Analog Control Register
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$\overline{\text{DRDY}}$	U/$\overline{\text{B}}$	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0

bit 7 $\overline{\text{DRDY}}$: Data Ready (Read Only)
This bit duplicates the state of the $\overline{\text{DRDY}}$ signal.

bit 6 U/$\overline{\text{B}}$: Data Format
0 = Bipolar (default)
1 = Unipolar

U/$\overline{\text{B}}$	ANALOG INPUT	DIGITAL OUTPUT
0	+FSR Zero –FSR	0x7FFFFF 0x000000 0x800000
1	+FSR Zero –FSR	0xFFFFFF 0x000000 0x000000

bit 5 SPEED: Modulator Clock Speed
0 = $f_{MOD} = f_{OSC}/128$ (default)
1 = $f_{MOD} = f_{OSC}/256$

bit 4 BUFFER: Buffer Enable
0 = Buffer Disabled (default)
1 = Buffer Enabled

bit 3 BIT ORDER: Set Order Bits are Transmitted
0 = Most Significant Bit Transmitted First (default)
1 = Least Significant Bit Transmitted First

Data is always shifted into the part most significant bit first. Data is always shifted out of the part most significant byte first. This configuration bit only controls the bit order within the byte of data that is shifted out.

bit 2 RANGE: Range Select
0 = Full-Scale Output Range Equal to $\pm V_{REF}$ (default).
1 = Full-Scale Output Range Equal to $\pm 1/2\ V_{REF}$

NOTE: This allows reference voltages as high as AV_{DD}, but even with a 5V reference voltage the calibration must be performed with this bit set to 0.

bit 1-0 DR1: DR0: Data Rate (f_{OSC} = 2.4576MHz, SPEED = 0)
00 = 15Hz (default)
01 = 7.5Hz
10 = 3.75Hz
11 = Reserved

ODAC (Address 03_H) Offset DAC
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0

bit 7 Offset Sign
0 = Positive
1 = Negative

$$\text{Offset} = \frac{V_{REF}}{2 \bullet PGA} \bullet \left(\frac{\text{Code}}{127}\right) \quad \text{RANGE} = 0$$

$$\text{Offset} = \frac{V_{REF}}{4 \bullet PGA} \bullet \left(\frac{\text{Code}}{127}\right) \quad \text{RANGE} = 1$$

NOTE: The offset must be used after calibration or the calibration will nullify the effects.

DIO (Address 04_H) Data I/O
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIO 7	DIO 6	DIO 5	DIO 4	DIO 3	DIO 2	DIO 1	DIO 0

If the IOCON register is configured for data, a value written to this register will appear on the data I/O pins if the pin is configured as an output in the DIR register. Reading this register will return the value of the data I/O pins.

DIR (Address 05_H) Direction Control for Data I/O
Reset Value = FF_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIR7	DIR6	DIR5	DIR4	DIR3	DIR2	DIR1	DIR0

Each bit controls whether the data I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.

IOCON (Address 06_H) I/O Configuration Register
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

bit 7-0 IO7: IO0: Data I/O Configuration
0 = Analog (default)
1 = Data

Configuring the pin as a data I/O pin allows it to be controlled through the DIO and DIR registers.

OCR0 (Address 07_H) Offset Calibration Coefficient (Least Significant Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR1 (Address 08_H) Offset Calibration Coefficient (Middle Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR2 (Address 09_H) Offset Calibration Coefficient (Most Significant Byte)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR0 (Address $0A_H$) Full-Scale Register (Least Significant Byte)
Reset Value = 59_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR1 (Address $0B_H$) Full-Scale Register (Middle Byte)
Reset Value = 55_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR2 (Address $0C_H$) Full-Scale Register (Most Significant Byte)
Reset Value = 55_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

DOR2 (Address $0D_H$) Data Output Register (Most Significant Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16

DOR1 (Address $0E_H$) Data Output Register (Middle Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08

DOR0 (Address $0F_H$) Data Output Register (Least Significant Byte) (Read Only)
Reset Value = 00_H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

ADS1240 AND ADS1241 CONTROL

COMMAND DEFINITIONS

The commands listed in Table IV control the operations of the ADS1240 and ADS1241. Some of the commands are stand-alone commands (e.g., RESET) while others require additional bytes (e.g., WREG requires count, and the data bytes).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

COMMANDS	DESCRIPTION	OP CODE	2nd COMMAND BYTE
RDATA	Read Data	0000 0001 (01_H)	—
RDATAC	Read Data Continuously	0000 0011 (03_H)	—
STOPC	Stop Read Data Continuously	0000 1111 ($0F_H$)	—
RREG	Read from REG "rrrr"	0001 r r r r ($1x_H$)	xxxx_nnnn (# of regs-1)
WREG	Write to REG "rrrr"	0101 r r r r ($5x_H$)	xxxx_nnnn (# of regs-1)
SELFCAL	Self Cal Offset and Gain	1111 0000 ($F0_H$)	—
SELFOCAL	Self Cal Offset	1111 0001 ($F1_H$)	—
SELFGCAL	Self Cal Gain	1111 0010 ($F2_H$)	—
SYSOCAL	Sys Cal Offset	1111 0011 ($F3_H$)	—
SYSGCAL	Sys Cal Gain	1111 0100 ($F4_H$)	—
DSYNC	Sync $\overline{DRDY}$	1111 1100 (FC_H)	—
SLEEP	Put in SLEEP Mode	1111 1101 (FD_H)	—
RESET	Reset to Power-Up Values	1111 1110 (FE_H)	—
NOTE: (1) The received data in format is always MSB First, the data out format is set by the BIT ORDER bit in ACR reg.			

TABLE IV. Command Summary.

RDATA–Read Data

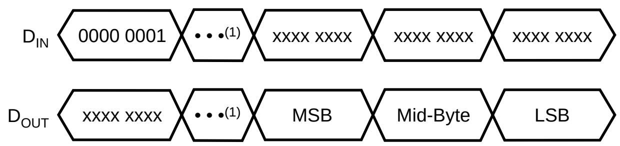
Description: Read a single data value from the Data Output Register (DOR) that is the most recent conversion result. This is a 24-bit value.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



NOTE: (1) For wait time, refer to timing specification.

RDATAC–Read Data Continuous

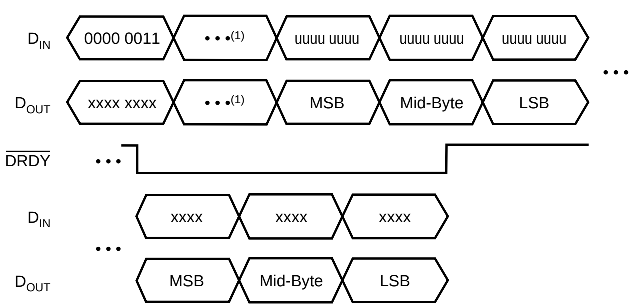
Description: Read Data Continuous mode enables the continuous output of new data on each $\overline{DRDY}$. This command eliminates the need to send the Read Data Command on each $\overline{DRDY}$. This mode may be terminated by either the STOP Read Continuous command or the RESET command.

Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence:
Command terminated when "uuuu uuuu" equals STOPC or RESET.



NOTE: (1) For wait time, refer to timing specification.

STOPC–Stop Continuous

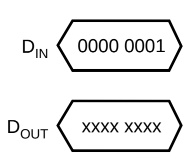
Description: Ends the continuous data output mode.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG–Read from Registers

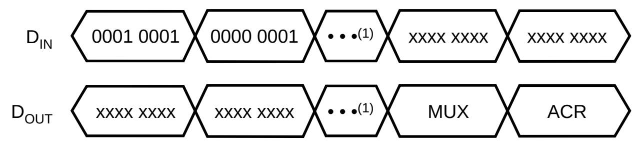
Description: Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte. If the count exceeds the remaining registers, the addresses will wrap back to the beginning.

Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence:
Read Two Registers Starting from Register 01_H (MUX)



NOTE: (1) For wait time, refer to timing specification.

WREG– Write to Register

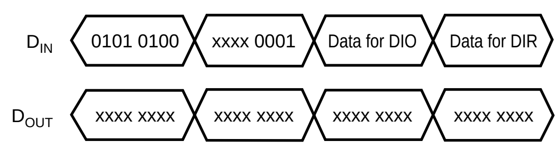
Description: Write to the registers starting with the register specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence:
Write Two Registers Starting from 04_H (DIO)



SELFCAL–Offset and Gain Self Calibration

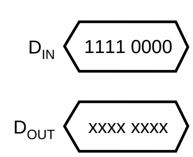
Description: Starts the process of self calibration. The Offset Control Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:



SELFOCAL–Offset Self Calibration

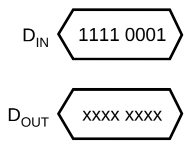
Description: Starts the process of self-calibration for offset. The Offset Control Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0001

Data Transfer Sequence:



SELFGCAL–Gain Self Calibration

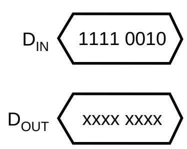
Description: Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0010

Data Transfer Sequence:



SYSOCAL–System Offset Calibration

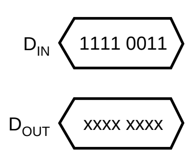
Description: Starts the system offset calibration process. For a system offset calibration, the input should be set to 0V, and the ADS1240 and ADS1241 compute the OCR register value that will compensate for offset errors. The Offset Control Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0011

Data Transfer Sequence:



SYSGCAL–System Gain Calibration

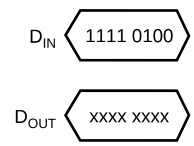
Description: Starts the system gain calibration process. For a system gain calibration, the input should be set to the reference voltage and the ADS1240 and ADS1241 computes the FSR register value that will compensate for gain errors. The FSR is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0100

Data Transfer Sequence:



DSYNC–Sync $\overline{\text{DRDY}}$

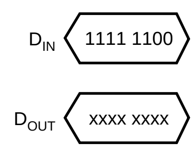
Description: Synchronizes the ADS1240 and ADS1241 to an external event.

Operands: None

Bytes: 1

Encoding: 1111 1100

Data Transfer Sequence:



SLEEP–Sleep Mode

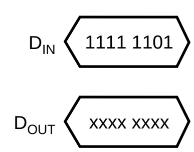
Description: Puts the ADS1240 and ADS1241 into a low power sleep mode. To exit sleep mode strobe SCLK.

Operands: None

Bytes: 1

Encoding: 1111 1101

Data Transfer Sequence:



RESET–Reset to Powerup Values

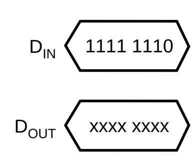
Description: Restore the registers to their power-up values. This command will also stop the Read Continuous mode.

Operands: None

Bytes: 1

Encoding: 1111 1110

Data Transfer Sequence:



	LSB															
MSB	**0000**	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1000**	**1001**	**1010**	**1011**	**1100**	**1101**	**1110**	**1111**
0000	x	rdata	x	rdatac	x	x	x	x	x	x	x	x	x	x	x	stopc
0001	rreg 0	rreg 1	rreg 2	rreg 3	rreg 4	rreg 5	rreg 6	rreg 7	rreg 8	rreg 9	rreg A	rreg B	rreg C	rreg D	rreg E	rreg F
0010	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0011	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0100	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0101	wreg 0	wreg 1	wreg 2	wreg 3	wreg 4	wreg 5	wreg 6	wreg 7	wreg 8	wreg 9	wreg A	wreg B	wreg C	wreg D	wreg E	wreg F
0110	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0111	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1000	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1001	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1010	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1011	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1100	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1101	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
1110	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1111	self cal	self ocal	self gcal	sys ocal	sys gcal	x	x	x	x	x	x	x	dsync	sleep	reset	x

x = Reserved

TABLE V. Command Map.

SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI), allows a controller to communicate synchronously with the ADS1240 and ADS1241. The ADS1240 and ADS1241 operate in slave-only mode.

SPI Transfer Formats

During an SPI transfer, data is simultaneously transmitted and received. The SCLK signal synchronizes shifting and sampling of the information on the two serial data lines: D_{IN} and D_{OUT}. The $\overline{CS}$ signal allows individual selection of the ADS1240 or ADS1241 device; an ADS1240 or ADS1241 with $\overline{CS}$ HIGH is not active on the bus.

Clock Phase and Polarity Controls (POL)

The clock polarity is specified by the POL pin, that selects an active HIGH or active LOW clock, and has no effect on the transfer format.

Serial Clock (SCLK)

SCLK, a Schmitt trigger input to the ADS1240 or ADS1241, is generated by the master device and synchronizes data transfer on the D_{IN} and D_{OUT} lines. When transferring data to or from the ADS1240 or ADS1241, burst mode may be used i.e., multiple bits of data may be transferred back-to-back with no delay in SCLKs or toggling of $\overline{CS}$.

Chip Select ($\overline{CS}$)

The chip select ($\overline{CS}$) input of the ADS1240 or ADS1241 must be externally asserted before a master device can exchange data with the ADS1240 or ADS1241. $\overline{CS}$ must be LOW before data transactions and must stay LOW for the duration of the transaction.

DIGITAL INTERFACE

The ADS1240 and ADS1241's programmable functions are controlled using a set of on-chip registers, as outlined previously. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface.

The ADS1240 and ADS1241's serial interface consists of four signals: $\overline{CS}$, SCLK, D_{IN}, and D_{OUT}. The D_{IN} line is used for transferring data into the on-chip registers while the D_{OUT} line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on D_{IN} or D_{OUT}) take place with respect to this SCLK signal.

The $\overline{DRDY}$ line is used as a status signal to indicate when data is ready to be read from the ADS1240 and ADS1241's data register. $\overline{DRDY}$ goes LOW when a new data word is available in the DOR register. It is reset HIGH when a read operation from the data register is complete. It also goes HIGH prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated.

$\overline{CS}$ is used to select the device. It can be used to decode the ADS1240 and ADS1241 in systems where a number of parts are connected to the serial bus.

The timing specifications show the timing diagram for interfacing to the ADS1240 or ADS1241 with $\overline{CS}$ used to decode the part.

The ADS1240 or ADS1241 serial interface can operate in three-wire mode by tying the $\overline{CS}$ input LOW. In this case, the SCLK, D_{IN}, and D_{OUT} lines are used to communicate with the ADS1240 and ADS1241, the status of $\overline{DRDY}$ can be obtained by interrogating bit 7 of the ACR register (address 2_H). This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port bit.

DEFINITION OF TERMS

An attempt has been made to be consistent with the terminology used in this data sheet. In that regard, the definition of each term is given as follows:

Analog Input Voltage—the voltage at any one analog input relative to AGND.

Analog Input Differential Voltage—given by the following equation: (IN+) – (IN–). Thus, a positive digital output is produced whenever the analog input differential voltage is positive, while a negative digital output is produced whenever the differential is negative.

For example, when the converter is configured with a 2.5V reference and placed in a gain setting of 1, the positive full-scale output is produced when the analog input differential is 2.5V. The negative full-scale output is produced when the differential is –2.5V. In each case, the actual input voltages must remain within the AGND to AV_{DD} range.

Conversion Cycle—the term “conversion cycle” usually refers to a discrete A/D conversion operation, such as that performed by a successive approximation converter. As used here, a conversion cycle refers to the t_{DATA} time period.

Data Rate—The rate at which conversions are completed. See definition for f_{DATA}.

$$f_{DATA} = \frac{f_{OSC}}{128 \bullet 2^{SPEED} \bullet 1280 \bullet 2^{DR}}$$

$$SPEED = 0, 1$$

$$DR = 0, 1, 2$$

Effective Resolution—the effective resolution of the ADS1240 and ADS1241 in a particular configuration can be expressed in two different units: bits rms (referenced to output) and Vrms (referenced to input). Computed directly from the converter’s output data, each is a statistical calculation. The conversion from one to the other is shown below.

“Effective number of bits” (ENOB) or “effective resolution” is commonly used to define the usable resolution of the A/D converter. It is calculated from empirical data taken directly from the device. It is typically determined by applying a fixed known signal source to the analog input and computing the standard deviation of the data sample set. The rms noise defines the $\pm\sigma$ interval about the sample mean (which implies that 95% of the data values fall within this range) and the peak-to-peak noise defines the $\pm 3\sigma$ interval about the sample mean (which implies that 99.6% of the data values fall within this range).

The data from the A/D converter is output as codes, which then can be easily converted to other units, such as ppm or volts. The equations and table below show the relationship between bits or codes, ppm, and volts.

$$ENOB = \frac{-20 \log(ppm)}{6.02}$$

ENOB	VOLTS/BIT	VOLTS/BIT
BITS rms	BIPOLAR Vrms	UNIPOLAR Vrms
	RANGE = 0 $\frac{\left(\frac{2 \bullet V_{REF}}{PGA}\right)}{10^{\left(\frac{6.02 \bullet ER}{20}\right)}}$	RANGE = 0 $\frac{\left(\frac{V_{REF}}{PGA}\right)}{10^{\left(\frac{6.02 \bullet ER}{20}\right)}}$
24	298nV	149nV
22	1.19µV	597nV
20	4.77µV	2.39µV
18	19.1µV	9.55µV
16	76.4µV	38.2µV
14	505µV	152.7µV

f_{OSC}—the frequency of the crystal oscillator or CMOS compatible input signal at the X_{IN} input of the ADS1240 and ADS1241.

f_{MOD}—the frequency or speed at which the modulator of the ADS1240 and ADS1241 is running. This depends on the SPEED bit as given by the following equation:

	SPEED = 0	SPEED = 1
mfactor	128	256

$$f_{MOD} = \frac{f_{OSC}}{mfactor} = \frac{f_{OSC}}{128 \bullet 2^{SPEED}}$$

f_{SAMP}—the frequency, or switching speed, of the input sampling capacitor. The value is given by one of the following equations:

PGA SETTING	SAMPLING FREQUENCY
1, 2, 4, 8	$f_{SAMP} = \frac{f_{OSC}}{mfactor}$
16	$f_{SAMP} = \frac{f_{OSC} \bullet 2}{mfactor}$
32	$f_{SAMP} = \frac{f_{OSC} \bullet 4}{mfactor}$
64, 128	$f_{SAMP} = \frac{f_{OSC} \bullet 8}{mfactor}$

f_{DATA}—the frequency of the digital output data produced by the ADS1240 and ADS1241, f_{DATA} is also referred to as the Data Rate.

Full-Scale Range (FSR)—as with most A/D converters, the full-scale range of the ADS1240 and ADS1241 is defined as the "input", that produces the positive full-scale digital output minus the "input", that produces the negative full-scale digital output.

For example, when the converter is configured with a 2.5V reference and is placed in a gain setting of 2, the full-scale range is: [1.25V (positive full-scale) minus –1.25V (negative full-scale)] = 2.5V.

Least Significant Bit (LSB) Weight—this is the theoretical amount of voltage that the differential voltage at the analog input would have to change in order to observe a change in the output data of one least significant bit. It is computed as follows:

$$\text{LSB Weight} = \frac{\text{Full–Scale Range}}{2^N}$$

where N is the number of bits in the digital output.

t_{DATA}—the inverse of f_{DATA}, or the period between each data output.

	5V SUPPLY ANALOG INPUT(1)			GENERAL EQUATIONS		
GAIN SETTING	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES(2)	PGA OFFSET RANGE	FULL-SCALE RANGE	DIFFERENTIAL INPUT VOLTAGES(2)	PGA SHIFT RANGE
1	5V	±2.5V	±1.25V	$\frac{2 \bullet V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{2 \bullet PGA}$
2	2.5V	±1.25V	±0.625V			
4	1.25V	±0.625V	±312.5mV		RANGE = 0	
8	0.625V	±312.5mV	±156.25mV			
16	312.5mV	±156.25mV	±78.125mV	$\frac{V_{REF}}{PGA}$	$\frac{\pm V_{REF}}{2 \bullet PGA}$	$\frac{\pm V_{REF}}{4 \bullet PGA}$
32	156.25mV	±78.125mV	±39.0625mV			
64	78.125mV	±39.0625mV	±19.531mV		RANGE = 1	
128	39.0625mV	±19.531mV	±9.766mV			

NOTES: (1) With a 2.5V reference. (2) Refer to electrical specification for analog input voltage range.

TABLE VI. Full-Scale Range versus PGA Setting.

TOPIC INDEX

TOPIC PAGE

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