# Audio signal processing IC for notebook PC

## Overview

AN12942B is an one-chip IC for the stereo speakers which can output 1 W by 8  $\Omega$ , headphone amplifiers, line amplifiers, and electronic volumes.

The AGC circuit is built-in to prevent the resonance or the vibration by the speaker's energy and the clipping distortion what is called "broken up sound".

Also the AN12942B is built-in power saving on/off function automatically detecting input signal to save the power of speaker amplifier.

#### Features

• Speaker amplifier

1 W × 2-channel: 8  $\Omega$ , V<sub>CC</sub> = 5 V

- Built-in AGC circuit Prevention of the resonance or the vibration due to the speaker and the clipping distortion by AGC at excessive input signal (with AGC on/off switch).
- Built-in automatic power saving function.
  - It detects input signals and switches on/off (with the on/off switch for the auto power saving).
- Built-in headphone amplifier and line amplifier

### Applications

• Notebook PC

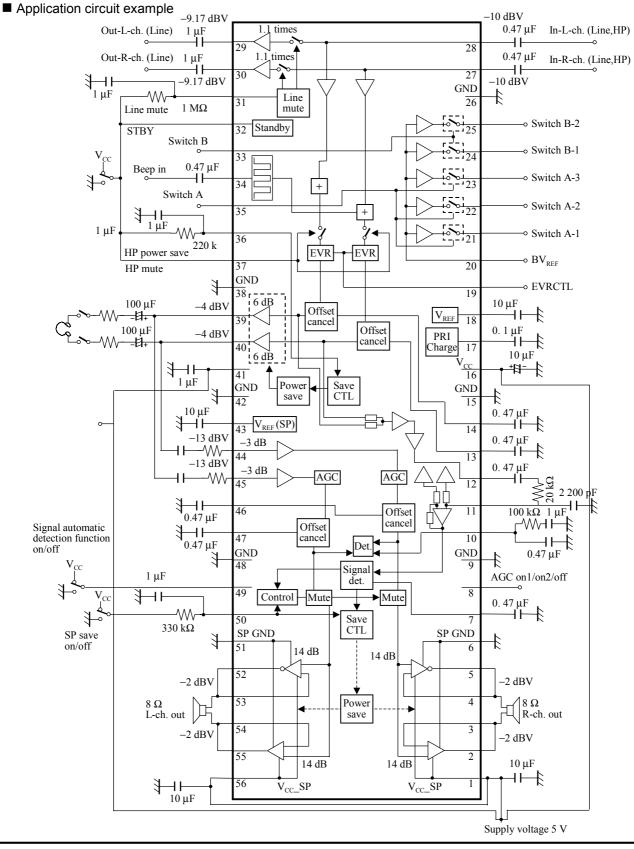
### Package

• Dual surface implementing package (HSOP056-P-0300A)

## ■ Туре

• Silicon monolithic bipolar IC

# Panasonic



SDC00047AEB

# Panasonic

## Pin Descriptions

Pin No.	Pin name	Туре	Description
1	V <sub>CC</sub> _SP	V <sub>CC</sub>	V <sub>CC</sub> _SP R-channel
2	SP_OUT_R+	Output	Speaker amplifier R-channel positive phase output (+)
3	SP_OUT_R+	Output	Speaker amplifier R-channel positive phase output (+)
4	SP_OUT_R-	Output	Speaker amplifier R-channel negative phase output (-)
5	SP_OUT_R-	Output	Speaker amplifier R-channel negative phase output (-)
6	GND_SP	GND	GND_SP R-channel
7	DETECT_CAP	Input	Demodulation pin for signal automatic detection
8	AGC_LV	TTL input	AGC-on level control
9	GND	GND	GND
10	AGC_CAP	Input	AGC demodulation pin
11	DETECT_IN	Input	Signal input for signal automatic detection
12	DAMP_OUT	Output	Signal automatic detection mix amplifier output
13	OFFSET_HPR	Input	Offset cancel pin for headphone R-channel
14	OFFSET_HPL	Input	Offset cancel pin for headphone L-channel
15	GND	GND	GND
16	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
17	PRI_V	Input	PRI-charge level pin
18	V <sub>REF</sub> _IN	Input	V <sub>REF</sub>
19	EVR_CTL	TTL input	EVR control for speaker and headphone
20	BV <sub>REF</sub>	Input	Bias in
21	Switch A-1	Output	Switch A-1
22	Switch A-2	Output	Switch A-2
23	Switch A-3	Output	Switch A-3
24	Switch B-1	Output	Switch B-1
25	Switch B-2	Output	Switch B-2
26	GND	GND	GND
27	INPUT_R	Input	R-channel input
28	INPUT_L	Input	L-channel input
29	LINEOUT_L	Output	Line L-channel output
30	LINEOUT_R	Output	Line R-channel output
31	LINE_MUTE	TTL input	Line mute on/off control
32	STANDBY	TTL input	Standby on/off control
33	Switch B	TTL input	Switch B
34	BEEP_IN	Input	Input for beep signal

# Panasonic

# Pin Descriptions (continued)

Pin No.	Pin name	Туре	Description
35	Switch A	TTL input	Switch A
36	HP_SAVE	TTL input	Headphone power save control
37	HP_MUTE	TTL input	Headphone mute on/off control
38	GND	GND	GND
39	HP_OUT_L	Output	Headphone amplifier L-channel output
40	HP_OUT_R	Output	Headphone amplifier R-channel output
41	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
42	GND	GND	GND
43	V <sub>REF</sub> _SP	Input	V <sub>REF</sub> SP
44	SP_IN_R	Input	Speaker amplifier R-channel input
45	SP_IN_L	Input	Speaker amplifier L-channel input
46	OFFSET_SPR	Input	Offset cancel pin for speaker R-channel
47	OFFSET_SPL	Input	Offset cancel pin for speaker L-channel
48	GND	GND	GND
49	DETECT_ON	TTL input	Signal automatic detection on/off control
50	SP_SAVE	TTL input	Speaker power save control
51	GND_SP	GND	GND_SP L-channel
52	SP_OUT_L-	Output	Speaker amplifier L-channel negative phase output (-)
53	SP_OUT_L-	Output	Speaker amplifier L-channel negative phase output (-)
54	SP_OUT_L+	Output	Speaker amplifier L-channel positive phase output (+)
55	SP_OUT_L+	Output	Speaker amplifier L-channel positive phase output (+)
56	V <sub>CC</sub> _SP	V <sub>CC</sub>	V <sub>CC</sub> _SP L-channel

## Absolute Maximum Ratings

A No.	Parameter	Symbol Rating		Unit	Note
1	Sumply voltage	V <sub>CC</sub>	5.75	V	*1
1	Supply voltage	V <sub>CC</sub> _SP	5.75	v	.1
2	Supply current	I <sub>CC</sub>		А	_
3	Power dissipation	P <sub>D</sub>	517	mW	*2
4	Storage temperature	T <sub>stg</sub>	-55 ~ +150	°C	*3
5	Operating ambient temperature	T <sub>opr</sub>	-20 ~ +75	°C	*3

Note) \*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

\*2: When using this IC, referring to the technical data in page 17, observe the power dissipation characteristic curve.

Be sure to use the IC so that the power dissipation of the IC without heat sink will not exceed 517 mW at  $T_a = 75^{\circ}C$ .

\*3: Except for the operating ambient temperature and storage temperature, all ratings are for  $T_a = 25^{\circ}C$ .

## Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Note
	V <sub>CC</sub>	4.50 ~ 5.50	V	—
Operating supply voltage range	V <sub>CC</sub> _SP	4.50 ~ 5.50	v	*

Note) \*: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

# Panasonic

# Electrical Characteristics at $V_{CC} = 5.0 \text{ V}$ , $V_{CC}$ SP = 5.0 V Note) $T_a = 25^{\circ}C \pm 2^{\circ}C$ unless otherwise specified.

В	Demonster	Ourseland	Test	O and life and		Limits		Llnit	
No.	Parameter	Symbol	circuits	Conditions	Min	Тур	Max	Unit	Note
Circu	it current	1	1						
1	Circuit current 1A at non-signal (V <sub>CC</sub> SP)	IT1A	1	$V_{\rm CC} = 5.00$ V, at non-signal,		35	70	μΑ	_
2	Circuit current 2A at non-signal $(V_{CC})$	IT2A	1	at automatic distinction: on	_	20.0	27.0	mA	_
3	Circuit current 1B at non-signal (V <sub>CC</sub> SP)	IT1B	1	$V_{CC} = 5.00 \text{ V}$ , at non-signal, SP and HP power save: off,		9.3	18.6	mA	_
4	Circuit current 2B at non-signal $(V_{CC})$	IT2B	1	at automatic distinction		21.0	28.0	mA	_
5	Circuit current 1C at non-signal (V <sub>CC</sub> _SP)	IT1C	1	$V_{CC} = 5.00$ V, at non-signal, at automatic distinction: off,		35	70	μΑ	
6	Circuit current 2C at non-signal $(V_{CC})$	IT2C	1	SP and HP power save: on		14.0	19.0	mA	
7	Standby current 1 at non-signal (V <sub>CC</sub> _SP)	IST1	1	V <sub>CC</sub> = 5.00 V,		10	50	μΑ	
8	Standby current 2 at non-signal $(V_{CC})$	IST2	1	at standby mode		0.1	50	μΑ	_
Speaker amplifier ( $R_L = 8 \Omega$ ): Speaker_input (pin 44, pin 45) $\rightarrow$ Speaker_output (pin 2 to pin 5, pin 52 to pin 55)									
9	Output level L-channel	VSPL	1	$V_{IN} = -13.0 \text{ dBV}, f = 1 \text{ kHz},$	2.0	4.0	6.0	dBV	_
10	Output level R-channel	VSPR	1	$R_{L} = 8 \Omega$	2.0	4.0	6.0	dBV	_
11	Output distortion L-channel	TH <sub>s</sub> L	1	$V_{IN} = -13.0 \text{ dBV}, f = 1 \text{ kHz},$		0.04	0.5	%	—
12	Output distortion R-channel	TH <sub>s</sub> R	1	$R_L = 8 \Omega$ , to THD fifth		0.04	0.5	%	_
13	Maximum output electric power L-channel	VMAXSL	1	V <sub>IN</sub> = 1 kHz, THD = 1%,	0.7	0.88		W	
14	Maximum output electric power R-channel	VMAXSR	1	$R_L = 8 \Omega,$	0.7	0.88	_	W	_
15	Output noise L-channel	VNSL	1	$Rg = 1 k\Omega, R_L = 8 \Omega,$	_	-76	-67	dBV	_
16	Output noise R-channel	VNSR	1	A curve filter		-76	-67	dBV	—
17	Channel balance	CHBS	1	$V_{IN} = -13.0 \text{ dBV}, f = 1 \text{ kHz},$ $R_L = 8 \Omega$	-1	0	1	dB	_
18	Cross talk in L-channel	CTLSLR	1	$V_{IN} = -13.0 \text{ dBV}, f = 1 \text{ kHz},$	70	76		dB	—
19	Cross talk in R-channel	CTLSRL	1	$R_L = 8 \Omega$ , A curve filter	70	76		dB	_
Head	phone amplifier ( $R_L = 32 \Omega$ ): L-chan	nel, R-channe	l_input (p	bin 28, pin 27) $\rightarrow$ Headphone_or	utput (p	in 39, p	in 40)		
20	Output level L-channel	VHPL	1	$V_{IN} = -10.0 \text{ dBV}, R_L = 32 \Omega$	-5.0	-4.0	-3.0	dBV	_
21	Output level R-channel	VHPR	1	Vol = 3.3 V (max), f = 1 kHz	-5.0	-4.0	-3.0	dBV	-
22	Channel balance	СНВН	1	$V_{IN} = -10.0 \text{ dBV}, R_L = 32 \Omega$ Vol = 3.3 V (max), f = 1 kHz R-ch./L-ch. difference	-1.0	0.0	1.0	dB	_

# Electrical Characteristics at $V_{CC} = 5.0 \text{ V}$ , $V_{CC}SP = 5.0 \text{ V}$ (continued) Note) $T_a = 25^{\circ}C \pm 2^{\circ}C$ unless otherwise specified.

В		0	Test			Limits		11.11	
No.	Parameter	Symbol	circuits	Conditions	Min	Тур	Max	Unit	Note
Head	phone Amplifier ( $R_L = 32 \Omega$ ) (continu	ied): L-chann	el, R-chai	nnel_input (pin 28, pin 27) $\rightarrow$ H	eadpho	ne_outp	ut (pin	39, pin 4	10)
23	Output distortion L-channel	THHL	1	$V_{OUT} = -14 \text{ dBV}, R_L = 32 \Omega$		0.03	0.1	%	_
24	Output distortion R-channel	THHR	1	Vol = 3.3 V (max), f = 1 kHz		0.03	0.1	%	_
25	Maximum input level L-channel	VMAHIL	1	THD = 1%, $R_L = 10 \text{ k}\Omega$	0.0	6.0		dBV	_
26	Maximum input level R-channel	VMAHIR	1	Vol = 1.65 V (typ), f = 1 kHz	0.0	6.0		dBV	_
27	Maximum output level L-channel	VMAHOL	1	THD = 1%, $R_L = 10 \text{ k}\Omega$	0.0	2.8	_	dBV	_
28	Maximum output level R-channel	VMAHOR	1	Vol = 3.3 V (max), f = 1 kHz	0.0	2.8		dBV	_
29	Output noise L-channel	VNHL	1	Da = 1 lco A sum filter		-94	-79	dBV	_
30	Output noise R-channel	VNHR	1	$Rg = 1 k\Omega$ , A curve filter		-94	-79	dBV	_
31	Cross talk in L-channel	CTLHLR	1	$V_{IN} = -10 \text{ dBV}, R_L = 32 \Omega$	60	70		dB	_
32	Cross talk in R-channel	CTLHRL	1	f = 10  kHz, A curve filter	60	70		dB	_
33	Mute attenuation quantity L-channel	VMUHL	1	$V_{IN} = -10 \text{ dBV}, R_L = 32 \Omega$	70	90		dB	_
34	Mute attenuation quantity R-channel	VMUHR	1	f = 1 kHz, A curve filter	70	90		dB	_
35	Beep output level L-channel	BEHL	1	$V_{IN} = 3.3 V_{PP}, R_L = 32 \Omega$	0.28	0.58		V <sub>PP</sub>	_
36	Beep output level R-channel	BEHR	1	1  cycle = 1  ms	0.28	0.58		V <sub>PP</sub>	_
Volume part: L-channel, R-channel_input (pin 28, pin 27) → Headphone_output (pin 39, pin 40)									
37	Medium voltage gain L-channel	VOLL	1	$V_{IN} = -20 \text{ dBV}, f = 1 \text{ kHz},$	-32.5	-30.0	-27.5	dBV	—
38	Medium voltage gain R-channel	VOLR	1	Vol = 1.65 V (typ)	-32.5	-30.0	-27.5	dBV	_
39	Channel balance at the time of the medium gain	V <sub>CHB</sub>	1	$V_{IN} = -20 \text{ dBV}, f = 1 \text{ kHz},$ Vol = 1.65 V (typ) R-ch./L-ch. Difference	-2.0	0.0	2.0	dB	_
40	Volume maximum attenuation quantity L-channel	VOLNL	1	$V_{IN} = -10 \text{ dBV}, f = 1 \text{ kHz},$ Vol = 0.0 V (min),	70	90		dB	
41	Volume maximum attenuation quantity R-channel	VOLNR	1	A curve filter	70	90	_	dB	_
Line	amplifier part : L-channel, R-channel_	input (pin 28,	, pin 27) -	→ Headphone_output (pin 29, p	in 30)				
42	Output level L-channel	VHLL	1	$V_{IN} = -10.0 \text{ dBV},$	-10.0	-9.2	-8.4	dBV	—
43	Output level R-channel	VHLR	1	$R_L = 10 \text{ k}\Omega, \text{ f} = 1 \text{ kHz}$	-10.0	-9.2	-8.4	dBV	—
44	Channel balance	CHBL	1	$V_{IN} = -10.0 \text{ dBV},$ $R_L = 10 \text{ k}\Omega, \text{ f} = 1 \text{ kHz},$ R-ch./L-ch. difference	-0.8	0.0	0.8	dB	
45	Output distortion L-channel	THLL	1	$V_{IN} = -10.0 \text{ dBV},$		0.003	0.03	%	_
46	Output distortion R-channel	THLR	1	$R_L = 10 \text{ k}\Omega, \text{ f} = 1 \text{ kHz},$	_	0.003	0.03	%	_
47	Maximum output level L-channel	VMALL5	1	THD = 1%, $R_L = 10 \text{ k}\Omega$	0.0	4.0		dBV	_
48	Maximum output level R-channel	VMALR5	1	f = 1 kHz	0.0	4.0		dBV	_

# Electrical Characteristics at $V_{CC} = 5.0 \text{ V}$ , $V_{CC}SP = 5.0 \text{ V}$ (continued) Note) $T_a = 25^{\circ}C \pm 2^{\circ}C$ unless otherwise specified.

49	Parameter amplifier part (continued) : L-channel Output noise L-channel	Symbol	circuits	Conditions			Limits					
49	, ,				Min	Тур	Max	Unit	Note			
	Output noise L-channel	Line amplifier part (continued) : L-channel, R-channel_input (pin 28, pin 27) → Headphone_output (pin 29, pin 30)										
50		VNLL	1	$Rg = 1 k\Omega$ , A curve filter		-105	-87	dBV	—			
	Output noise R-channel	VNLR	1	Rg = 1 Rs2, A curve inter		-105	-87	dBV	—			
51	Cross talk in L-channel	CTLLLR	1	$V_{\rm IN} = -10 \text{ dBV}, R_{\rm L} = 10 \text{ k}\Omega$	60	84		dB	—			
52	Cross talk in R-channel	CTLLRL	1	f = 10  kHz, A curve filter	60	84		dB	—			
53	Mute attenuation quantity L-channel	VMUHL	1	$V_{\rm IN} = -10 \text{ dBV}, R_{\rm L} = 10 \text{ k}\Omega$	70	87		dB				
54	Mute attenuation quantity R-channel	VMUHR	1	f = 1 kHz, A curve filter	70	87	—	dB	—			
Speak	ker AGC part : Speaker_input (pin 44	, pin 45) $\rightarrow$ S	peaker_o	utput (pin 2 to pin 5, pin 52 to p	in 55)							
	Speaker amplifier output level L-channel AGC-on1	VAGSPL	1		4.5	6.0	7.5	dBV				
	Speaker amplifier output level R-channel AGC-on1	VAGSPR	1	$V_{IN} = -3.0 \text{ dBV}, f = 1 \text{ kHz},$	4.5	6.0	7.5	dBV				
	Speaker amplifier output level L-channel AGC-on2	VAGSP1L	1	$R_L = 8 \Omega$	5.5	7.0	8.5	dBV	_			
	Speaker amplifier output level R-channel AGC-on2	VAGSP1R	1		5.5	7.0	8.5	dBV				
Auton	natic signal detection part : L-channe	el, R-channel	_input (pi	n 28, pin 27) $\rightarrow$ Signal detection	n pream	plifier o	output (	pin 12)				
	Preamplifier output voltage level L-channel entry	VSDTL	1	$V_{IN} = -33 \text{ dBV}, f = 1 \text{ kHz}$	-13	-10	-7	dBV				
	Preamplifier output voltage level R-channel entry	VSDTR	1	Vol = 1.65 V (typ)	-13	-10	-7	dBV				
61	Signal detection limit entry voltage level L-channel	VSDTTHL	1	$V_{IN} = 1 \text{ kHz}$	-63	-58	-53	dBV				
62	Signal detection limit entry voltage level R-channel	VSDTTHR	1	Vol = 1.65 V (typ)	-63	-58	-53	dBV	_			
Switch	h switching-over voltage level											
63	Headphone mute on	HMUON	1		GND		0.8	V				
64	Headphone mute off	HMUOF	1		2.0		5.5	V				
65	Headphone power save on	HPSON	1		GND		0.8	V				
66	Headphone power save off	HPSOF	1		2.0		5.5	V	_			
67	Speaker power save on	SPSON	1		GND		0.8	V				
68	Speaker power save off	SPSOF	1		2.0		5.5	V	_			
69	Standby on	STON	1		GND		0.8	V	_			
	Standby off	STOF	1		2.0		5.5	V	_			
	Line mute on	LMUON	1		GND		0.8	V				
	Line mute off	LMUOF	1		2.0		5.5	V				

# Panasonic

# Electrical Characteristics at $V_{CC} = 5.0 \text{ V}$ , $V_{CC}SP = 5.0 \text{ V}$ (continued) Note) $T_a = 25^{\circ}C \pm 2^{\circ}C$ unless otherwise specified.

В	Deremeter	Querrahal	Test	Canditiana		Limits		1.1.0.14	Note
No.	Parameter	Symbol	circuits	Conditions	Min	Тур	Max	Unit	Note
Switc	Switch switching-over voltage level (continued)								
73	Signal automatic detection feature off	ATOF	1		GND		0.8	V	_
74	Signal automatic detection feature on	ATON	1		2.0		5.5	V	
75	Speaker-AGC off	AGOF	1		GND		0.5	V	_
76	Speaker-AGC on2	AGON1	1			Open		V	_
77	Speaker-AGC on1	AGON	1		2.5		5.5	V	—
78	Switch A Off	CMUOF	1		GND		0.8	V	—
79	Switch A On	CMUON	1		2.0	_	5.5	V	_
80	Switch B Off	DMUOF	1		GND		0.8	V	_
81	Switch B On	DMUON	1		2.0		5.5	V	_

# Control Terminal, The Mode Table

Note) The holding range of control voltage is shown in B No. 63 to B No. 81 of Electrical Characteristics.

	Description	Volt	age		Demerke	
Pin No.	Description	Low	High		Remarks	
37	Headphone mute on/off	Mute on	Mute off			
36	Headphone power save on/off	Save on (HP off)	Save off (HP on)	_		
49	The signal automatic detection feature on/off	Automatic distinction: off	Automatic distinction: on	_		
32	Standby on/off	STB on	STB off			
50	Speaker power save on/off	Save on (SP off)	Save off (SP on)	It has priority over power saving by pin 50 more than an automatic detection.		
35	Switch A	Off	On		_	
33	Switch B	Off	On		_	
31	Line mute on/off	Mute on	Mute off		_	
	Description		Voltage			
Pin No.	Description	Low	Open	High		
8	At the time of time of AGC: on, it changes on level.	AGC: off	AGC: on2	AGC: on1		

# Panasonic

# • Control Terminal, The Leakage Current Table at $V_{CC} = 5.0 \text{ V}, V_{CC}\text{SP} = 5.0 \text{ V}$

Design reference value

Dia Ma	Description	Leakage	e current	Inputimpodopoo	
Pin No.	Description	I <sub>iL-max</sub>	I <sub>iH-max</sub>	Input impedance	
33	Switch B	+2μΑ	+80µA	The low holding range: High impedance The high holding range: About 80 $k\Omega$	
35	Switch A	+2μΑ	+80µA	The low holding range: High impedance The high holding range: About 80 $k\Omega$	
37	Headphone mute on/off	-20µA	+30µA	About 170 kΩ	
8	At the time of AGC = on, it changes on level.	-20µA	+50µA	About 125 kΩ	

				an the voltage of tation circuit	In the case beyond the voltage of the input voltage limitation circuit			
Pin No.	Description	Leakage current		Input impodance	Leakage	e current	Inputimpodopoo	
		l <sub>iL-max</sub>	I <sub>iH-max</sub>	Input impedance	l <sub>iL-max</sub>	l <sub>iH-max</sub>	Input impedance	
31	Line mute on/off	+1µA	+1µA	High impedance	_	+100µA	25 kΩ typ.	
32	Standby on/off	+1µA	+1µA	High impedance	_	+50µA	45 kΩ typ.	
36	Headphone power save on/off	-1µA	+1µA	High impedance	+40µA	+200µA	16 k $\Omega$ typ.	
49	Signal automatic detection feature on/off	+1µA	+1µA	High impedance	_	+20µA	85 k $\Omega$ typ.	
50	Speaker power save on/off	-1µA	+1µA	High impedance	+5µA	+200µA	15 kΩ typ.	

- The sourcing current of the pin is indicated with "+".
- The range that a control voltage is held in low level : Pin 33, pin 35, pin 37, pin 31, pin 32, pin 36, pin 49, pin 50 : 0 V ~ 0.8 V Pin 8 : 0 V ~ 0.5 V
- The range that a control voltage is held in high level : Pin 33, pin 35, pin 37, pin 31, pin 32, pin 36, pin 49, pin 50 : 2.0 V ~ 5.5 V Pin 8 : 2.5 V ~ 5.5 V
- Pin 31, pin 32, pin 36, pin 49 and pin 50 builds in an input voltage limitation circuit.
- In the case beyond the voltage of the input voltage limitation circuit, leakage current depends on inside resistance.
- When resistance is connected to a pin, current decreases by the sum total of resistance and internal resistance.

Note) The characteristics listed above are reference values based on the IC design and are not guaranteed.

# Technical Data

 $\bullet\,$  Circuit diagrams of the input/output part and pin function descriptions

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
1, 56	V <sub>CC</sub> _SP DC: 5.0 V			<ul> <li>Power supply pins specifically designed for speaker amplifiers.</li> <li>Pin 1 for R-channel.</li> <li>Pin 56 for L-channel.</li> <li>Because the big electric current flows, it is desirable to separate from the V<sub>CC</sub> line to the other power supply pins on the board pattern.</li> </ul>
52, 53, 54, 55, 2, 3, 4, 5	Speaker output Pin 52, pin 53 Pin 2, pin 3 Positive phase Pin 54, pin 55 Pin 4, pin 5 Negative phase OC: 2.20 V AC: 4 dBV	V <sub>CC</sub> _SP (5.0 V)	The output impedance: Equal to or less than 1 Ω	<ul> <li>Output pins of speaker amplifiers.</li> <li>It becomes BTL output.</li> <li>Pin 54, pin 55 for L-channel positive phase output</li> <li>Pin 52, pin 53 for L-channel negative phase output</li> <li>Pin 2, pin 3 for R-channel positive phase output</li> <li>Pin 4, pin 5 for R-channel negative phase output</li> <li>To reduce voltage loss caused by the wire resistance in maximum output, it makes output 2 terminals.</li> <li>When the speaker amplifiers save power, DC voltage is also kept.</li> </ul>
51, 6	GND_SP DC : 0.0 V			<ul> <li>It is GND pin for the speaker amplifier.</li> <li>Pin 6 is for R-channel.</li> <li>Pin 51 is for L-channel.</li> <li>Because the big electric current flows, it is desirable to separate from the GND line to the other GND pin on the board pattern. Also, it isn't connected with the substrate potential in the IC.</li> </ul>
31	Line mute control	31 25 k	The base entry (With the resistance) In the range which entry limiter does not depend on, it is high impedance.	It controls on/off of the mute function of the line output.

# **Panasonic**

#### Technical Data (continued)

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
7	Audio automatic detection detection pin: Signal nothing DC: 0.0 V Signal's there being DC: 2.0 V	VREG (4.5 V)           100           40k	Signal less time: Constant current source Signal's there being: The output impedance: About 200 Ω	It connects a condenser for the peak detection. It is the circuit which detects a peak after rectifying the audio signal of the audio signal automatic detection circuit in both waves. By changing a capacity value, the time which the power saving depends on in case of the switchover which is without signal with signal's there being can be changed.
9, 15, 26, 38, 42, 48	GND DC: 0.0 V			It is the GND pins of the signal system. It is connected with the substrate potential of the IC. Pin 15, pin 42 connect with the lead frame of the IC.
43	V <sub>REF</sub> (SP) DC: 2.20 V	$\begin{array}{c} & & & & \\ & & & & \\ & & & & \\ & & &$	The entry impedance: About 200 kΩ	It is the standard voltage pin to fix the DC bias of the speaker output. It connects a condenser to remove a ripple.
29, 30	Line out AC: –9.17 dBV DC : 2.25 V	$V_{REG} (4.5 V)$ $Pin 29,$ $Pin 30$ $17.4k$ $777$	The output impedance: Equal to or less than about 10 Ω	It is the output pin of the line amplifier.

### Technical Data (continued)

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
49	Signal automatic detection function on/off control pin DC: —	$ \begin{array}{c}                                     $	The entry impedance: The high impedance	We change an audio signal automatic detection function in on/off. In case of automatic detection off, it controls power saving by speaker with the manual with the power saving on/off pin. • High: Function on • Low: Function off
44, 45	Speaker amplifier entry DC: 2.25 V AC: -10 dBV	Pin 45, pin 44 $V_{REF}$ 777 (2.25 V) $777$ $777$	The entry impedance: About 18 kΩ	It is the voice input pins of the speaker amplifier. To make offset voltage in power saving on/off changing by the speaker amplifier little, it combines capacity. ( It makes POP noise small ). Pin 44: R-channel speaker entry Pin 45: L-channel speaker entry
20	BV <sub>REF</sub> DC: — V	V <sub>REG</sub> (4.5 V)	The entry impedance: The high impedance	It is the input pin of BV <sub>REF</sub> .
21, 22, 23, 24, 25	Switch A-1 Switch A-2 Switch A-3 Switch B-1 Switch B-2 DC: V	V <sub>REG</sub> (4.5 V) Pin 21, pin 22, pin 23, pin 24, pin 24, pin 25 (20)	The output impedance: Equal to or less than about 10 Ω	It is the output pin of BV <sub>REF</sub> .
33 35	Switch B Switch A DC: 0 V (at Open)	80k Pin 33, pin 35 250k	The entry impedance: About 80 kΩ	We change a noise removal function in on/off. • High: Function on • Low: Function off

### ■ Technical Data (continued)

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
17	Pri_charge level pin DC: 3 V	$\frac{V_{CC}(5.0 \text{ V})}{160 \text{ k}}$	The entry impedance: About 100 kΩ	It is the voltage pin for DC bias pri_charge.
27, 28	Audio signal input DC: 2.25 V AC: -10 dBV	Pin 28, $V_{REG}$ (4.5 V) pin 27 22.5k 13.2k 22.5k 31.8k $V_{REF}$ (2.25 V)	The entry impedance: About 22.5 kΩ	It enters a main audio signal. • Pin 27: R-channel entry • Pin 28: L-channel entry
16, 41	V <sub>CC</sub> DC: 5.0 V			It is the power supply $(V_{CC})$ pin to supply the regulator circuit to create the inner power supply $V_{REG}$ with the voltage. It is separating from $V_{CC}$ _SP of pin 1, pin 56 fully inside. It is desirable to separate as far as it finishes coming out about the P board pattern, too.
32	Standby on/off changing SW Open DC voltage DC: 0.00 V	32 80k 240k 777	The entry impedance: About 80 kΩ	It changes whether or not it makes this IC an operation condition or whether or not it makes it a standby. • Low: Standby • High: The operation condition In that the power changes a connected condition to the standby, the circuit electric current can be almost made 0.

## Technical Data (continued)

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
34	Beep entry DC: 2.25 V AC: 3.3 V <sub>PP</sub>	34 180 (34) (35) (34)	The entry impedance: About 180 kΩ	It is the entry pin to enter beep signal. The same signal is entered both by L-channel and R-channel with the audio signal mix amplifier of the following paragraph.
18	V <sub>REF</sub> DC: 2.25 V	$\begin{array}{c} & & \\ & & \\ \hline \\$	The entry impedance: About 200 kΩ	With the pin to fix the bias voltage (the operation point) of the system which the inner power supply ( $V_{REG}$ ) works, it becomes 1/2 $V_{REG}$ (V). To remove noise, it connects a condenser with the interval of GND.
12	The signal detection system preamplifier output pin DC: 2.25 V AC: -10 dBV	V <sub>REG</sub> (4.5 V)	The output impedance: About 10 Ω	It is the output pin of the signal detection system preamplifier.
11	Signal input for signal automatic detection DC: 2.25 V AC: -10 dBV	(1) 777 20k V <sub>REF</sub> (2.25 V) 777 777	The entry impedance: About 20 kΩ	It is the signal input pin for signal automatic detection. It is possible to adjust in the direction lowers a gain by adding external resistance.

### Technical Data (continued)

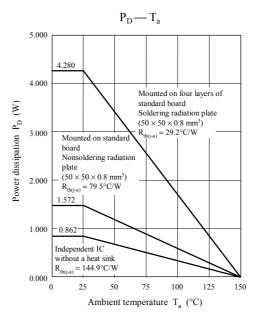
Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
19	EVR control for SP and HP DC: — V	19 	The entry impedance: The high impedance	It is the pin which controls EVR for speaker amplifier and Headphone amplifier. The holding range with control voltage is 0 V to 3.3 V.
10	AGC detection pin DC: 0 V ~ 1 V	UREG (4.5 V) 90 10 	The entry impedance: Unsettled	It is the detection circuit to detect the signal level of the AGC circuit of the speaker output for the clip prevention. It connects a condenser for the detection.
8	AGC on1/on2/off control pin DC: —	$V_{REG} (4.5 V)$ $216k + 40k + 8$ $40k + 40k + 777$ $777 + 777$	The entry impedance: About 76 kΩ	It is the pin which controls the operation of the AGC circuit of the speaker output for the clip prevention in on/off. At the time of off, the AGC circuit does not work. • "High" : AGC-on1 • "Open" : AGC-on2 • "Low" : AGC-off
13, 14, 46, 47	Offset cancellation C pin DC : 2.25 V	V <sub>REG</sub> (4 V) Pin 13, pin 14, pin 46, pin 47 	The entry impedance: About 80 kΩ	It is the condenser connection pin of the offset cancellation circuit to remove the DC offset. As the principle, it composes high pass filter by entry impedance "R" and connection condenser "C".

# **Panasonic**

#### Technical Data (continued)

Pin No.	Waveform and voltage	Inner circuit	Impedance	Description
50	SP amplifier power saving on/off control pin DC: —	$V_{CC} (5 V)$ $V_{REG} (4.5 V)$ $180k$ $80k$ $50$ $48k$ $777$	The entry impedance: The high impedance	It is the pin which controls power saving by the speaker amplifier. At the time of on in addition to the control in case of automatic distinction function off, too, power saving on by pin 50 have priority over.
36	HP amplifier power saving on/off control pin DC: —	$V_{CC} (5 V)$ $V_{REG} (4.5 V)$ $16k$ $70k$ $770k$ $777$	The entry impedance: The high impedance	It is the pin which controls power saving by the headphone amplifier.
37	HP amplifier mute on/off control terminal DC : 2.0 V	$V_{REG}$ (4.5 V) 220k 200k 80k 37 130k 160k 37	The input impedance: Equal to or less than about 170 kΩ	It controls on/off of the mute function of the headphone output.
39, 40	Output terminal for the HP amplifier DC : 2.20 V AC : -4 dBV	V <sub>REG</sub> (4.5 V) Pin 39, pin 40	The output impedance: Equal to or less than about 1 Ω	It is an output pin for the headphone amplifier. The signal which was adjusted in the volume in EVR can be output by the low impedance.

- Technical Data (continued)
- Power dissipation of package HSOP056-P-0300A

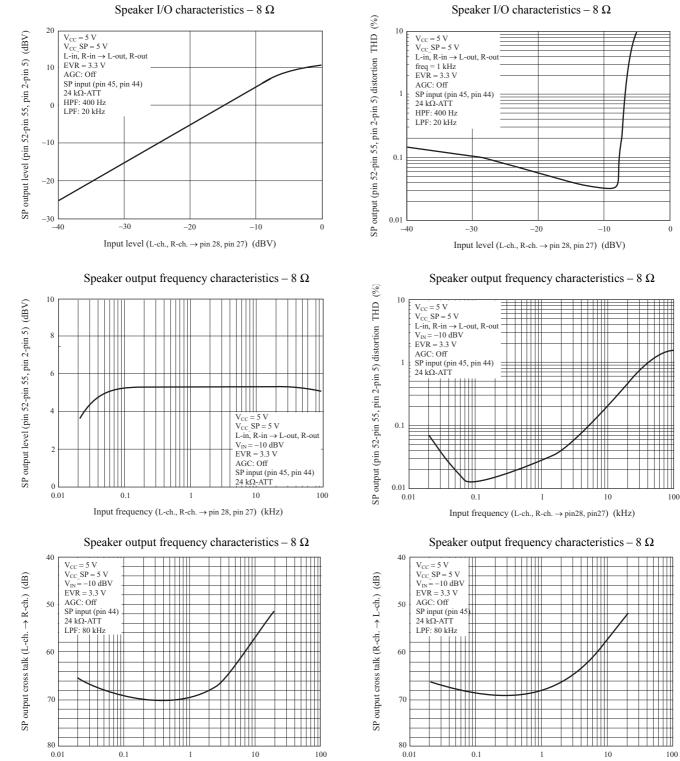


Note) The characteristics listed above are reference values based on the IC design and are not guaranteed.

# Panasonic

#### Technical Data (continued)

- Main characteristics
- 1) Speaker amplifier



SDC00047AEB

Input frequency (L-ch.-pin 28) (kHz)

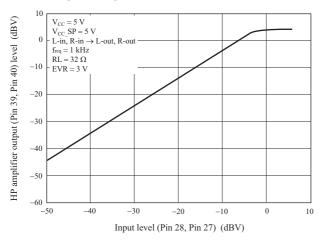
Input frequency (R-ch.-pin 27) (kHz)

# Panasonic

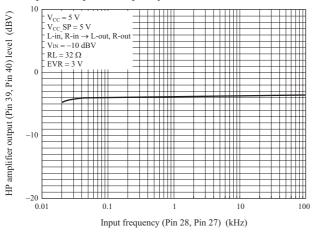
#### Technical Data (continued)

- Main characteristics
- 2) Headphone amplifier

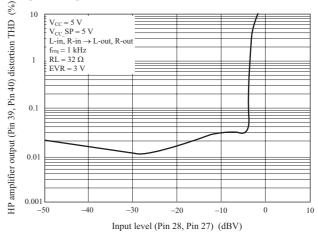
Headphone amplifier I/O characteristics - EVR = max



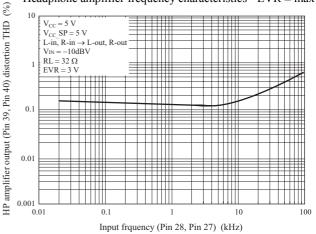
Headphone amplifier frequency characteristics - EVR = max



Headphone amplifier I/O distortion characteristics - EVR = max



Headphone amplifier frequency characteristics - EVR = max

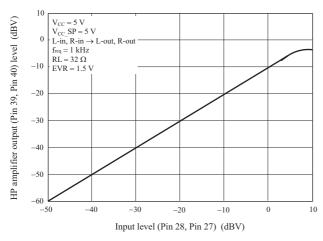


# Panasonic

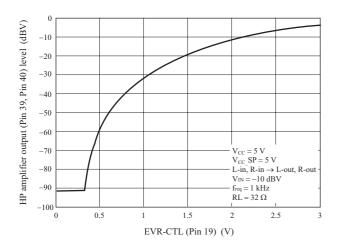
#### Technical Data (continued)

- Main characteristics (continued)
- 2) Headphone amplifier (continued)

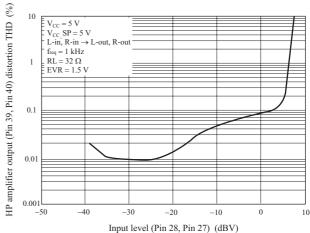
Headphone amplifier I/O characteristics - EVR = typ

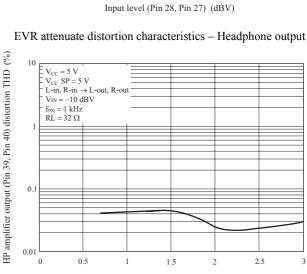


EVR attenuate level characteristics - Headphone output



Headphone amplifier I/O distortion characteristics - EVR = typ



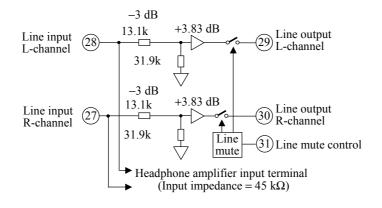


EVR-CTL (Pin 19) (V)

#### Application Notes

1. Linear amplifier circuit block

Following block diagrams is line amplifier circuit.



- 1) The gain of the linear amplifier system is +0.83 dB.
- 2) To become a connection of the standing in the row, the entry impedance of pin 28, pin 27 becomes 22.5 k $\Omega$ . It stores up that these pins also serve as the headphone entry (the impedance = 45 k $\Omega$ ).
- 3) It is possible to adjust to the direction which lowers a gain in adding resistance to pin 28, pin 27.
- But, the gain of the headphone system, too, changes at the same time.

If external resistance is "R"

Gain = 20 log 
$$\frac{31.9 \text{ k}\Omega}{\text{R} + 13.1 \text{ k}\Omega + 31.9 \text{ k}\Omega}$$

- 4) By the mute control by pin 31, the line can be output in the mute.
- 5) For the pop sound measure at the time of power on, delay from the standby cancellation by pin 32 and cancel a linear mute. (Refer to sheet no.2 for circuit constant.)

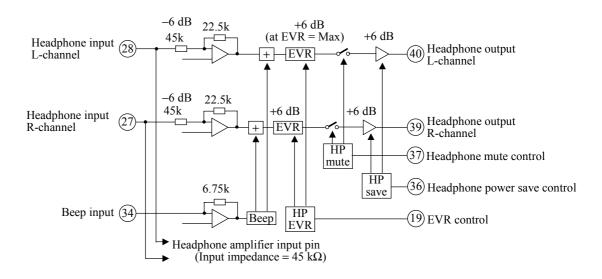
## Design reference value

Parameter	Design reference value	Note
The input/output gain	+0.83 dB	
Input impedance	22.5 kΩ	Note) *: It done the change being of ±10% because there is a change of the inner resistance.
Output impedance	Equal to or less than 10 $\Omega$	Note) *: But, it limits into the sound band range of equal to or less than 50 kHz.
Maximum input level	1.6 dBV	Note) *: The time of the warp (to 5th of THD) of 1% of output.
Maximum output level	3.0 dBV	Note) *: The time of the warp (to 5th of THD) of 1% of output.
Ability of the output drive	Equal to or more than 10 k $\Omega$ of loads	

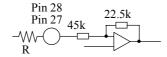
#### Application Notes (continued)

2. Headphone amplifier circuit block

Following block diagrams is headphone amplifier circuit.



- 1) The gain of the headphone amplifier system is +6.0 dB when EVR is maximum.
- 2) To become a connection of the standing in the row, the entry impedance of pin 28, pin 27 becomes 22.5 k $\Omega$ .
- It stores up that these pin also serve as the headphone entry (the impedance = 45 k $\Omega$ ).
- It is possible to adjust to the direction which lowers a gain in adding resistance to pin 28, pin 27. But, the gain of the line system, too, changes at the same time.



If external resistance is "R"

Gain = 20 log 
$$\frac{22.5 \text{ k}\Omega}{\text{R} + 45 \text{ k}\Omega}$$

- 4) By the mute control by pin 37, the headphone can be output in the mute.
- 5) By the EVR control of pin 19, the gain of the headphone output can be variably done.
- 6) The entry of the beep circuit of pin 34 is a virtual grounding entry. Therefore, the external resistance is necessary.
- 7) For the pop sound measure at the time of power on, delay from the standby cancellation by pin 32 and cancel a headphone save mute.

(Refer to sheet no.2 for circuit constant.)

8) When high impedance load is likely to be connected to headphone amplifier output, insert a resistor of 1  $\Omega$  to 4.7 k $\Omega$  so as to lower shock noise at power on or standby on/off.

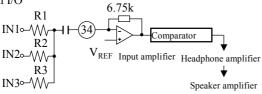
Pin 39  
Pin 40  

$$-\bigcirc$$
  $-\Box$   $+$   $-\bigcirc$   $1k \sim 4.7k$ 

# **Panasonic**

#### Application Notes (continued)

- 2. Headphone amplifier circuit block (continued)
  - Beep signal I/O



Since input amplifier is of a reverse amplifier system, any input to pin 34 through a resistor from some circuits would not cause any drop of input impedance.

Gain of in 1

$$Gain = 20 \log \frac{6.75 \text{ k}\Omega}{\text{R1}}$$

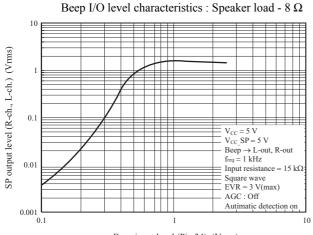
$$Gain \text{ of in 2}$$

$$Gain = 20 \log \frac{6.75 \text{ k}\Omega}{\text{R2}}$$

Threshold level of comparator is 0.1 Vrms to 0.4 Vrms.

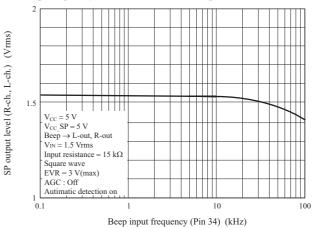
Therefore, keep output of input amplifier equal to or more than 0.4 Vrms.

Equal to or more than 0.4 Vrms ensures that a certain level of beep sound is output to the speaker.





Beep frequency level characteristics : Speaker load - 8  $\Omega$ 



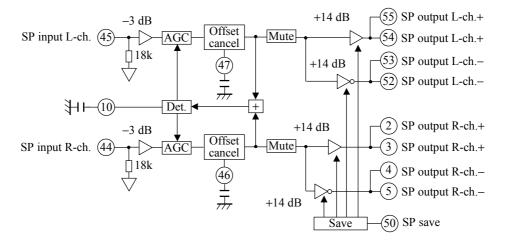
Design reference value

Parameter	Design reference value	Note
The input/output gain	+6.0 dB	Note) *: At EVR is maximum.
Input impedance	22.5 kΩ	Note) *: It done the change being of ±10% because there is a change of the inner resistance.
Output impedance	Equal to or less than 1 $\Omega$	Note) *: But, it limits into the sound band range of equal to or less than 50 kHz.
Maximum input level	3.0 dBV	Note) *: The time of the warp (to 5th of THD) of 1% of output.
Maximum output level	2.4 dBV	Note) *: The time of the warp (to 5th of THD) of 1% of output.
Ability of the output drive	Equal to or more than 32 $\Omega$ of loads	

#### Application Notes (continued)

3. Speaker amplifier circuit block

Following block diagrams is speaker amplifier circuit.



1) The gain of the speaker amplifier system is +17.0 dB.

2) The entry impedance of pin 45, pin 44 becomes 18 k $\Omega$ .

3) It is possible to adjust to the direction which lowers a gain in adding resistance to pin 28, pin 27.

$$\begin{array}{c} \begin{array}{c} \text{Pin 44} \\ \text{Pin 45} \\ \text{-} \\ R \\ 18k \\ \end{array}$$

Gain at insert a resistance

$$Gain = 20 \log \frac{18 \text{ k}\Omega}{\text{R} + 18 \text{ k}\Omega} + 17 \text{ dB}$$

4) By the power save control by pin 50, the speaker can be output in the save mute.

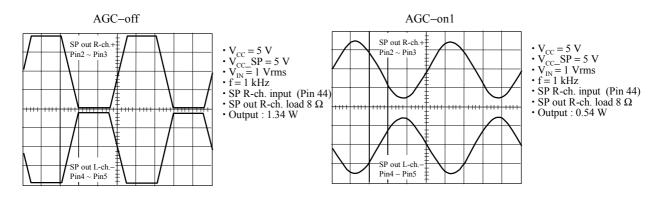
5) For the pop sound measure at the time of power on, delay from the standby cancellation by pin 32 and cancel a speaker save mute.

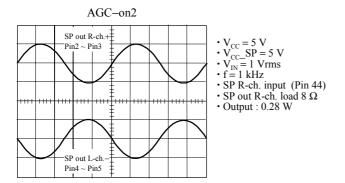
#### Design reference value

Parameter	Design reference value	Note
The input/output gain	+17.0 dB	
Input impedance	18 kΩ	Note) *: It done the change being of ±10% because there is a change of the inner resistance.
Output impedance	Equal to or less than 1 $\Omega$	Note) *: But, it limits into the sound band range of equal to or less than 50 kHz.
Maximum output level	1 W : at 8 $\Omega$ of loads	Note) *: The time of the warp (to 5th of THD) of 10% of output.
Ability of the output drive	Equal to or more than 8 $\Omega$ of loads	

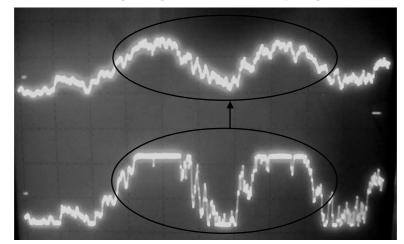
#### Application Notes (continued)

• The output wave at the time of AGC operation It is the following output wave form chart at the AGC operation time.





#### Example: Output waveform of sound signal input



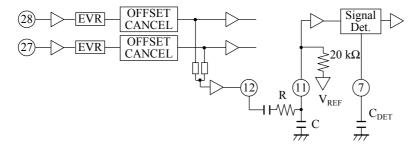
AGC off

AGC on

#### Application Notes (continued)

4. Automatic power save of speaker amplifier function

When input signal becomes zero or very small, a speaker amplifier is automatically power save off.



In the case that a detection circuit operation error to noise, insert "R" and "C" between pin 12 and pin 11 to prevent operation error.

$$f_{\rm C} = \frac{1}{2\pi RC}$$

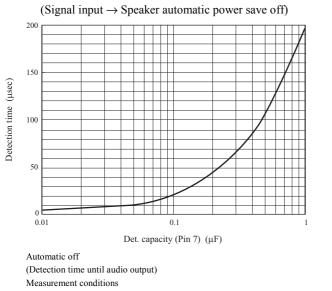
However, that insertion of "R" causes input signal to attenuate.

Det.capacity vs detection time

Gain = 20 log 
$$\frac{20 \text{ k}\Omega}{\text{R} + 20 \text{ k}\Omega}$$

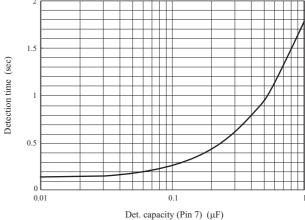
Setting L-channel, R-channel input of -58 dBV (Vol = 1.65 V) as detection threshold, insertion of "R" would drive detection threshold value up for the above gain ...

C<sub>DET</sub> of pin 7 is capacitor to determine detection time.



- $V_{CC}$ ,  $V_{CC}$  SP = 5 V
- Signal input  $\rightarrow$  Time difference until speaker output
- Measure time difference from signal input (sine wave) at no signal status until speaker output.
- Speaker output (load 8  $\Omega$ ) = -4 dBV, f = 1 kHz

Det.capacity vs detection time (Input signal off  $\rightarrow$  Speaker automatic power save on)



Automatic power save on

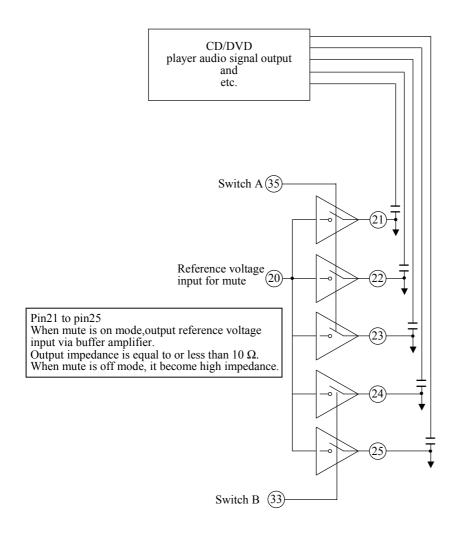
(No sound  $\rightarrow$  Time until power save)

- Measurement conditions •  $V_{CC}$ ,  $V_{CC}$  SP = 5 V
- Input signal off  $\rightarrow$  Time difference until speaker power save
- Measure time difference from switching speaker signal (sine wave) output to no input until speaker power save.
- Speaker output (load 8  $\Omega$ ) = -4 dBV, f = 1 kHz

# **Panasonic**

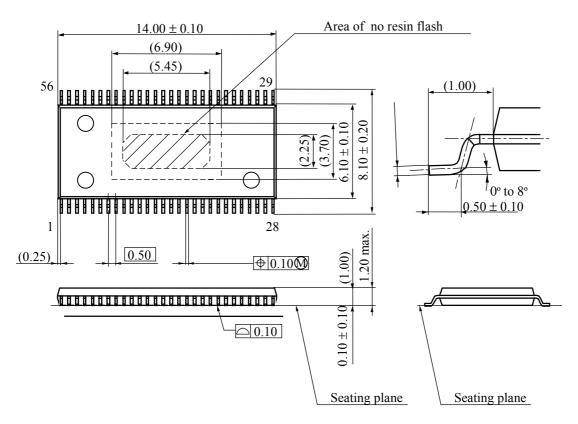
### Application Notes (continued)

5. Mute switch of signal line circuit



Note) \* : Refer to sheet no.12 for circuit of inner IC

- Outside figure (Unit: mm)
- HSOP056-P-0300A (Lead-free package)



## Usage Notes

- Avoid the power line short and the ground short of the terminals.
- Especially positive phase speaker output pins (pin 2, pin 3, pin 54 and pin 55) and negative phase speaker output pins (pin 4, pin 5, pin 52 and pin 53) have the possibility of break-down caused by the power line short and the ground short. Be sure to avoid power line short, ground short and load short.

## Request for your special attention and precautions in using the technical information and semiconductors described in this material

- (1) An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this material and controlled under the "Foreign Exchange and Foreign Trade Law" is to be exported or taken out of Japan.
- (2) The technical information described in this material is limited to showing representative characteristics and applied circuits examples of the products. It neither warrants non-infringement of intellectual property right or any other rights owned by our company or a third party, nor grants any license.
- (3) We are not liable for the infringement of rights owned by a third party arising out of the use of the product or technologies as described in this material.
- (4) The products described in this material are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).

Consult our sales staff in advance for information on the following applications:

- Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.
- (5) The products and product specifications described in this material are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.
- (6) When designing your equipment, comply with the guaranteed values, in particular those of maximum rating, the range of operating power supply voltage, and heat radiation characteristics. Otherwise, we will not be liable for any defect which may arise later in your equipment. Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
- (7) When using products for which damp-proof packing is required, observe the conditions (including shelf life and amount of time let standing of unsealed items) agreed upon when specification sheets are individually exchanged.
- (8) This material may be not reprinted or reproduced whether wholly or partially, without the prior written permission of Matsushita Electric Industrial Co., Ltd.

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.