4 CHANNEL BTL DRIVER FOR VCD PLAYERS AZ6392

General Description

The AZ6392 is a 4-channel BTL driver for VCD player motors and actuators. It has an internal primary filter, and can be directly connected (without attached components) to the servo PWM output of all drivers other than the spindle driver.

In AZ6392, PWM-input is filtered by the internal primary filter, eliminating the need for attached resistors and capacitors, thereby helping reduce the number of components. Resistor and capacitor time constants can also be changed with attached components.

The AZ6392 is available in HSOP-28 package.

Features

- HSOP 28-pin Package Allows for Miniaturization of Applications
- PWM-Input Filtered by the Internal Primary Filter
- Internal Thermal Shutdown Circuit
- Internal Mute Circuit

Applications

- VCD Driver

HSOP-28

Figure 1. Package Type of AZ6392

Pin Configuration

M28 Package
(HSOP-28)

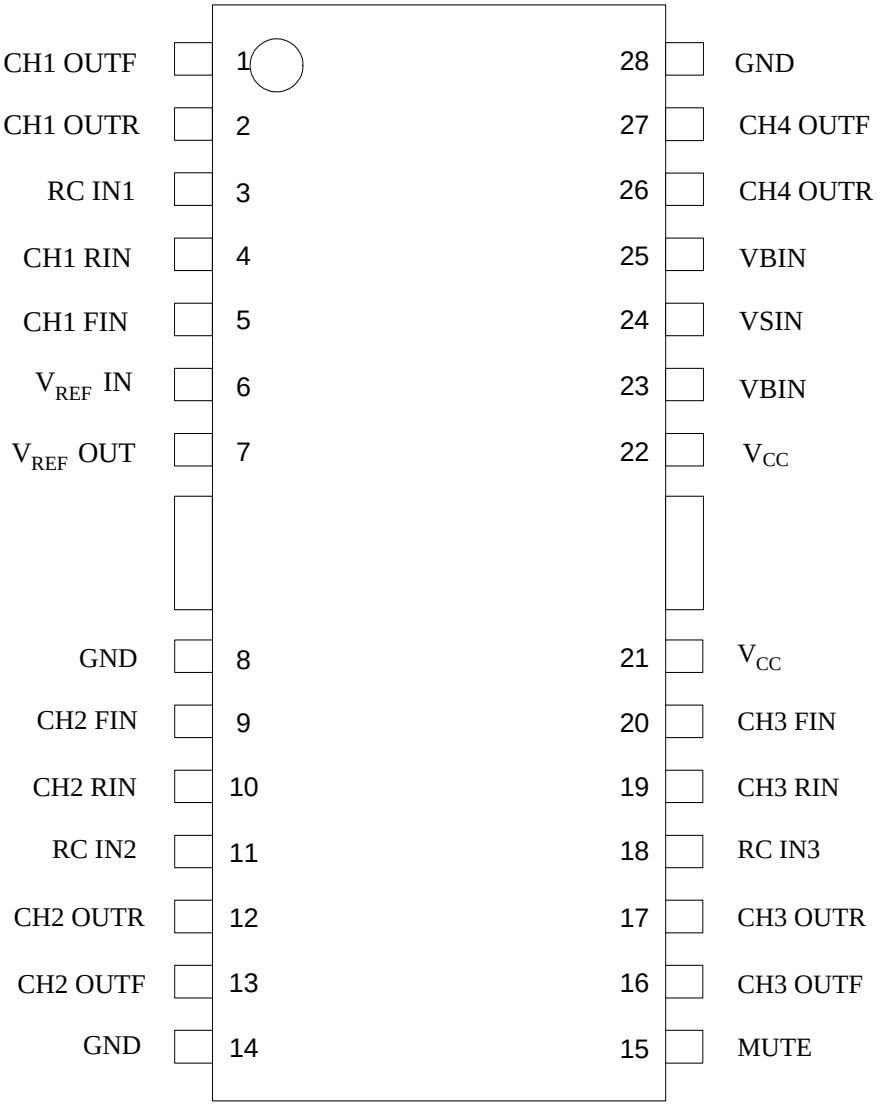


Figure 2. Pin Configuration of AZ6392 (Top View)

Pin Description

Pin Number	Pin Name	Function
1	CH1 OUTF	Driver channel 1 forward output
2	CH1 OUTR	Driver channel 1 reverse output
3	RC IN1	Connect to attached resistor/capacitor (1)
4	CH1 RIN	Driver channel 1 reverse input
5	CH1 FIN	Driver Channel 1 forward input
6	V_{REF} IN	Internal reference amplifier input
7	V_{REF} OUT	Internal reference amplifier output
8	GND	Ground for internal reference and internal power circuit
9	CH2 FIN	Driver channel 2 forward input
10	CH2 RIN	Driver channel 2 reverse input
11	RC IN2	Connect to attached resistor/capacitor (2)
12	CH2 OUTR	Driver channel 2 reverse output
13	CH2 OUTF	Driver channel 2 forward output
14	GND	Ground
15	MUTE	Driver mute control input
16	CH3 OUTF	Driver channel 3 forward output
17	CH3 OUTR	Driver channel 3 reverse output
18	RC IN3	Connect to attached resistor/capacitor (3)
19	CH3 RIN	Driver channel 3 reverse input
20	CH3 FIN	Driver channel 3 forward input
21	V_{CC}	Power supply
22	V_{CC}	Power supply
23	VBIN	Driver channel 4 bias input
24	VSIN	Driver channel 4 input
25	VBIN	Driver channel 4 bias input
26	CH4 OUTR	Driver channel 4 reverse output
27	CH4 OUTF	Driver channel 4 forward output
28	GND	Ground

Functional Block Diagram

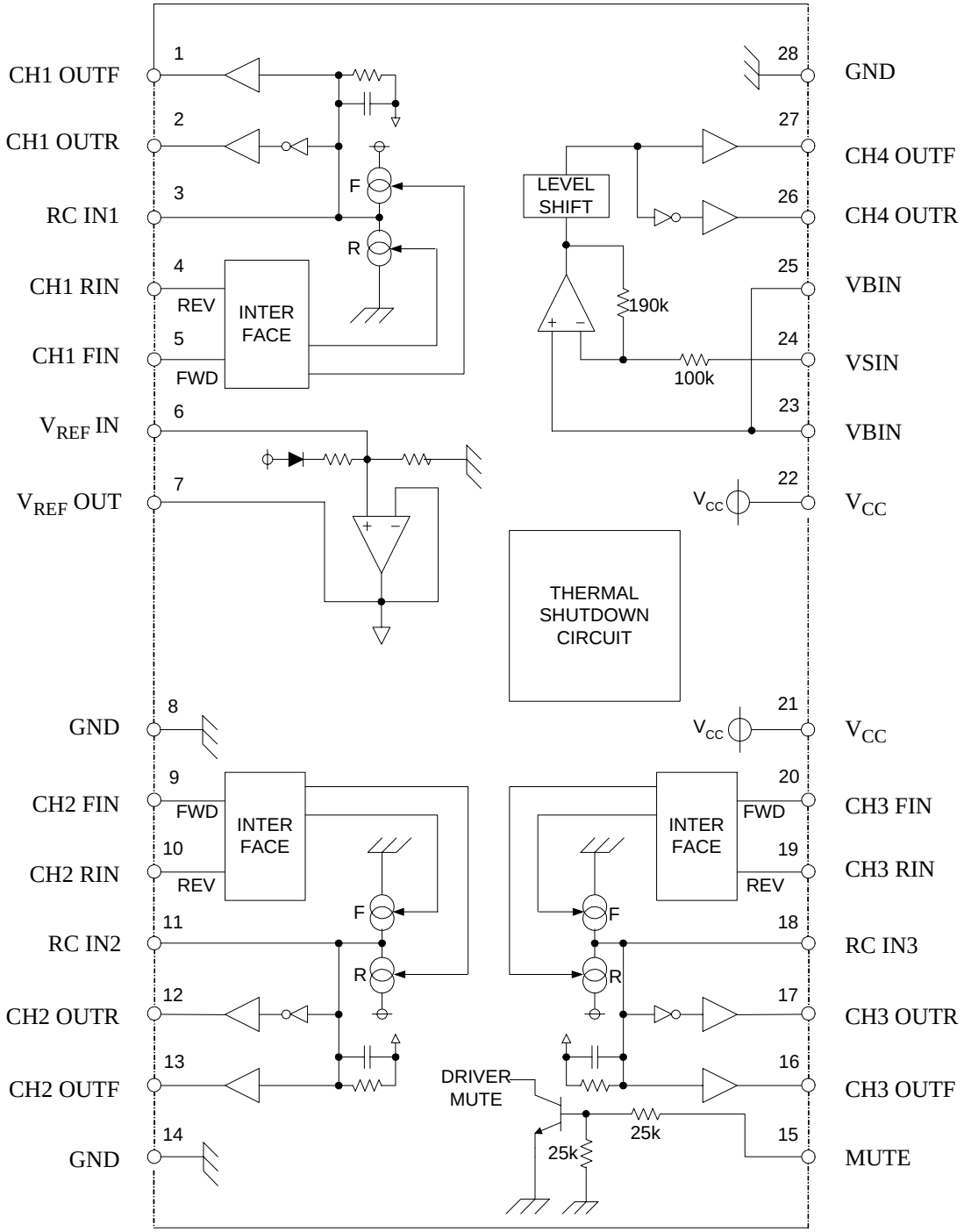
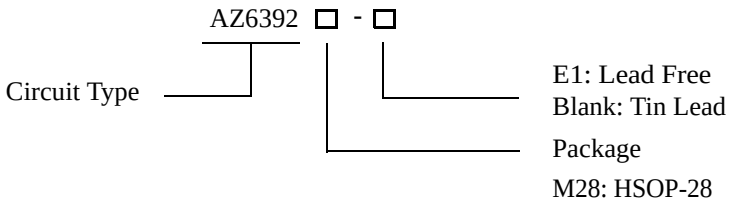


Figure 3. Functional Block Diagram of AZ6392

Ordering Information



Package	Temperature Range	Part Number		Marking ID		Packing Type
		Tin Lead	Lead Free	Tin Lead	Lead Free	
HSOP-28	0 to 70°C	AZ6392M28	AZ6392M28-E1	AZ6392M28	AZ6392M28-E1	Tube

BCD Semiconductor's Pb-free products, as designated with "E1" suffix in the part number, are RoHS compliant.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	1.7 (Note2)	W
Storage Temperature	T_{STG}	-55 to 150	°C

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Note 2: The power dissipation is reduced by 13.6mW for each increase in T_A of 1°C over 25°C when mounted on a 50 x 50 x 1.0 mm phenol paper PCB.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Note 3)	V_{CC}	6	16	V
Operating Temperature	T_A	0	70	°C

Note 3: Set the power supply voltage according to the power dissipation.

Electrical Characteristics

(V_{CC}=8V, R_L=8Ω, f=1kHz, T_A= 25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Current	I_Q	No load	8	12	18	mA
Bias Pin Voltage	V_{BIAS}		3.4	3.7	4.0	V
Bias Pin Voltage Variance	ΔV_{BIAS}	1mA source, sink	-30		30	mV
Mute-Off Voltage	V_{MOFF}		2.0			V
Mute-On Voltage	V_{MON}				0.5	V
Drivers (other than spindle)						
Input High Level Voltage	V_{IH}		2.4			V
Input Low Level Voltage	V_{IL}				0.5	V
Input High Level Current	I_{IH}	V_{IN} = 5V	170	300	450	μA
Input Low Level Current	I_{IL}	V_{IN} = 0V	-25		0	μA
Output Offset Voltage	V_{OO}	(Same for spindle)	-30		30	mV
Output High Level Voltage	V_{OH}	FIN = 5V, RIN = 0	5.2	5.5		V
Output Low Level Voltage	V_{OL}	FIN = 0, RIN = 5V		1.3	1.6	V
Constant Current	I_{CONST}		14	24	30	μA
Internal Integral Capacitance	C			24		pF
Current Pulse Rise Time 1	Δtr	At startup		0.12		μS
Current Pulse Fall Time 2	Δtf	At shutdown		0.8		μS
Current Pulse Time Differential	Δtr-f		-160		160	μS
Drive Linearity	LIN	V_{IN} = V_{REF} ± 0.5, 1, 1.5V (Note 4)	90	100	110	%
Ripple Rejection	RR	V_{IN} = 100mV_{RMS}, 100Hz		70		dB
Spindle Driver						
Input Bias Current	I_B			10	300	nA
Synchronous Input Voltage	V_{ICM}		1.6		6.4	V
Output High Level Voltage	V_{OHD}		5.2	5.6		V
Output Low Level Voltage	V_{OLD}			1.5	1.8	V
Voltage Gain	G_{VC}		8.0	11.3	13.0	dB
Slew Rate	SR			5		V/μS
Ripple Rejection	RRs	V_{IN} = 100mV_{RMS}, 100Hz		70		dB

Note 4: If V_O=V_{O1} when V_{IN}=V_{REF} ± 0.5V, V_O=V_{O2} when V_{IN}=V_{REF} ± 1.0V, and V_O=V_{O3} when V_{IN}=V_{REF} ± 1.5V, then L_{IN}=(V_{O3}-V_{O2})/(V_{O2}-V_{O1}) x100%.

Typical Performance Characteristics

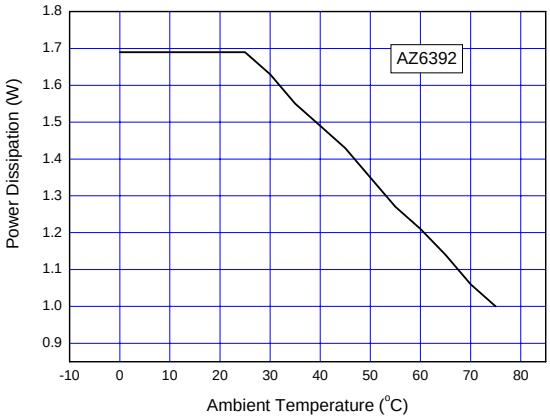


Figure 4. Thermal Derating Curve

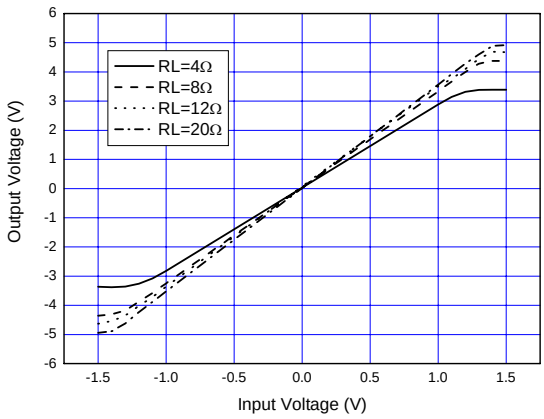


Figure 5. I/O Characteristics of Spindle Driver (CH4) (Load Variation)

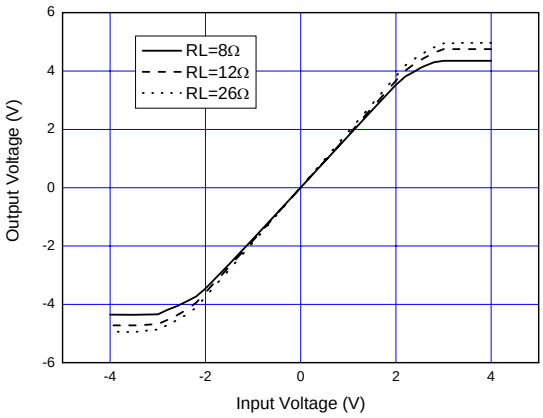


Figure 6. I/O Characteristics of Driving Stages (CH1)

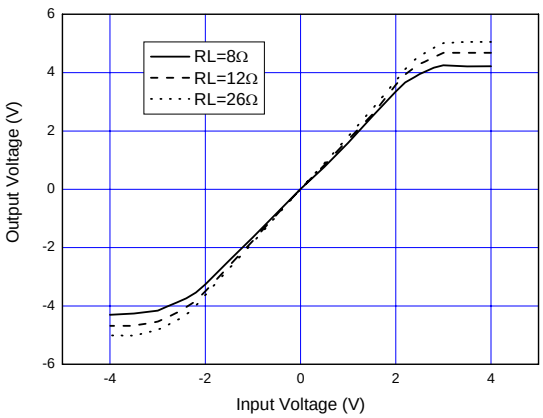


Figure 7. I/O Characteristics of Driver Stages (CH2)

Typical Performance Characteristics (Continued)

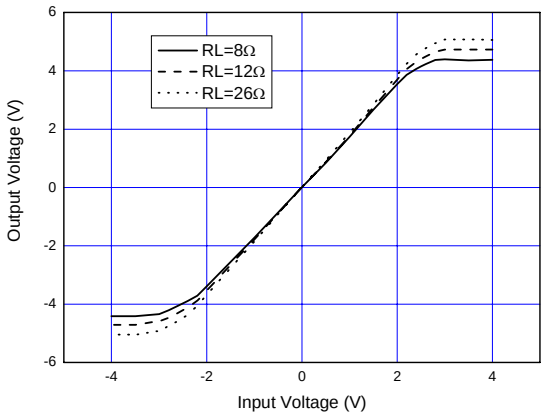


Figure 8. I/O Characteristics of Driver Stages (CH3)

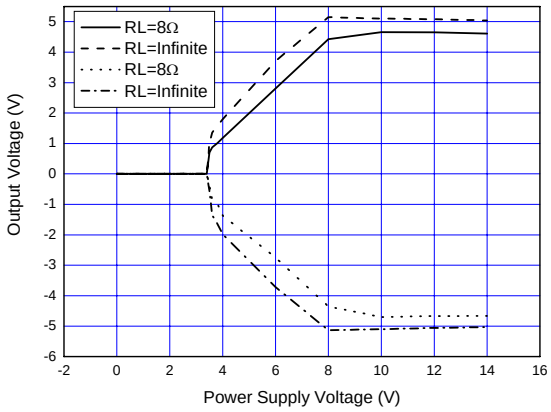


Figure 9.Driver (CH1) Supply Voltage vs. Output Voltage

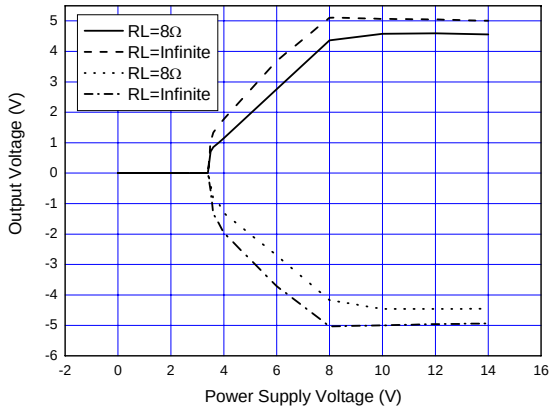


Figure 10.Driver (CH2) Supply Voltage vs. Output Voltage

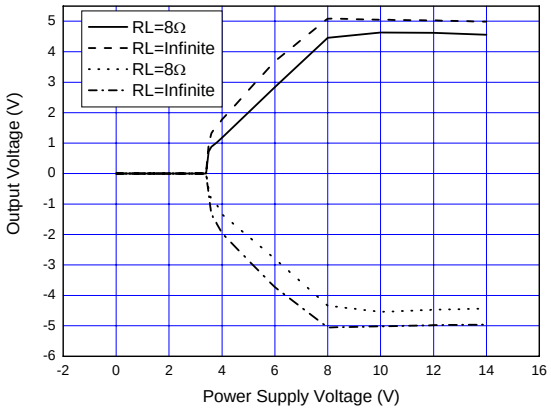


Figure 11.Driver (CH3) Supply Voltage vs. Output Voltage

Input and Output Circuits

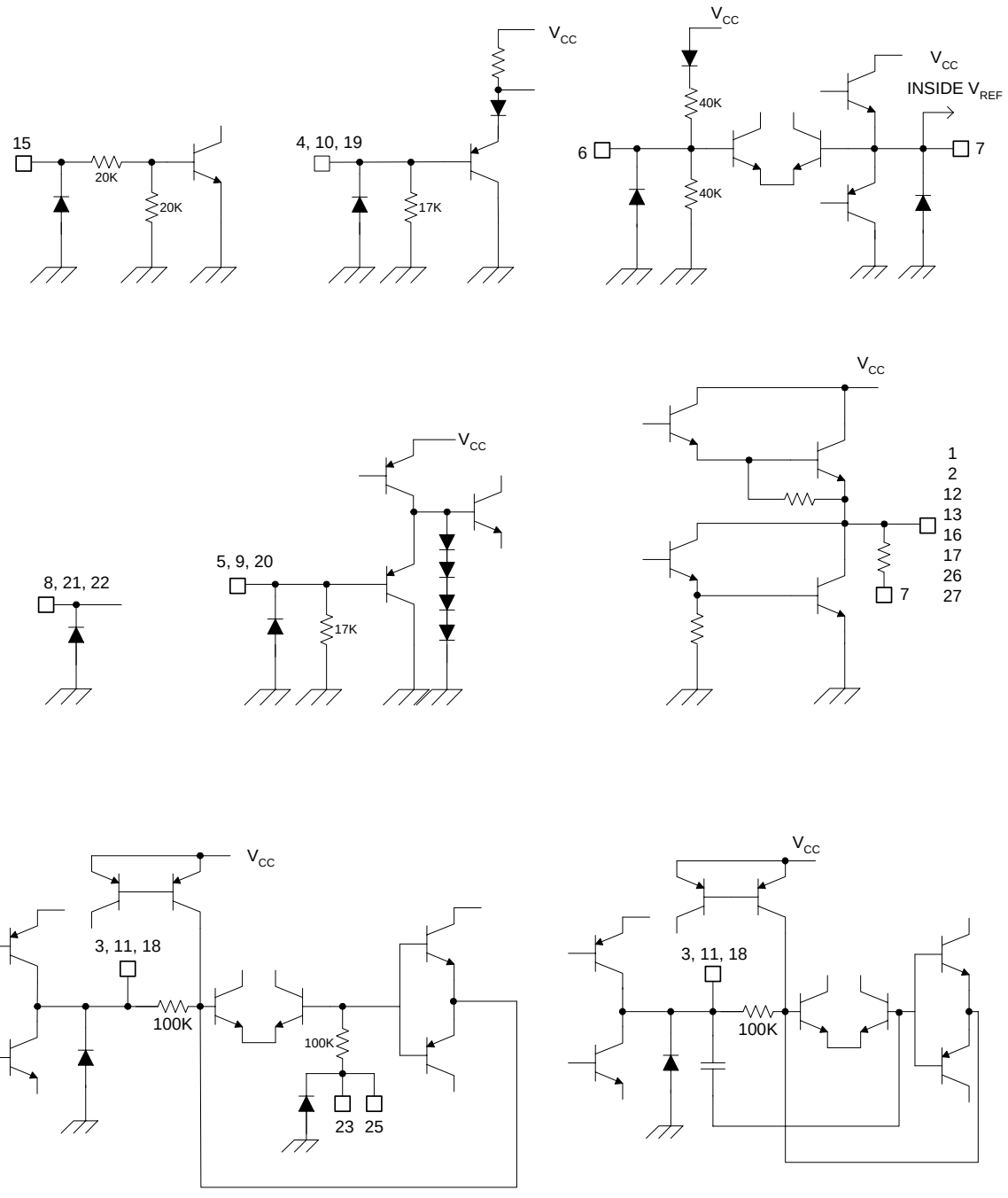


Figure 12. Input and Output Circuits

Application Information

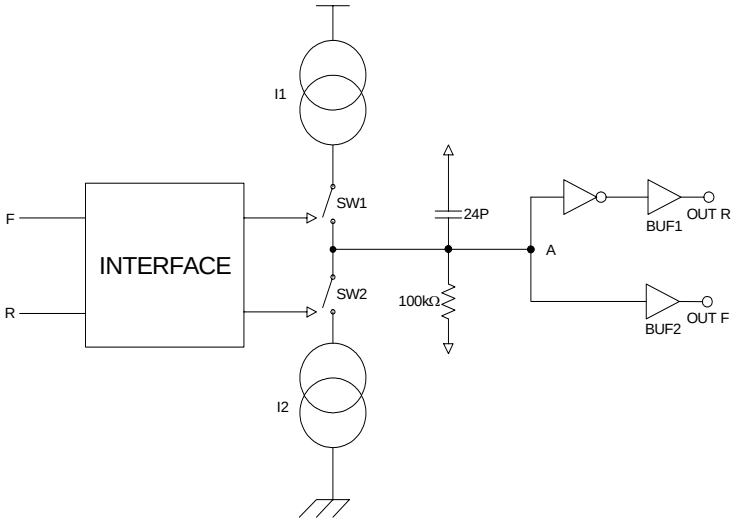


Figure 13

1. Circuit Operation explanation

SW1 is on when the forward input signal (HIGH Level, over 2.4V) is present. SW2 is on when the reverse input signal is present (Figure 13)

Figure 14 shows the inputs from the digital servo IC for CH1 to CH3 drivers (all drivers except the spindle).

The constant current (I1) at this time enters the RC and generates an integral waveform based on the duty of the input waveform. The BTL is output from BUF1 and BUF2 (Figure 15). The logic table is below.

F	R	SW1	SW2
L	L	OFF	OFF
L	H	OFF	ON
H	L	ON	OFF
H	H	OFF	OFF

$H \geq 2.4$ V
$L \leq 0.5$ V

To maintain the HIGH level with forward (or reverse) input, the DC voltage generated at point A is:

I1 x R ≈ 2.5V (reverse: -2.5V)

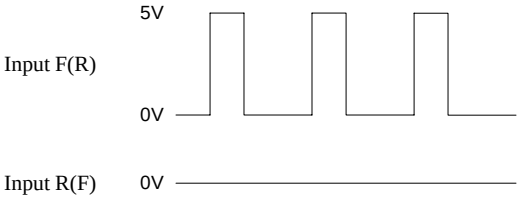


Figure 14

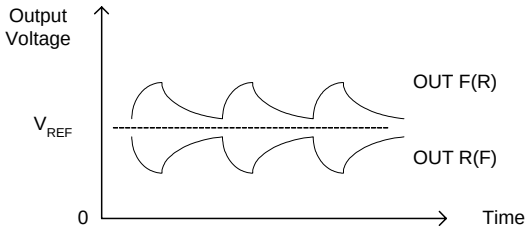


Figure 15

This is the voltage generated relative V_{REF}. The setting is such that a voltage differential of 5V is generated between output pins. The time constant is:

R x C =2.4μs

Application Information (Continued)

This can be increased by inserting a capacitor between point A (Pin 3, 11 and 18) and V_{REF}. The constant current (I_{CONST}) given in the electrical characteristics refers to I1 and I2 in Figure 13.

2. CH4 Driver (Spindle Driver)

Pins 23 and 25 are shorted inside the IC. Bias amplitudes are the primary type of inputs assumed. The level shift circuit converts the pre-stage amplifier output (centered on the bias level and impressed on pins 23 and 25) to positive and negative amplitudes centered on V_{REF}. The level shift circuit's output is BTL-output from the buffer amplifier.

Because of the high input impedance, the IC is designed to accommodate a filter comprising attached resistors and capacitors.

Figure 16 is an example for secondary filters.

3. Some Notes for Operation

1). The AZ6392 has an internal thermal shutdown circuit. Output current is muted when the chip temperature exceeds 180 ^{o}C (Typ.).

2). The output current can also be muted by lowering the mute pin (pin 15) voltage below 0.5V.

3). All four driver output channels are muted during thermal shutdown, muting and a drop in bias pin voltage. No other components are muted.

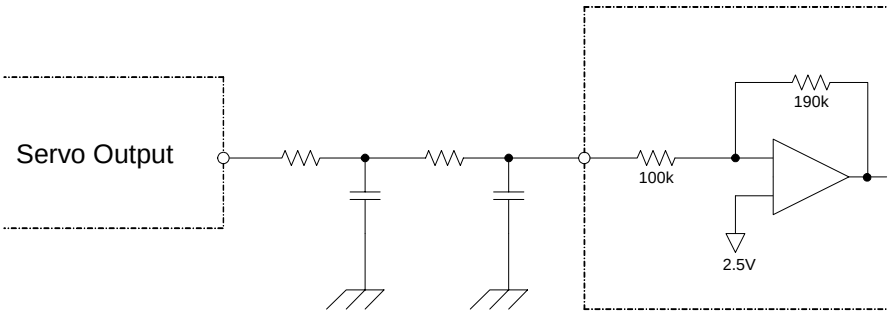
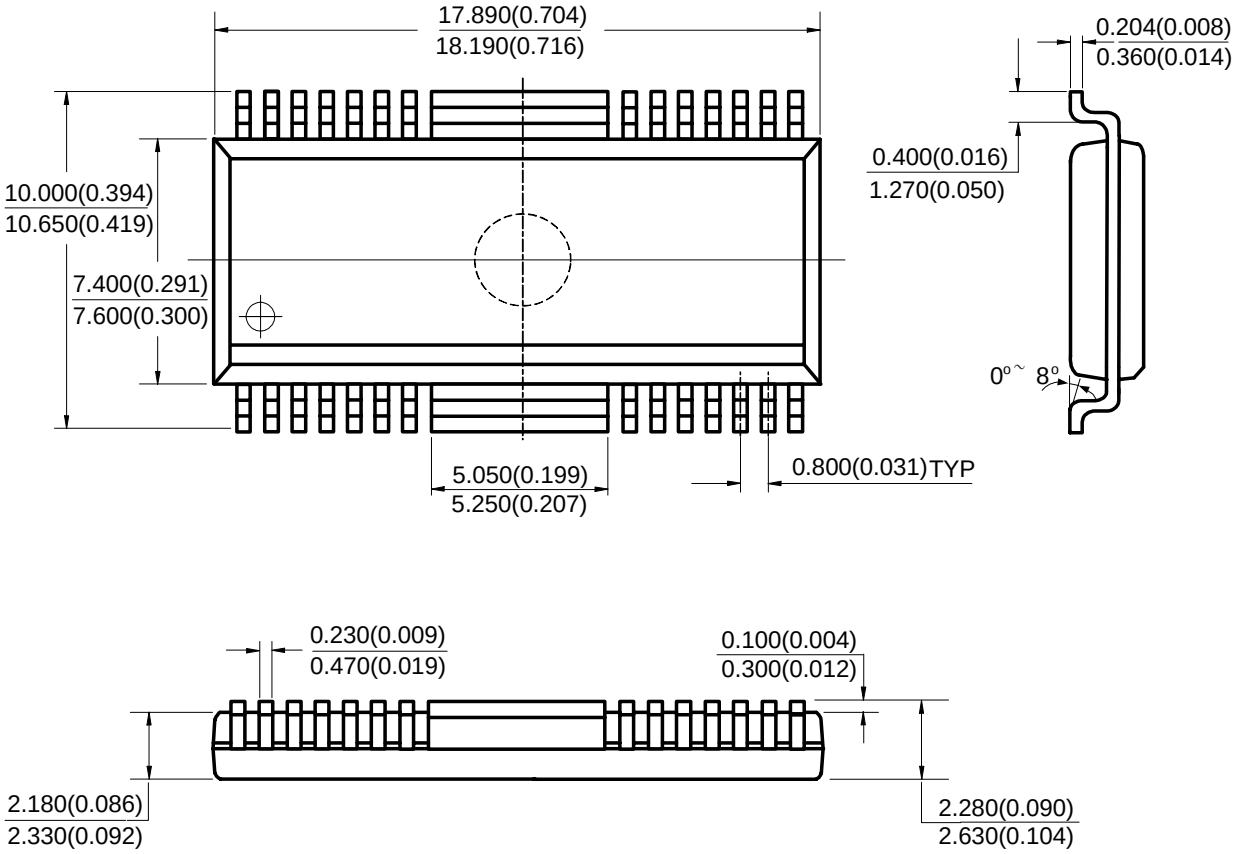


Figure 16

Mechanical Dimensions

HSOP-28 **Unit: mm(inch)**



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