Zero[1] Loss Automatic X Capacitor Discharge IC

Product Highlights

- Blocks current through X capacitor discharge resistors when AC voltage is connected
- Automatically discharges X capacitors through discharge resistors when AC is disconnected
- Simplifies EMI filter design – larger X capacitor allows smaller inductive components with no change in consumption
- Only two terminals – meets safety standards for use before or after system input fuse
- >4 mm creepage on package and PCB
- Self supplied – no external bias required
- High common mode surge immunity – no external ground connection
- High differential surge withstand – 1000 V internal MOSFETs

EcoSmart® – Energy Efficient

- <5 mW consumption at 230 VAC for all X capacitor values

Applications

- All ACDC converters with X capacitors >100 nF
- Appliances requiring EuP Lot 6 compliance
- Adapters requiring ultra low no-load consumption
- All converters requiring very low standby power

Description

When AC voltage is applied, CAPZero blocks current flow in the X capacitor safety discharge resistors, reducing the power loss to less than 5 mW, or essentially zero[1] at 230 VAC. When AC voltage is disconnected, CAPZero automatically discharges the X capacitor by connecting the series discharge resistors. This operation allows total flexibility in the choice of the X capacitor to optimize differential mode EMI filtering and reduce inductor costs, with no change in power consumption.

Designing with CAPZero is simply a matter of selecting the appropriate CAPZero device and external resistor values in Table 1 for the X capacitor value being used. This design choice will provide a worst case RC time constant, when the AC supply is disconnected, of less than 1 second as required by international safety standards.

The simplicity and ruggedness of the two terminal CAPZero IC makes it an ideal choice in systems designed to meet EuP Lot 6 requirements.

The CAPZero family has two voltage grades: 825 V and 1000 V. The voltage rating required depends on surge requirement and circuit configuration of the application. See Key Applications Considerations section for details.

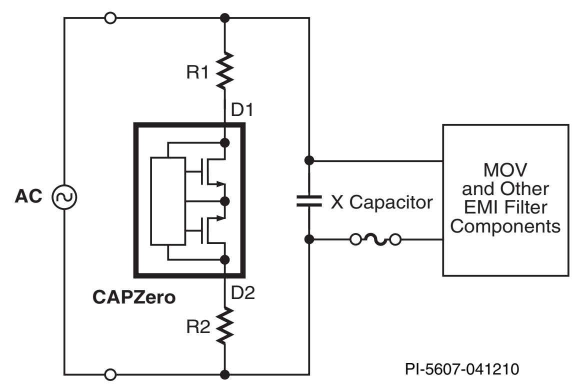


Figure 1. Typical Application – Not a Simplified Circuit.

Component Selection Table

Product[3]	BV_{DSS}	Max Total X Capacitance	Total Series Resistance[2] (R1 + R2)
CAP002DG	825 V	500 nF	1.5 MΩ
CAP012DG	1000 V		
CAP003DG	825 V	750 nF	1.02 MΩ
CAP013DG	1000 V		
CAP004DG	825 V	1 µF	780 kΩ
CAP014DG	1000 V		
CAP005DG	825 V	1.5 µF	480 kΩ
CAP015DG	1000 V		
CAP006DG	825 V	2 µF	360 kΩ
CAP016DG	1000 V		
CAP007DG	825 V	2.5 µF	300 kΩ
CAP017DG	1000 V		
CAP008DG	825 V	3.5 µF	200 kΩ
CAP018DG	1000 V		
CAP009DG	825 V	5 µF	150 kΩ
CAP019DG	1000 V		

Table 1. Component Selection Table.

Notes:
1. IEC 16301 clause 4.5 rounds standby power use below 5 mW to zero.
2. Values are nominal. RC time constant is <1 second with ±20% X capacitor and ±5% resistance from these nominal values.
3. Packages: D: SO-8.

Pin Functional Description

The pin configuration of Figure 2 ensures that the width of the SO-8 package is used to provide creepage and clearance distance of over 4 mm.

Although electrical connections are only made to pins 2, 3, 6 and 7, it is recommended that pins 1-4 and pins 5-8 are coupled together on the PCB – See Applications Section.

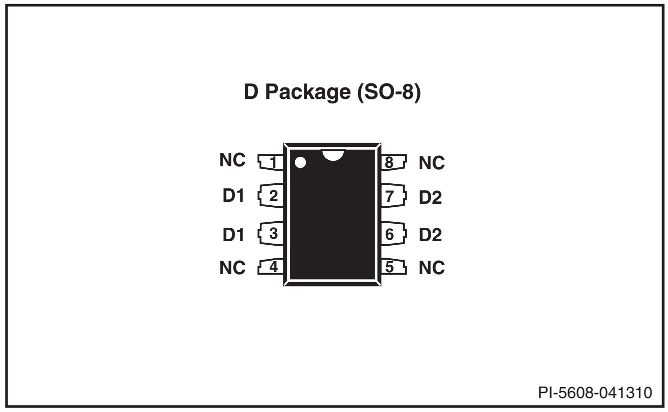


Figure 2. Pin Configuration.

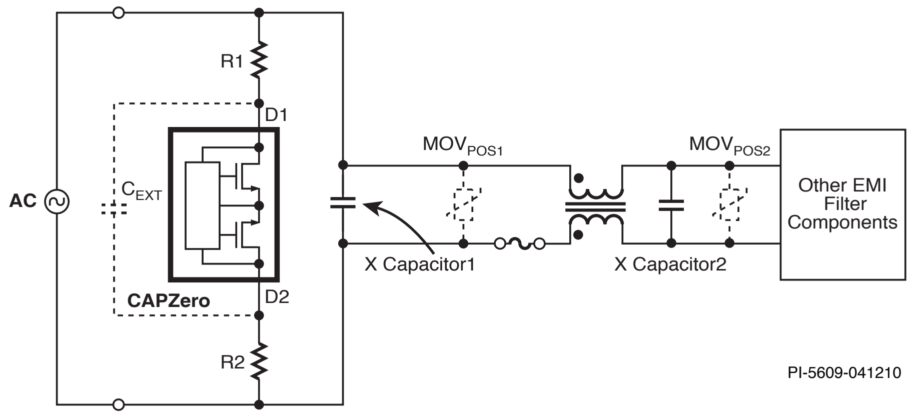


Figure 3. Placement Options of MOV and C_{EXT}.

Key Application Considerations

Breakdown Voltage Selection

Figure 3 illustrates possible system configurations influencing the choice of CAPZero breakdown voltage. The system configuration variables include the placement of the system MOV and X capacitor(s) as well as the differential surge voltage specifications of the application.

As shown in Table 1, each device in the CAPZero family has a 825 V or 1000 V option. For applications where the system MOV is placed in position 1 (MOV_{POS1} in Figure 3), the 825 V option will typically provide adequate voltage withstand for surge requirements up to 3 kV or more. The 1 kV CAPZero would be recommended for higher surge requirements or if additional voltage margin is required.

For MOV placement that is not directly across the X Capacitor1 (for example MOV_{POS2} in Figure 3) the 1000 V CAPZero devices can be used up to a surge specification of 1.5 kV. For differential surge voltage specifications of >1.5 kV it is recommended that the MOV is always placed in the location shown in Figure 3 as MOV_{POS1}.

It is always recommended that the peak voltage between terminals D1 and D2 of CAPZero is measured during surge tests in the final system. Measurements of peak voltage across CAPZero during surge tests should be made with oscilloscope probes having appropriate voltage rating and using an isolated supply to the oscilloscope to avoid ground currents influencing measurement results. When making such measurements, it is recommended that 50 V engineering margin is allowed below the breakdown voltage specification (for example 950 V with the 1000 V CAPZero).

If the measured peak Drain voltage exceeds 950 V, an external 1 kV ceramic capacitor of value up to 47 pF can also be placed between D1 and D2 terminals to attenuate the voltage applied between the CAPZero terminals during surge. This optional external capacitor placement is shown as C_{EXT} in Figure 3. It should be noted that use of an external capacitor in this way will increase power consumption slightly due to the C_{EXT} charge/discharge currents flowing in R1 and R2 while AC is connected. A C_{EXT} value of 33 pF will add approximately 0.5 mW at 230 VAC 50 Hz.

PCB Layout and External Resistor Selection

Figure 4 shows a typical PCB layout configuration for CAPZero. The external resistors in this case are divided into two separate surface mount resistors to distribute loss under fault conditions – for example where a short circuit exists between CAPZero terminals D1 and D2. R1 and R2 values are selected according to Table 1.

Under a fault condition where CAPZero terminals D1 and D2 are shorted together, each resistor will dissipate a power that can be calculated from the applied AC voltage and the R1 and R2 values. For example in an application using CAP004 or CAP014, R1=R2=390 kΩ. If CAPZero is shorted out at 265 VAC R1 and R2 will each dissipate 45 mW.

Resistors R1 and R2 should also be rated for 50% of the system input voltage again to allow for the short circuitry of CAPZero D1 to D2 pins during single point fault testing.

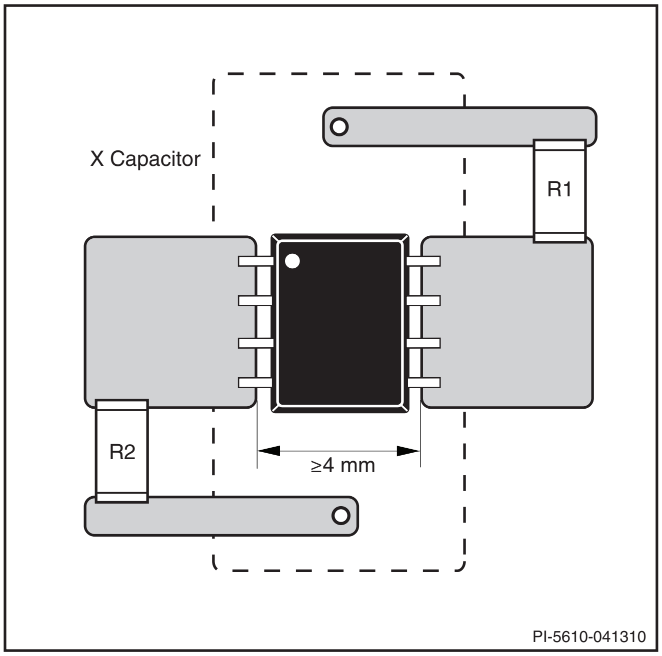


Figure 4. Typical PCB Layout.

If lower dissipation or lower voltage across each resistor is required during fault tests, the total external resistance can be divided into more discrete resistors, however the total resistance must be equal to that specified in Table 1.

Safety

CAPZero meets safety requirements even if placed before the system input fuse. If a short circuit is placed between D1 and D2 terminals of CAPZero, the system is identical to existing systems where CAPZero is not used.

With regard to open circuit tests, it is not possible to create a fault condition through a single pin fault (for example lifted pin test) since there are two pins connected to each of D1 and D2. If several pins are lifted to create an open circuit, the condition is identical to an open circuit X capacitor discharge resistor in existing systems where CAPZero is not used. If redundancy against open circuit faults is required, two CAPZero and R1 / R2 configurations can be placed in parallel.

Absolute Maximum Ratings

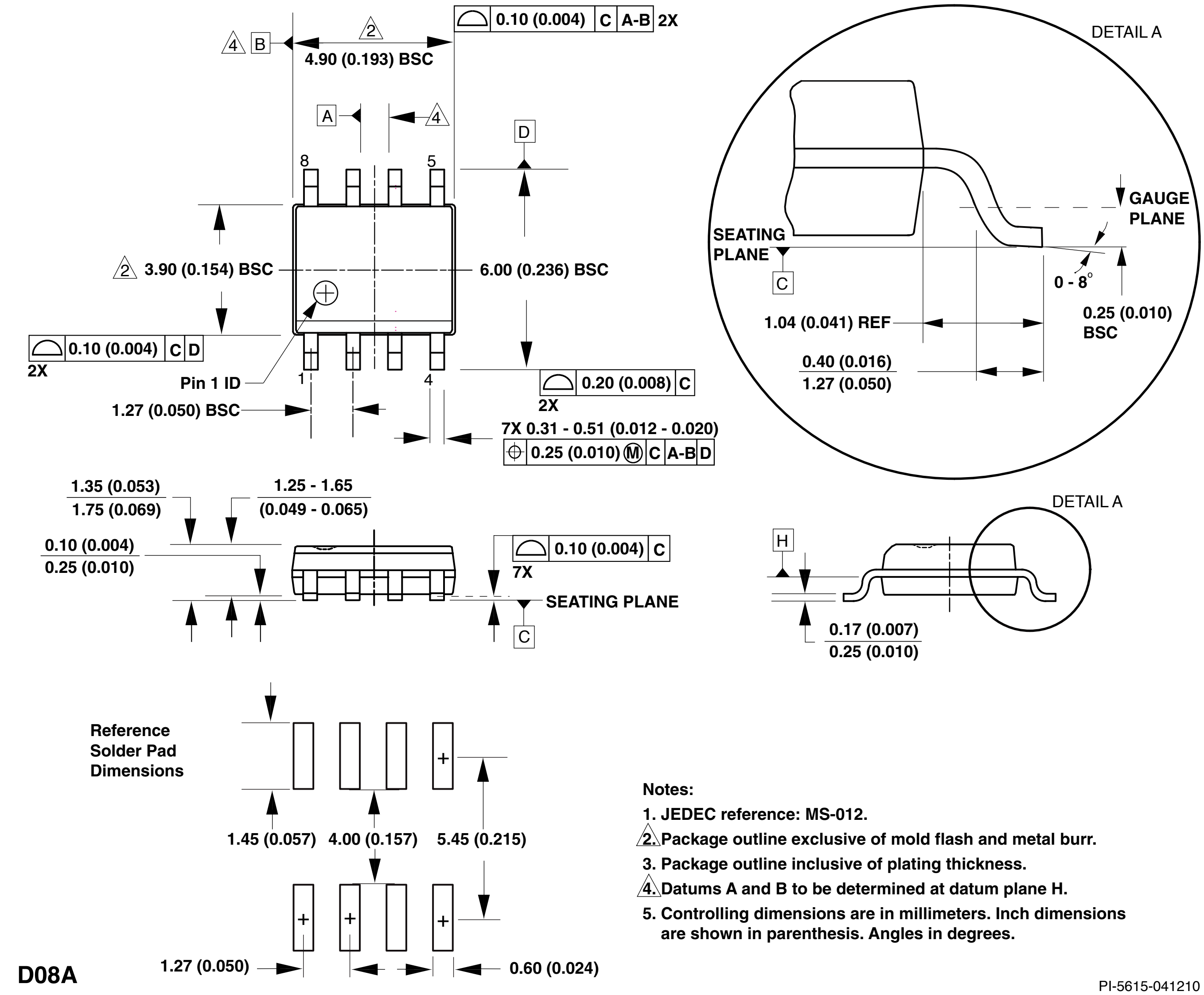
DRAIN Pin Voltage[1] CAP002-CAP009 .... 825 V
DRAIN Pin Voltage[1] CAP012-CAP019..............................1000 V

Notes:
1. Voltage of D1 pin relative to D2 pin in either polarity.

Parameter	Symbol	Conditions T_J = 0 to 105 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
AC Removal Detection Time	t_{DETECT}	Line Cycle Frequency 47-63 Hz	0.5		2	Line Cycles
Drain Saturation Current[1,2]	I_{DSAT}	CAP002/012	0.25			mA
		CAP003/013	0.37			
		CAP004/014	0.48			
		CAP005/015	0.78			
		CAP006/016	1.04			
		CAP007/017	1.25			
		CAP008/018	1.88			
		CAP009/019	2.5			
Supply Current	I_{Supply}				21.7	µA

Notes
1. Saturation current specifications ensure a natural RC discharge characteristic at all voltages up to 265 VAC pk with the external resistor values specified in Component Selection Table 1.
2. Specifications are guaranteed by characterization and design.

SO-8 (D Package)



Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

Part Ordering Information

CAP 002 D G - TL

- **CAPZero Product Family**
- **002 Series Number**
- **Package Identifier**

D	Plastic SO-8

- **Package Material**

G	GREEN: Halogen Free and RoHS Compliant

- **Tape & Reel and Other Options**

Blank	Standard Configurations
TL	Tape & Reel, 2.5 k pcs.

Revision	Notes	Date
A	Code A release	04/14/10

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Patent Information

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