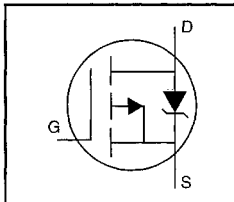


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- 175°C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = -60V$$

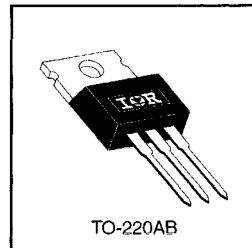
$$R_{DS(on)} = 0.50\Omega$$

$$I_D = -6.7A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

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Absolute Maximum Ratings

Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	-6.7	A
$I_D @ T_C = 100^\circ C$	-4.7	
I_{DM}	-27	
$P_D @ T_C = 25^\circ C$	43	W
	0.29	W/°C
V_{GS}	±20	V
E_{AS}	140	mJ
I_{AR}	-6.7	A
E_{AR}	4.3	mJ
dv/dt	-4.5	V/ns
T_J	-55 to +175	°C
T_{STG}		
	300 (1.6mm from case)	
	10 lbf•in (1.1 N•m)	

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	—	—	3.5	°C/W
$R_{\theta CS}$	—	0.50	—	
$R_{\theta JA}$	—	—	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V _{GS} =0V, I _D =-250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.060	—	V/°C	Reference to 25°C, I _D =-1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.50	Ω	V _{GS} =-10V, I _D =-4.0A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} =V _{GS} , I _D =-250μA
g _{fs}	Forward Transconductance	1.4	—	—	S	V _{DS} =-25V, I _D =-4.0A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	V _{DS} =-60V, V _{GS} =0V
		—	—	-500		V _{DS} =-48V, V _{GS} =0V, T _J =150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} =-20V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} =20V
Q _g	Total Gate Charge	—	—	12		I _D =-6.7A
Q _{gs}	Gate-to-Source Charge	—	—	3.8	nC	V _{DS} =-48V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	5.1		V _{GS} =-10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	11	—	ns	V _{DD} =-30V I _D =-6.7A R _G =24Ω R _D =4.0Ω See Figure 10 ④
t _r	Rise Time	—	63	—		
t _{d(off)}	Turn-Off Delay Time	—	10	—		
t _f	Fall Time	—	31	—		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	270	—	pF	V _{GS} =0V V _{DS} =-25V f=1.0MHz See Figure 5
C _{oss}	Output Capacitance	—	170	—		
C _{rss}	Reverse Transfer Capacitance	—	31	—		



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-6.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-27		
V _{SD}	Diode Forward Voltage	—	—	-5.5	V	T _J =25°C, I _S =-6.7A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	80	160	ns	T _J =25°C, I _F =-6.7A
Q _{rr}	Reverse Recovery Charge	—	0.096	0.19	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=-25V, starting T_J=25°C, L=3.6mH R_G=25Ω, I_{AS}=-6.7A (See Figure 12)
- ③ I_{SD}≤-6.7A, di/dt≤90A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤175°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

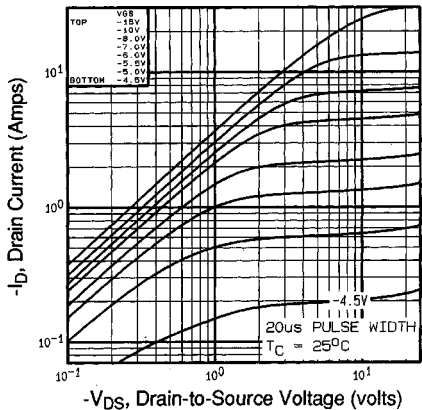


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

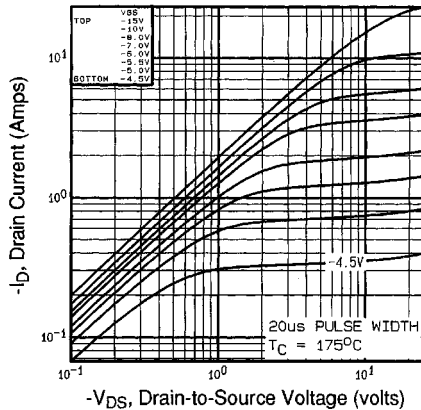


Fig 2. Typical Output Characteristics,
 $T_C=175^\circ\text{C}$

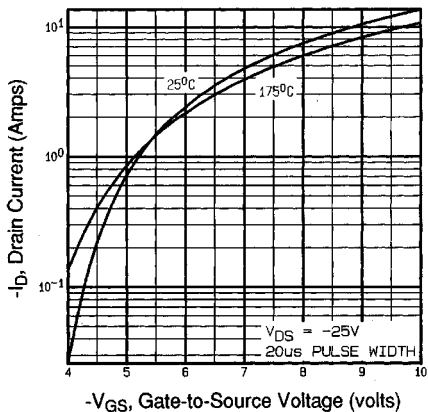


Fig 3. Typical Transfer Characteristics

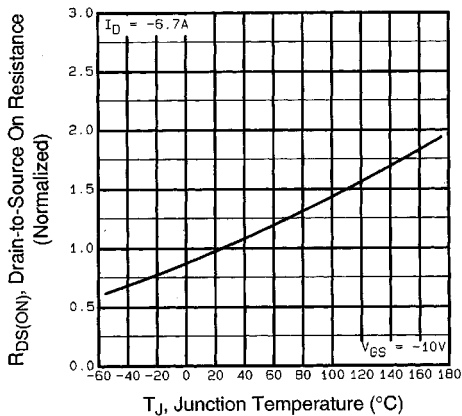


Fig 4. Normalized On-Resistance
Vs. Temperature

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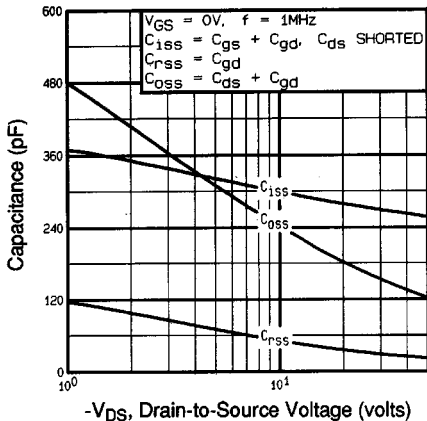


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

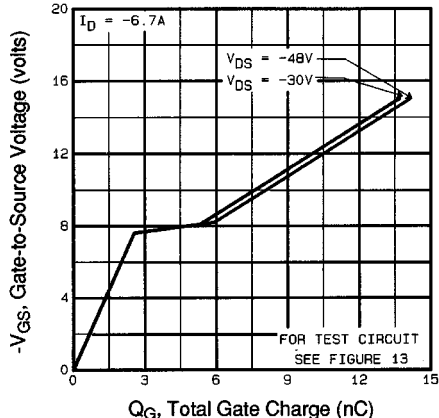


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

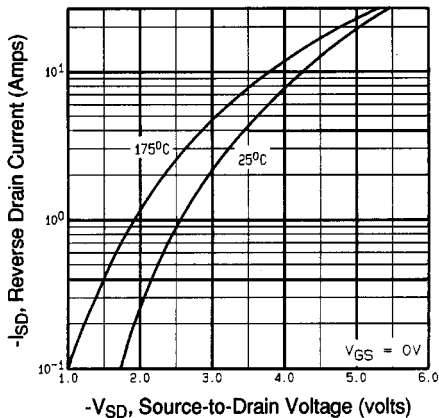


Fig 7. Typical Source-Drain Diode Forward Voltage

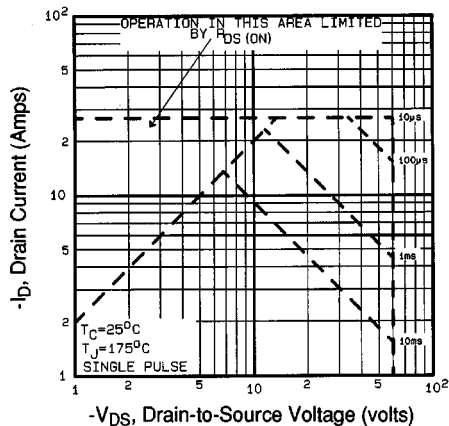


Fig 8. Maximum Safe Operating Area

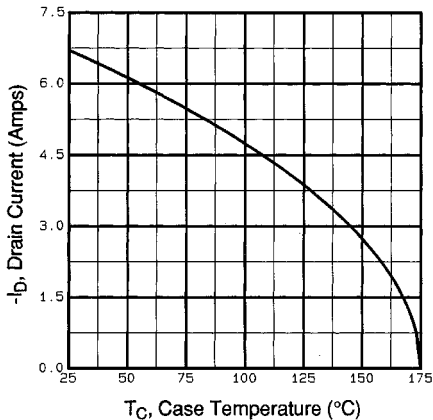


Fig 9. Maximum Drain Current Vs. Case Temperature

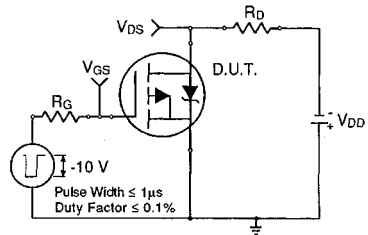


Fig 10a. Switching Time Test Circuit

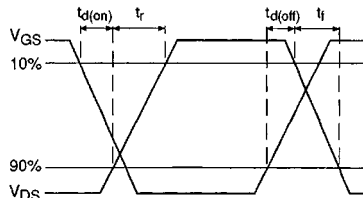


Fig 10b. Switching Time Waveforms

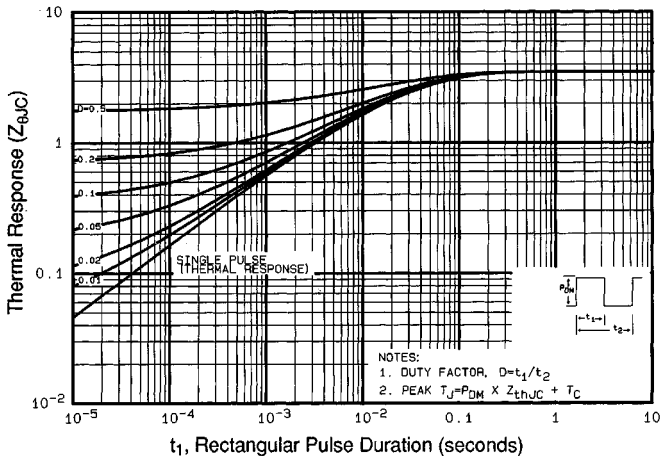


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

DATA SHEETS

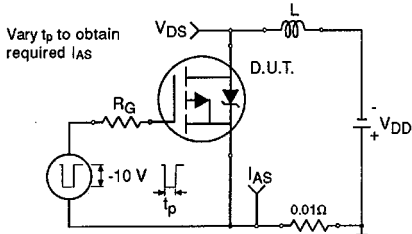


Fig 12a. Unclamped Inductive Test Circuit

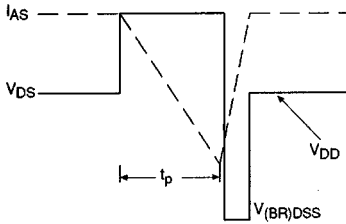


Fig 12b. Unclamped Inductive Waveforms

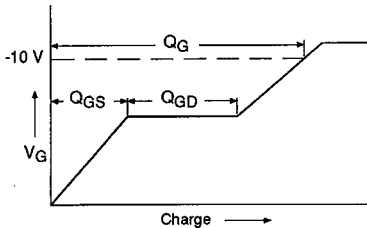


Fig 13a. Basic Gate Charge Waveform

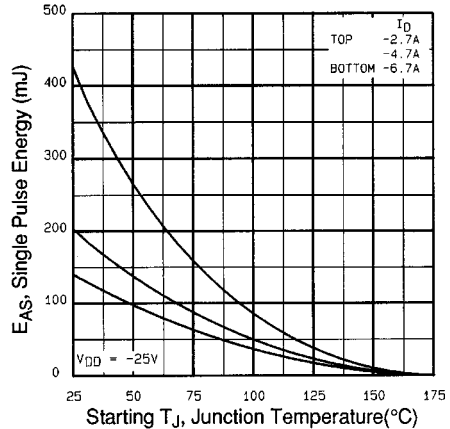


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

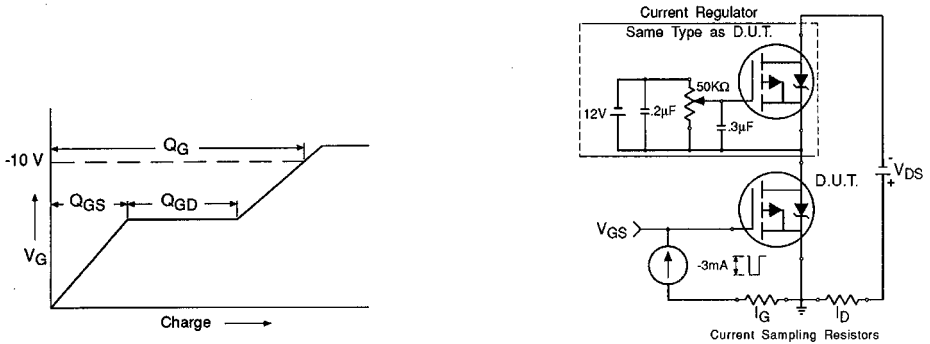


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1506

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525