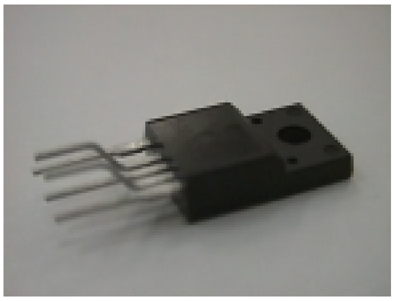
S P S

The SPS product family is specially designed for an off-line SMPS with minimal external components. The SPS consist of high voltage power SenseFET and current mode PWM IC.
Included PWM controller features integrated fixed oscillator, under voltage lock out, leading edge blanking, optimized gate turn-on/turn-off driver, thermal shut down protection, over voltage protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry. Compared to discrete MOSFET and controller or RCC switching converter solution, a SPS can reduce total component count, design size, and weight and at the same time increase efficiency, productivity, and system reliability. It has a basic platform well suited for cost-effective design in Quasi-Resonant Converter as C-TV power supply.

TO-220F-5L



1. Drain 2. GND 3. V_{CC} 4. FB 5. Sync

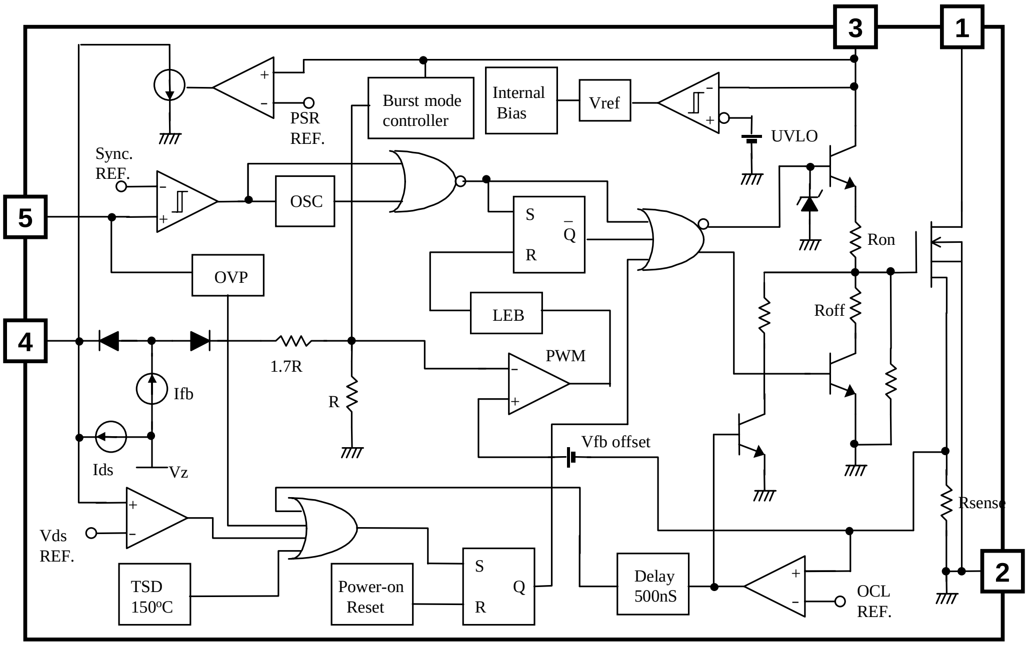
FEATURES

- Quasi Resonant Converter Controller
- Internal Burst mode Controller for Stand-by mode
- Pulse by pulse current limiting
- Over current Latch protection
- Over voltage protection (Vsync: Min. 11V)
- Internal thermal shutdown function
- Under voltage lockout
- Internal high voltage sense FET
- Auto-restart mode

ORDERING INFORMATION

Device	Package	Topr (°C)
KA5Q0765RT	TO-220F-5L	–25°C to +85°C

BLOCK DIAGRAM



FAIRCHILD SEMICONDUCTOR TM

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Drain-source (GND) voltage [(1)]	V_{DSS}	650	V
Drain-Gate voltage (R_{GS}=1MΩ)	V_{DGR}	650	V
Gate-source (GND) voltage	V_{GS}	±30	V
Drain current pulsed [(2)]	I_{DM}	28.0	A_{DC}
Single pulsed avalanche energy [(3)]	E_{AS}	570	mJ
Avalanche current [(4)]	I_{AS}	20	A
Continuous drain current (T_C=25°C)	I_D	7.0	A_{DC}
Continuous drain current (T_C=100°C)	I_D	5.6	A_{DC}
Supply voltage	V_{CC}	30	V
Analog input voltage range	V_{FB}	–0.3 to V_{SD}	V
Total power dissipation	P_D (wt H/S)	135	W
	Derating	1.1	W/°C
Operating temperature	T_{OPR}	–25 to +85	°C
Storage temperature	T_{STG}	–55 to +150	°C

NOTES:

1. Tj=25°C to 150°C
2. Repetitive rating: Pulse width limited by maximum junction temperature
3. L=24mH, starting Tj=25°C
4. L=13uH, starting Tj=25°C

ELECTRICAL CHARACTERISTICS (SFET part)

(Ta=25°C unless otherwise specified)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=50μA	650	–	–	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=Max., Rating, V_{GS}=0V	–	–	200	μA
		V_{DS}=0.8Max., Rating, V_{GS}=0V, T_C=125°C	–	–	500	μA
Static drain-source on resistance (note)	$R_{DS(ON)}$	V_{GS}=10V, I_D=4.0A	–	1.25	1.6	Ω
Forward transconductance (note)	gfs	V_{DS}=15V, I_D=4.0A	3.0	–	–	S
Input capacitance	Ciss	V_{GS}=0V, V_{DS}=25V, f=1MHz	–	1600	–	pF
Output capacitance	Coss		–	310	–	
Reverse transfer capacitance	Crss		–	120	–	
Turn on delay time	td(on)	V_{DD}=0.5BV_{DSS}, I_D=7.0A (MOSFET switching time are essentially independent of operating temperature)	–	25	–	nS
Rise time	tr		–	55	–	
Turn off delay time	td(off)		–	80	–	
Fall time	tf		–	50	–	
Total gate charge (gate-source+gate-drain)	Qg	V_{GS}=10V, I_D=7.0A, V_{DS}=0.5BV_{DSS} (MOSFET switching time are essentially independent of operating temperature)	–	–	72	nC
Gate-source charge	Qgs		–	9.3	–	
Gate-drain (Miller) charge	Qgd		–	29.3	–	

NOTE: Pulse test: Pulse width ≤ 300μS, duty cycle ≤ 2%

ELECTRICAL CHARACTERISTICS (Control part)

(Ta=25°C unless otherwise specified)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
SENSE FET SECTION						
Drain to PKG Breakdown voltage	BVpkg	60Hz AC, Ta=25°C	3500	–	–	V
Drain to Source Breakdown voltage	BVdss	Vdrain=650V, Ta=25°C	650	–	–	V
Drain to Source Leakage current	Idss	Vdrain=650V, Ta=25°C	–	–	200	μA
OSCILLATOR SECTION						
Initial Frequency	F_{OSC}	–	18	20	22	KHz
Voltage Stability	F_{STABLE}	$12 \leq V_{CC} \leq 23V$	0	1	3	%
Temperature Stability note 2	ΔF_{OSC}	-25°C≤Ta≤85°C	0	±5	±10	%
Maximum Duty Cycle	D_{MAX}	–	92	95	98	%
Minimum Duty Cycle	D_{MIN}	–	–	–	0	%
UVLO SECTION						
Start Threshold Voltage	V_{START}	V_{FB}=GND	14	15	16	V
Stop Threshold Voltage	VSTOP	V_{FB}=GND	8	9	10	V
FEEDBACK SECTION						
Feedback Source Current	I_{FB}	V_{FB}=GND	0.7	0.9	1.1	mA
Shotdown Feedback Voltage	V_{SD}	Vfb≥6.9V	6.9	7.5	8.1	V
Shutdown Delay Current	I_{DELAY}	V_{FB}=5V	4	5	6	μA
PROTECTION SECTION						
Over Current Protection	V_{OVP}	Vsync≥11V	11	12	13	V
Over Current Latch Voltage note 2	V_{OCL}	–	0.9	1.0	1.1	V
Thermal shutdown Temp.	TSD	–	140	160	–	°C
SYNC SECTION						
Normal Sync High Threshold Voltage	V_{NSH}	V_{CC}=16V, Vfb=5V	4.0	4.6	5.2	V
Normal Sync Low Threshold Voltage	V_{NSL}	V_{CC}=16V, Vfb=5V	2.3	2.6	2.9	V
Burst High Threshold Voltage	V_{BSH}	V_{CC}=10.5V, Vfb=0V	3.2	3.6	4.0	V
Burst Low Threshold Voltage	V_{BSL}	V_{CC}=10.5V, Vfb=0V	1.1	1.3	1.5	V

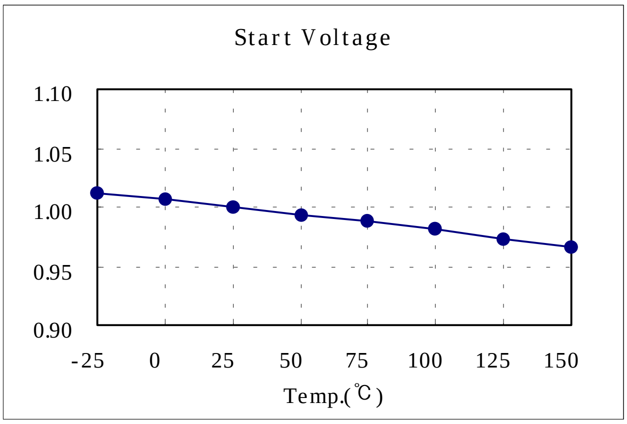
ELECTRICAL CHARACTERISTICS (Continued)

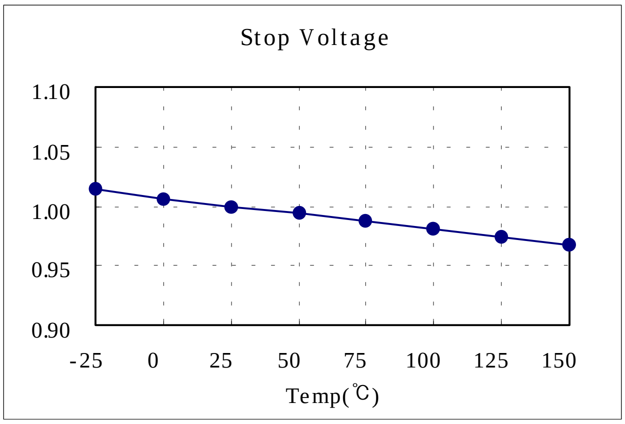
(Ta=25°C unless otherwise specified)

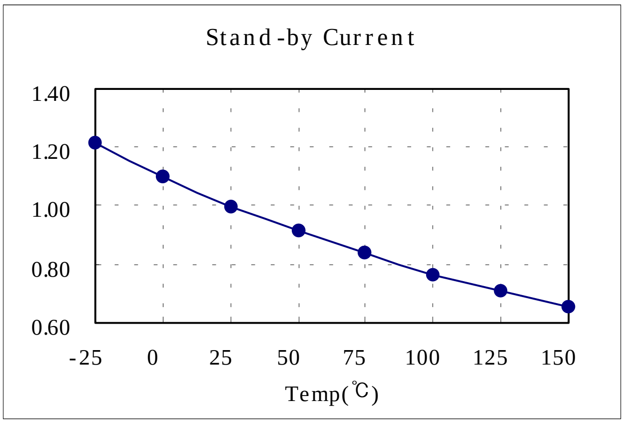
Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
BURST MODE SECTION						
Burst mode Low Threshold Voltage	V_{BURL}	Vfb=0V	10.4	11.0	11.6	V
Burst mode High Threshold Voltage	V_{BURH}	Vfb=0V	11.4	12.0	12.6	V
Burst mode Enable Feedback voltage	V_{BEN}	V_{CC}=10.5V	0.7	1.0	1.3	V
Burst mode Peak Current Limit	I_{BU_PK}	V_{CC}=10.5V	0.65	0.85	1.0	V
PRIMARY SIDE REGULATION SECTION						
Primary Regulation Threshold Voltage	V_{PR}	Ifb=700µA, Vfb=4V	32.0	32.5	33.0	V
Primary Regulation Thansconductance	G_{PR}	–	2.0	2.6	–	mA/V
CURRENT LIMIT (SELF-PROTECTION) SECTION						
Peak Current Limit [note 3]	I_{PK}	–	4.4	5.0	5.6	A
START UP CURRENT						
Start up Current	I_{START}	Vfb=GND, V_{CC}=14V	–	0.1	0.2	mA
Operatig Supply Current [noet 1]	I_{OP}	Vfb=GND, V_{CC}=16V	–	10	18	mA
	$I_{OP(MIN)}$	Vfb=GND, V_{CC}=12V				
	$I_{OP(MAX)}$	Vfb=GND, V_{CC}=28V				

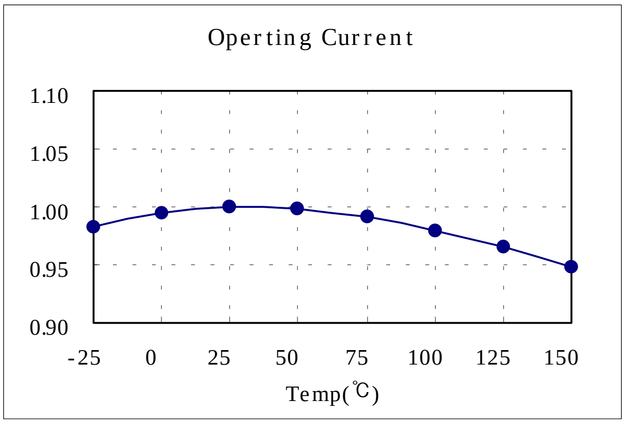
NOTE:
1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. These parameters indicate inductor current

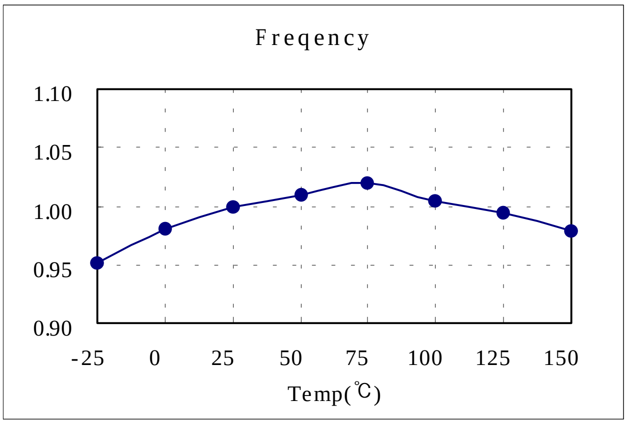
TYPICAL PERFORMANCE CHARACTERISTICS

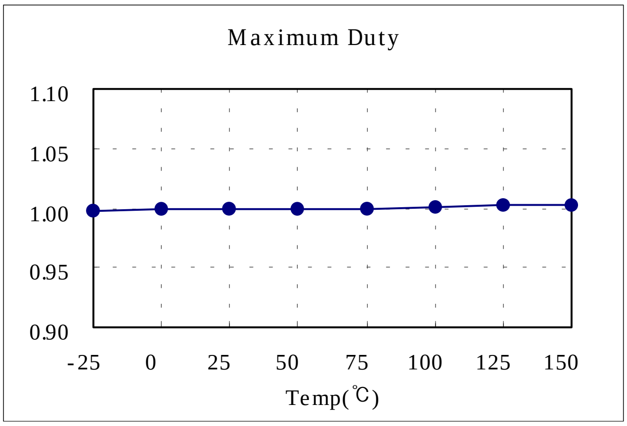












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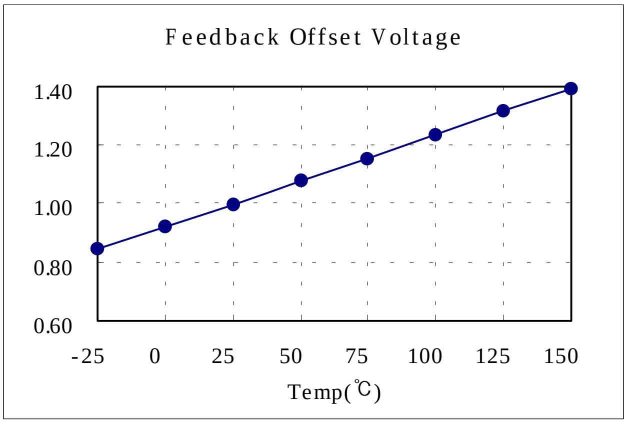

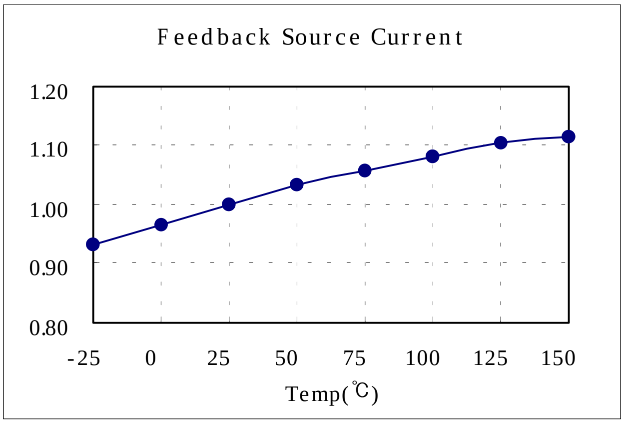

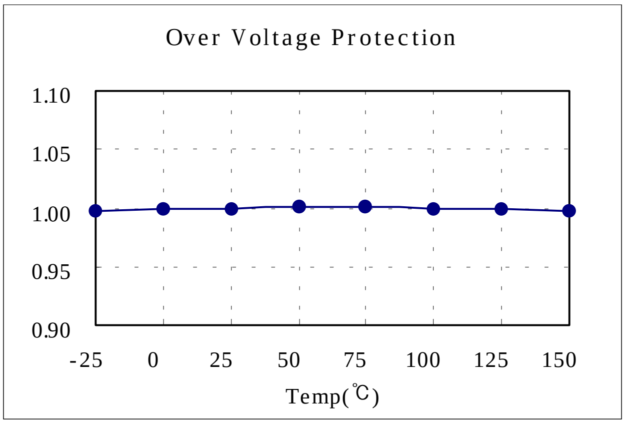

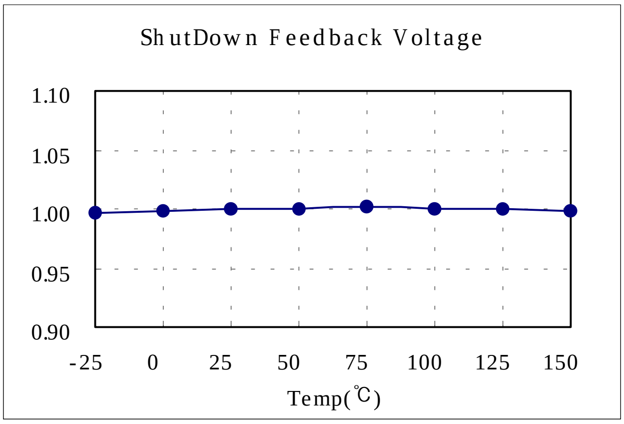

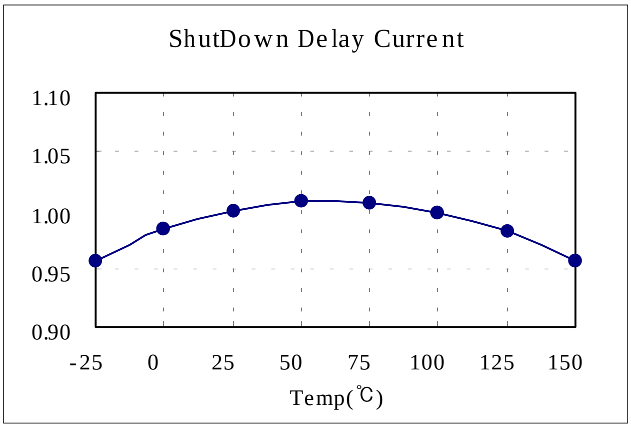

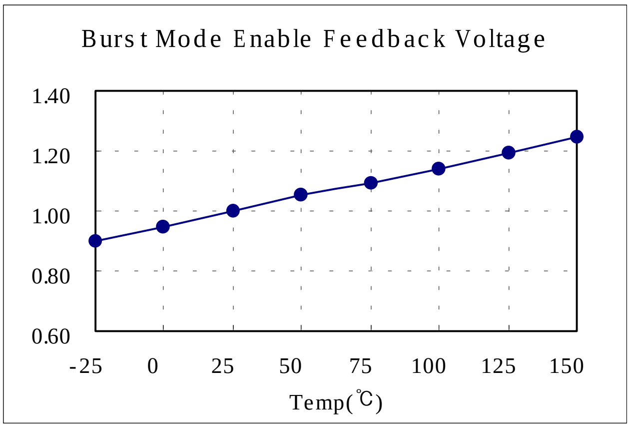

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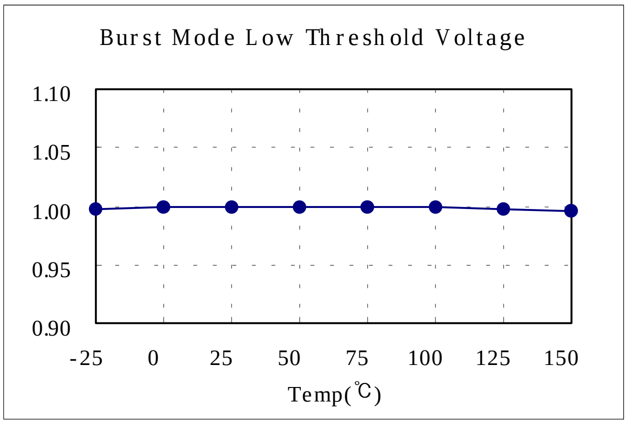

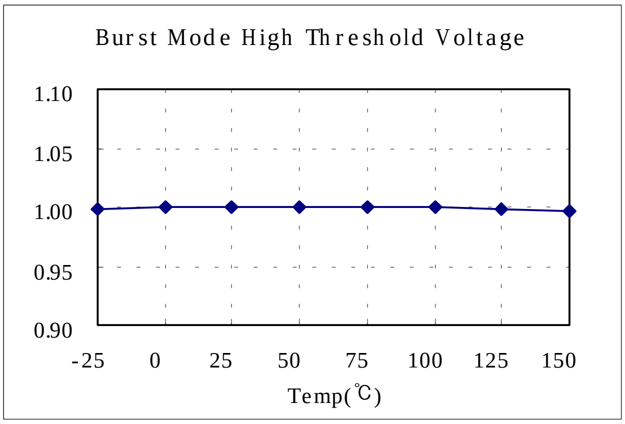

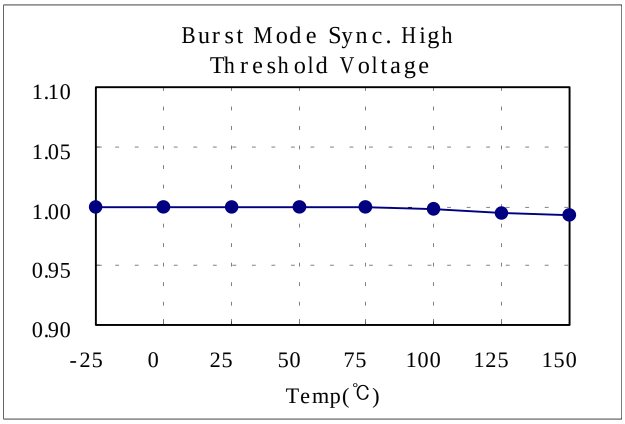

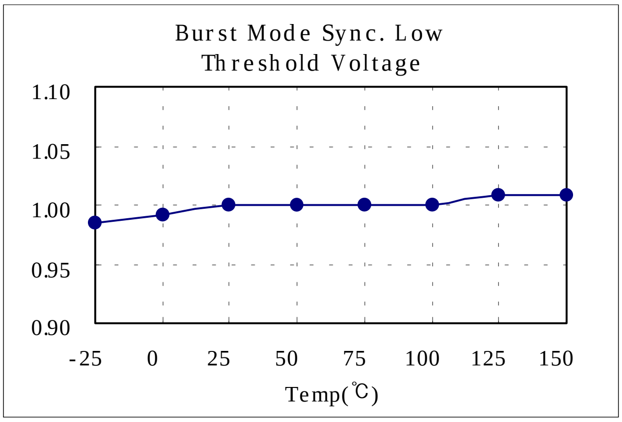

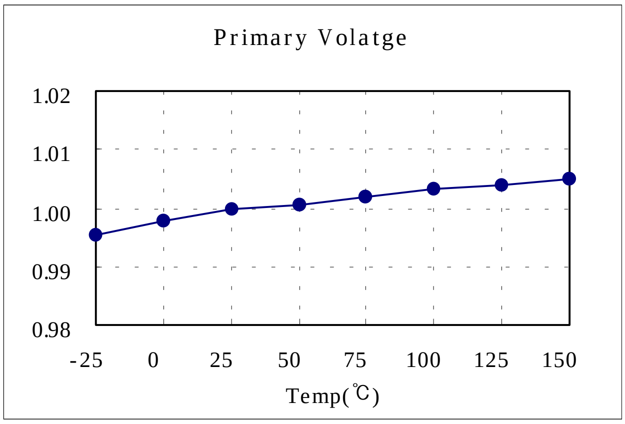

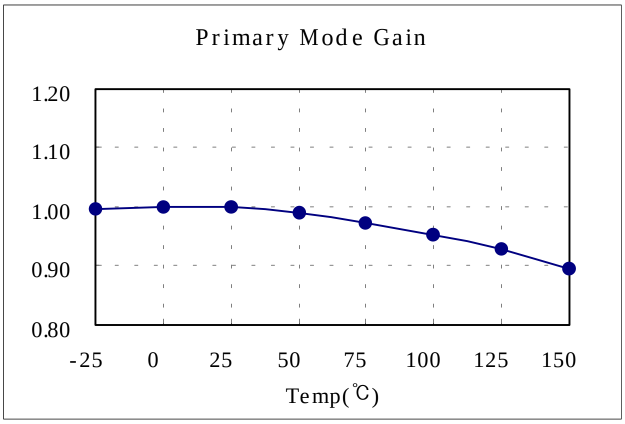

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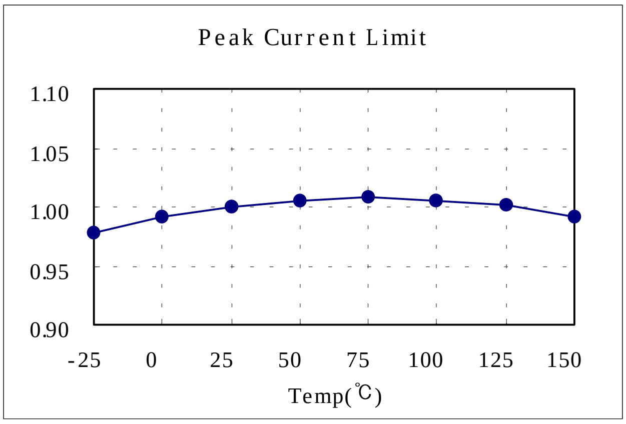

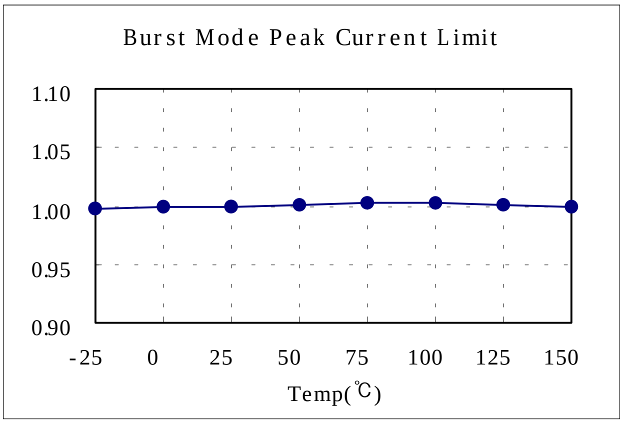

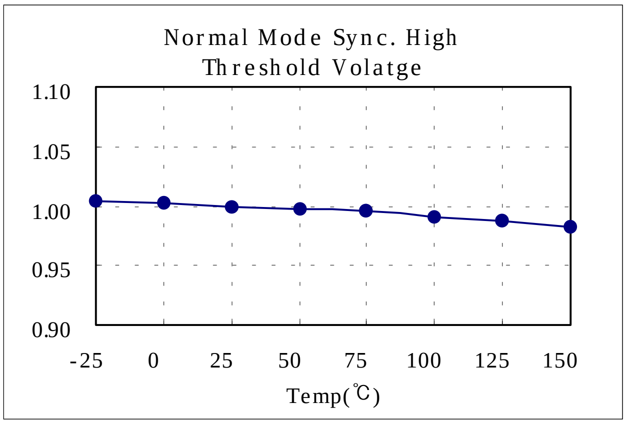

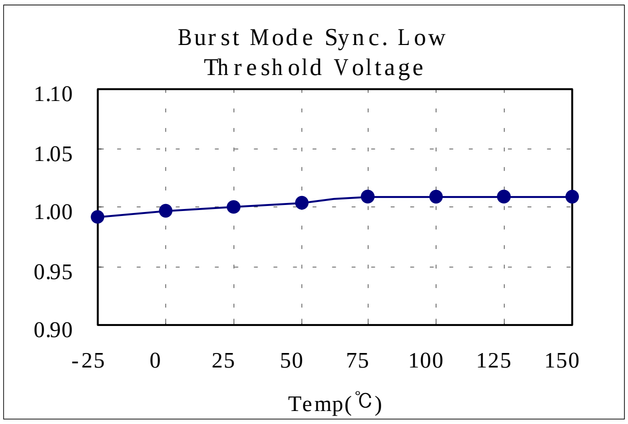

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