Ordering number: EN5205A

Monolithic Linear IC

LA4820M

Monaural Speaker/Stereo Headphone Power Amplifier

Overview

The LA4820M compound power IC is designed for portable information processing equipment, such as electronic book players and personal notebook computers, and provides on chip headphone stereo amplifier and monaural speaker amplifier functions required of such devices. This system IC also provides on chip a power-saving headphone jack plug-in/out detection function, which automatically switches the amplifiers, and an optimum volume level controller.

Features

- Power-saving headphone jack plug-in/out detection function on chip that electronically switches between the stereo headphone amplifier and the monaural BTL amplifier according to jack plug-in/out.
- The monaural amplifier has, as output control functions, a built-in output limiter that permits adjustment in accordance with the speaker impedance and a non-clipping circuit that outputs a sine wave suited to the output D range, while the headphone amplifier has a built-in user-friendly PVSS (Peak Volume Select System).
- On-chip ripple filter with a high ripple rejection ratio in order to reduce power line noise.
- Less external components needed thanks to system and circuit technology, and low-capacitance design (22 µF or less) allowing support for chip components.

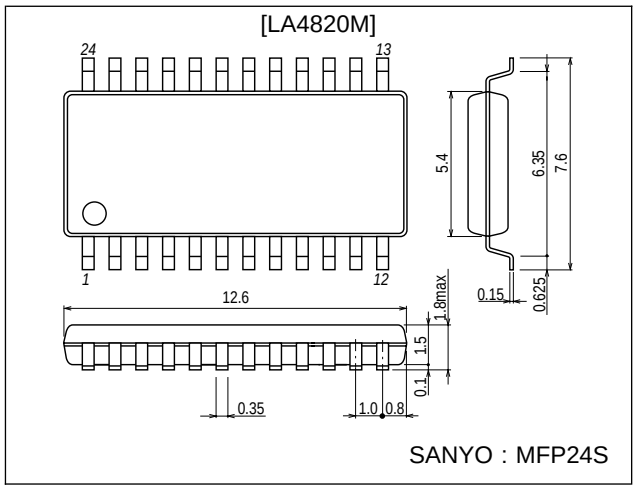
Functions

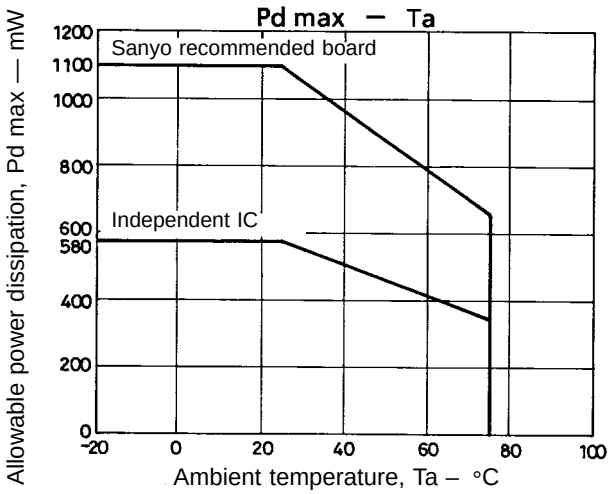
- Monaural BTL power amplifier
- Headphone OCL power amplifier (16 Ω) × 2
- Output control functions:
  - Headphone power: PVSS
  - Monaural power: Non-clipping circuit and output limiter
- Headphone jack plug-in/out detection function (monaural amplifier/headphone amplifier switching)
- Ripple filter
- Power mute switch
- Common amplifier on/off switching

Package Dimensions

unit : mm

3112-MFP24S





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Specifications

Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}1,2 max		8.0	V
Allowable power dissipation	Pd max		580	mW
		With Sanyo evaluation board (84.2 × 92.6 mm^2)	1.1	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +150	°C

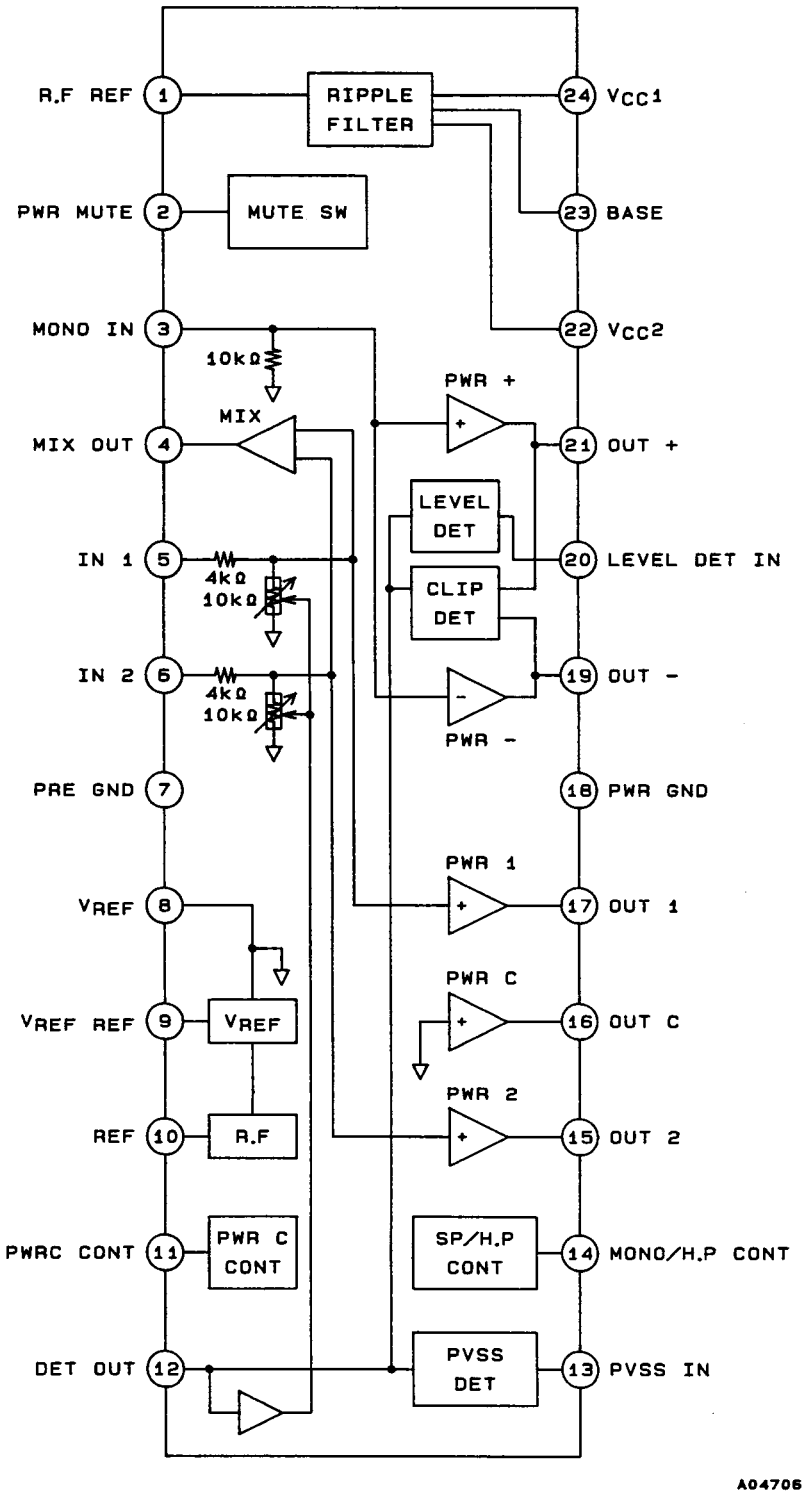
Operating Conditions at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}1		6.0	V
Operating voltage range	V_{CC}1 op		2.5 to 7.2	V
	V_{CC}2 op		2.0 to 7.2	V

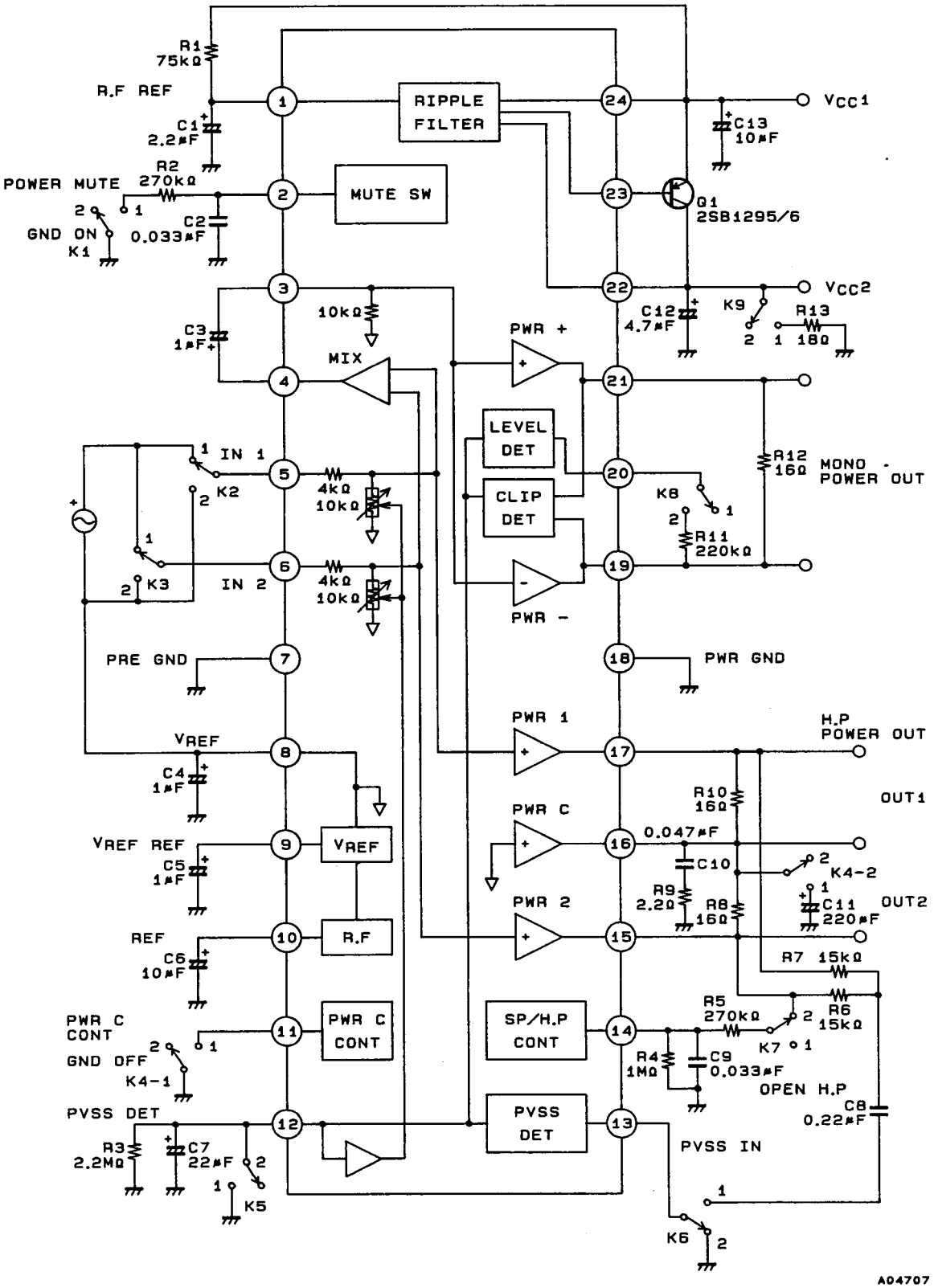
Operating Characteristics at Ta = 25 °C, V_{CC}1 = 6.0 V, fi = 1 kHz, 0.775 V = 0 dBm, R_L = 16 Ω: monaural amplifier, R_L = 16 Ω : headphone amplifier

Parameter	Symbol	Conditions	min	typ	max	Unit
[Total]						
Quiescent current	I_{CCO}1	Rg = 0 kΩ, monaural amplifier	7.0	11.5	21.0	mA
	I_{CCO}2	Rg = 0 kΩ, headphone amplifier	5.5	9.0	14.0	mA
	I_{CCO}3	Headphone common amplifier off	4.0	6.3	10.0	mA
Input resistance	Ri		10	13	16	kΩ
[Monaural Amplifier]						
Output power	P_O1	THD = 10%, pin 12 connected to GND	500	760		mW
Voltage gain (closed)	VG1	V_O = 0 dBm	36.0	39.0	42.0	dB
Total harmonic distortion	THD1	P_O = 100 mW		0.1	1.0	%
Output noise voltage	V_{NO} 1	Rg = 0 Ω, BPF = 20 to 20 kHz		170	300	μV
Ripple rejection ratio	Rr1	Rg = 0 Ω, Vr = –10 dBm, fr = 100 Hz	60	77		dB
DC offset voltage	V_{OFF}1	Between pin 19 and pin 21	–80	0	+80	mV
[Non-clipping + Monaural Amplifier]						
Output power	P_O2	Vi = 0 dBm	300	450		mW
Total harmonic distortion	THD2	Vi = 0 dBM		1.2	2.0	%
[Output Limiter + Monaural Amplifier]						
Output power	P_O3	Vi = 0 dBm, output limiter input resistance 220 Ω	120	200	300	mW
Total harmonic distortion	THD3	Vi = 0 dBm, output limiter input resistance 220 Ω		0.5	1.2	%
[Headphone Amplifier]						
Output power	P_O4	THD = 10%	30	120		mW
Voltage gain (closed)	VG2	V_O = –10 dBm	15.3	18.3	21.3	dB
Total harmonic distortion	THD4	P_O = 1 mW		0.1	0.5	%
Interchannel crosstalk	CT	VO = –5 dBm, Rg = 0 Ω	30	39		dB
Output noise voltage	V_{NO}2	Rg = 0 Ω, BPF = 20 to 20 kHz		16	35	μV
Ripple rejection ratio	Rr2	Rg = 0 Ω, Vr = –10 dBm, fr = 100 Hz	70	92		dB
DC offset voltage	V_{OFF}2	Between pin 15 and pin 16, and pin 16 and pin 17	–40	0	+40	mV
[PVSS + Headphone Amplifier]						
PVSS voltage	V_O	Vi = –30 dBm, PVSS2	–39	–36	–33	dBm
PVSS distortion factor	THD5	Vi = –30 dBm, PVSS2		0.25	1.6	%
PVSS start input	V_{OPi}	PVSS2	–59	–55	–51	dBm
PVSS width	W_{PVSS}	Input width from the starting point to the point where the output is +4 dB, PVSS ON	28	35		dB
[Ripple Filter]						
Output voltage	V_{RF}	I_{RF} = 300 mA, 2SB1295 h_{FE}6 used	5.30	5.49	5.70	V
Ripple rejection ratio	Rr3	Vr = –10 dBm, fr = 100 Hz, I_{RF} = 300 mA, 2SB1295 h_{FE}6 used	30	34		dB

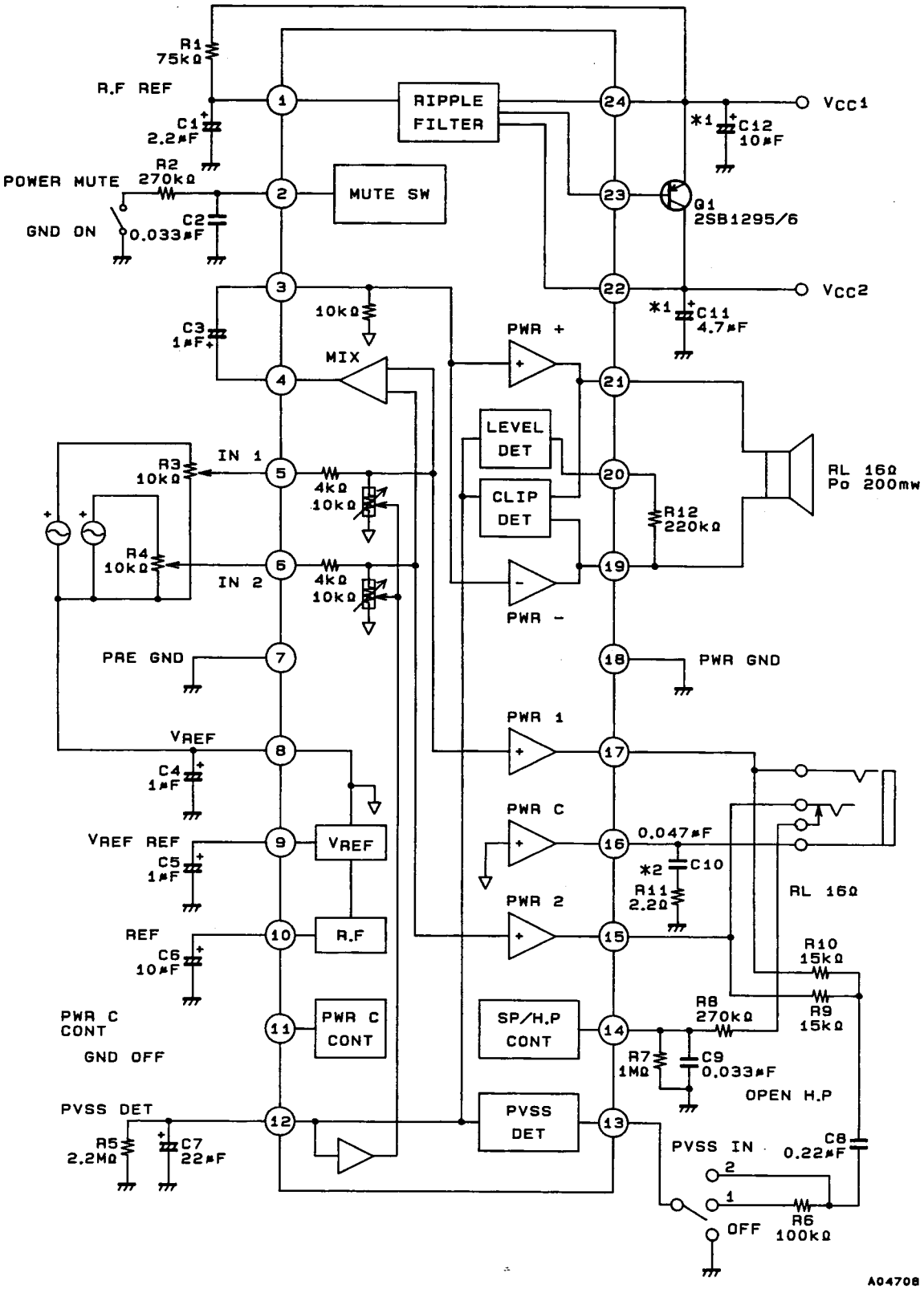
Block Diagram



Test Circuit Diagram



Sample Application Circuit 1

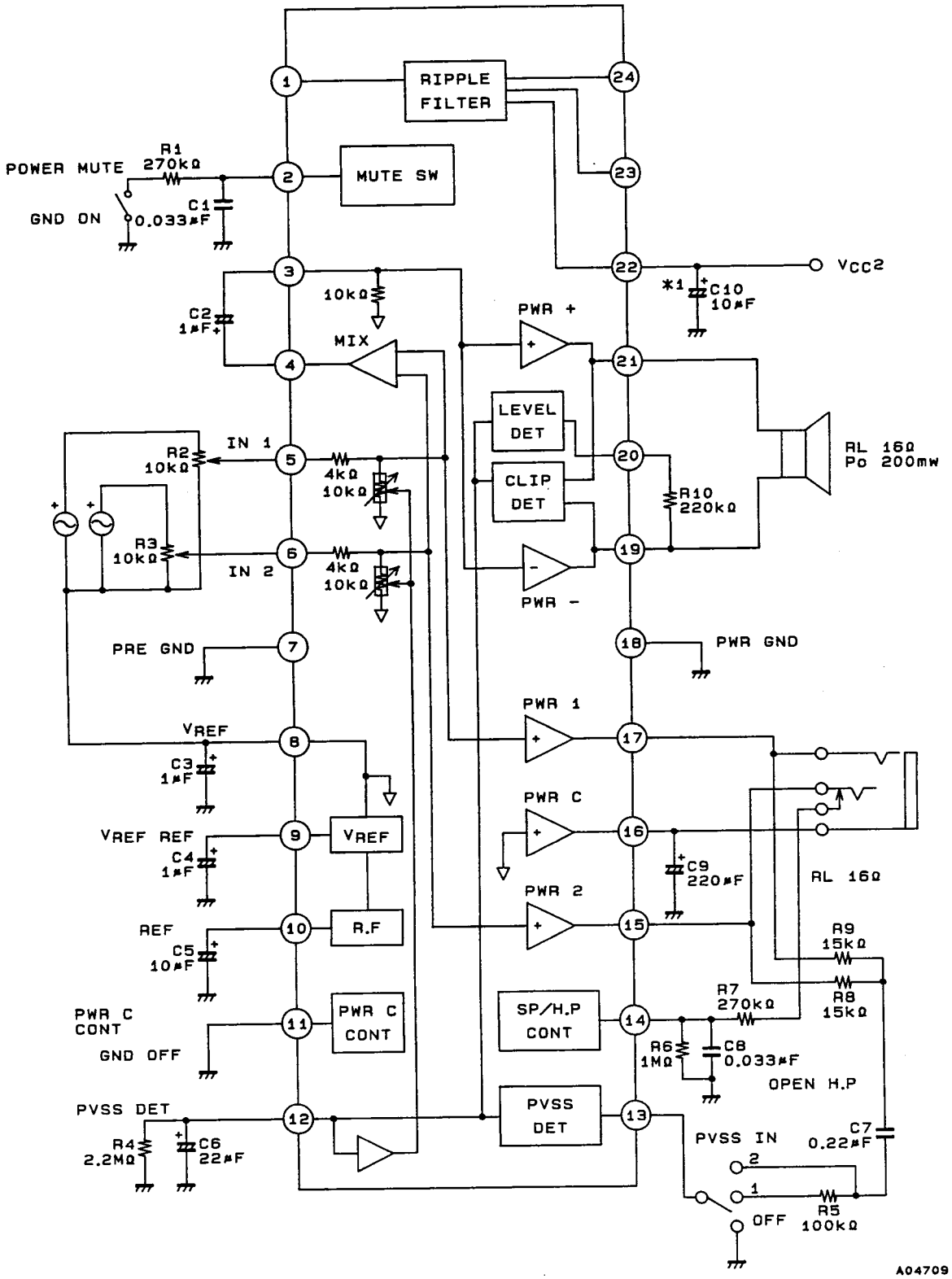


*1 A Tantalum capacitor is recommended.

*2 A polyester film or ceramic capacitor (of which capacitance specified must be independent of temperature changes) is recommended.

Sample Application Circuit 2

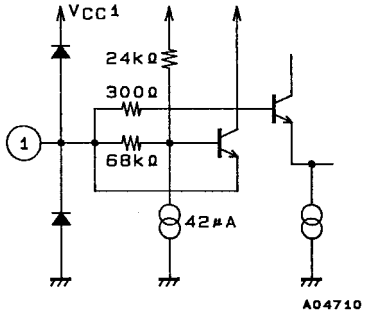
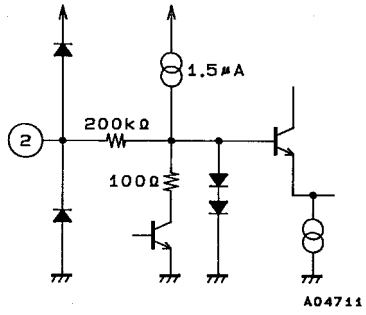
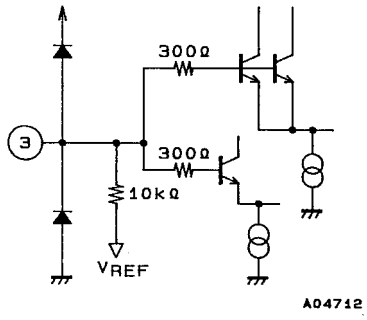
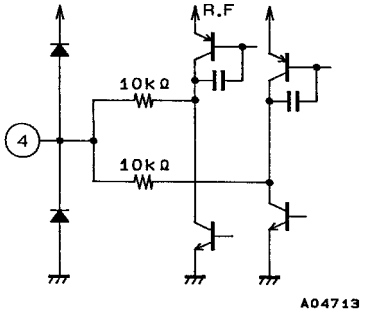
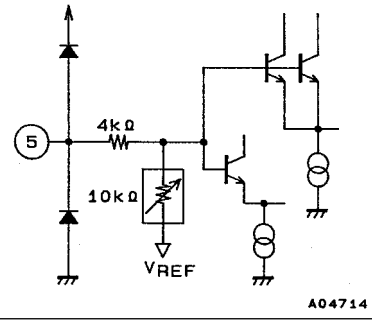
(When neither ripple filter nor common amplifier is used.)



*1 A Tantalum capacitor is recommended.

Pin Description

* When the pin voltage is for $V_{CC}1$ = 6.0 V

Pin No.	Pin name	Pin voltage [V]	Internal equivalent circuit	Remarks
1	R.F REF (Ripple Filter)	5.5		• LPF pin for ripple filter reference bias. • Ripple rejection ratio can be adjusted through an external capacitor. • Open when no ripple filter is needed.
2	PWR MUTE	1.2		• Power mute is turned on when pin 2 is pulled down. • Turns on and off supply of constant current to the power block.
3	MONO IN	2.8		• BTL power input pin. • Input resistance 9 kΩ.
4	MIX OUT	2.8		• IN1 and IN2 addition output pin. • Output resistance 5 kΩ.
5 6	IN1 IN2	2.8		• Power input pins. • Input resistance can be varied between 14 kΩ and 4 kΩ by ALC.

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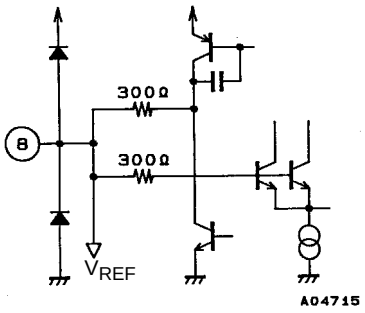
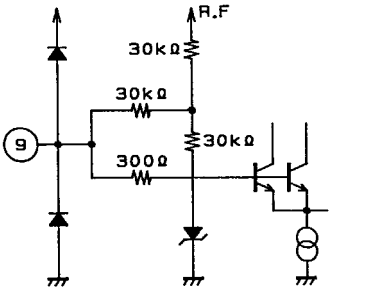
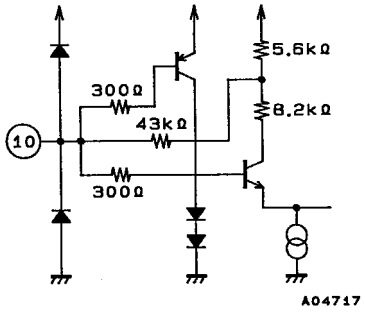
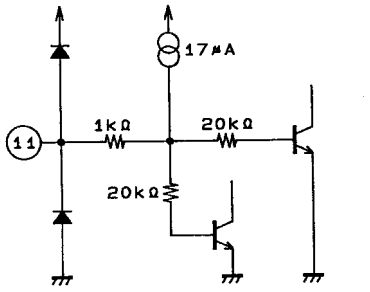
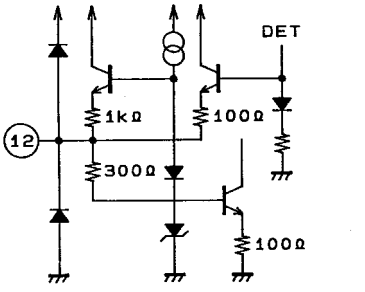
Pin No.	Pin Name	Pin Voltage	Internal equivalent circuit	Remarks
7	PRE GND			• Connects small-signal block to GND.
8	V_{REF}	2.8		• Virtual ground bias pin. • Impedance is lowered by V_{REF} amplifier. (ro = 10 Ω or less) • V_{REF} voltage is determined by the following formula: $V_{REF} = \frac{V_{CC}2 \text{ voltage (pin 22)}}{2}$ (V)
9	V_{REF}REF	2.8		• LPF pin for V_{REF} amplifier reference bias.
10	REF	5.1		• LPF pin for internal ripple filter reference bias. • Voltage of $V_{CC}2$ – 0.4 V.
11	PWRC CONT	0.8		• H·P Power is such that the common amplifier turns off and the output common capacitor mode is entered when pin 11 is pulled down.
12	DET OUT	0.5 to 1.0		• PVSS, output limiter, non-clipping circuit ALC rectification pin. • The attack and recovery time are determined by the external capacitance and resistance.

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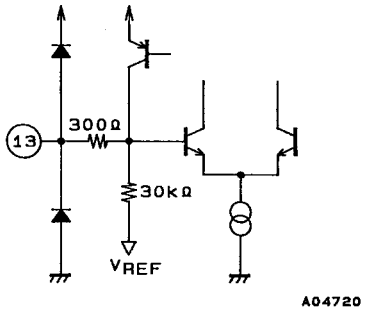
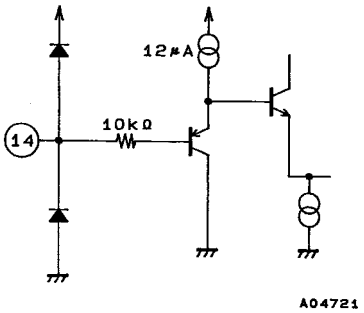
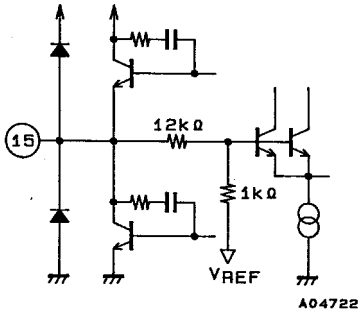
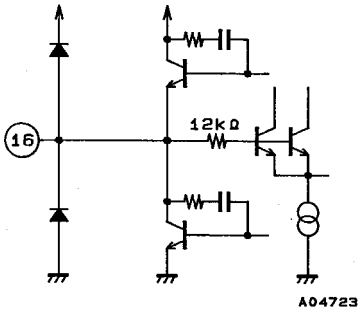
Pin No.	Pin Name	Pin Voltage	Internal equivalent circuit	Remarks
13	PVSS IN	2.8		• PVSS detection input pin. • PVSS turns off when pulled down or left open.
14	MONO/H·P CONT	0.6		• Switches to H·P when pin 14 is pulled down (connected to GND through 1 MΩ). • The external capacitance and resistance is for mode switching smoothing.
15 17	OUT2 OUT1	2.3		• H·P Power output pin.
16	OUTC	2.3		• H·P Power COMMON pin. • Turns off when pin 11 is pulled down.
18	PWR GND			• Connects power amplifier output block to GND.

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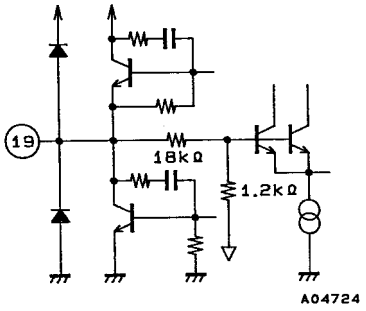
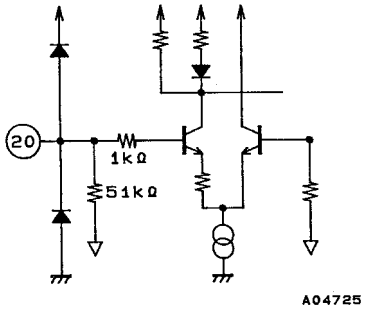
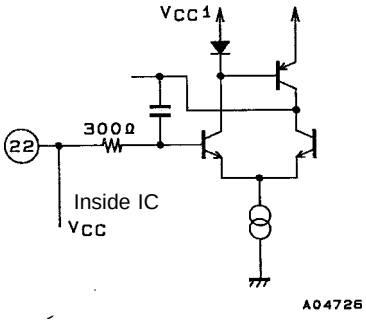
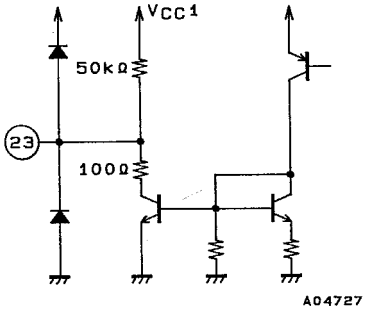
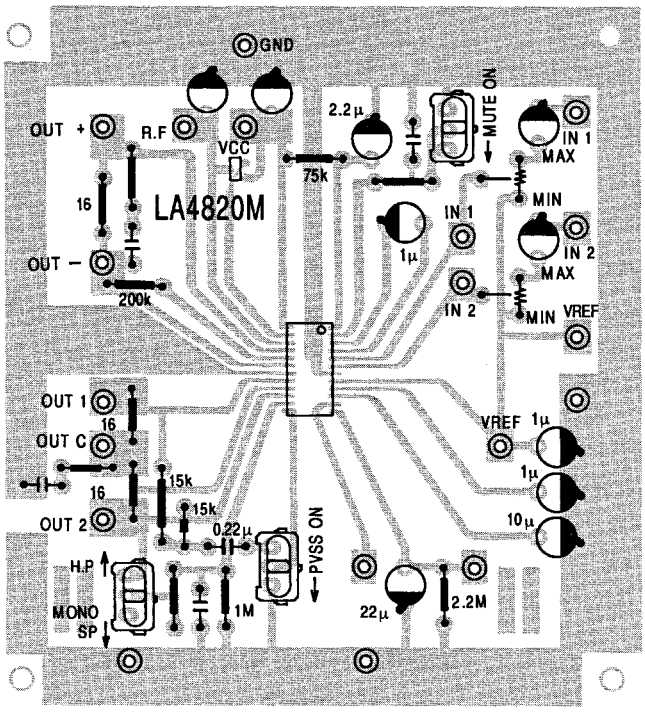
Pin No.	Pin Name	Pin Voltage	Internal equivalent circuit	Remarks
19 21	OUT– OUT+	2.3		• MONO Power output pin. • BTL operation provides phase inversion and amplitude.
20	LEVEL DET IN	2.9		• MONO Power output level detection input pin. • Output limiter level can be varied by external resistance.
22	$V_{CC}2$	5.5		• Ripple filter output pin. • Power supply pin when no ripple filter is used. • Amplifier block V_{CC} pin.
23	BASE	5.4		• Tr base grounding pin for ripple filter. • Left open when no ripple filter is needed.
24	$V_{CC}1$	6.0		• Ripple filter V_{CC} pin. • Left open when no ripple filter is needed.

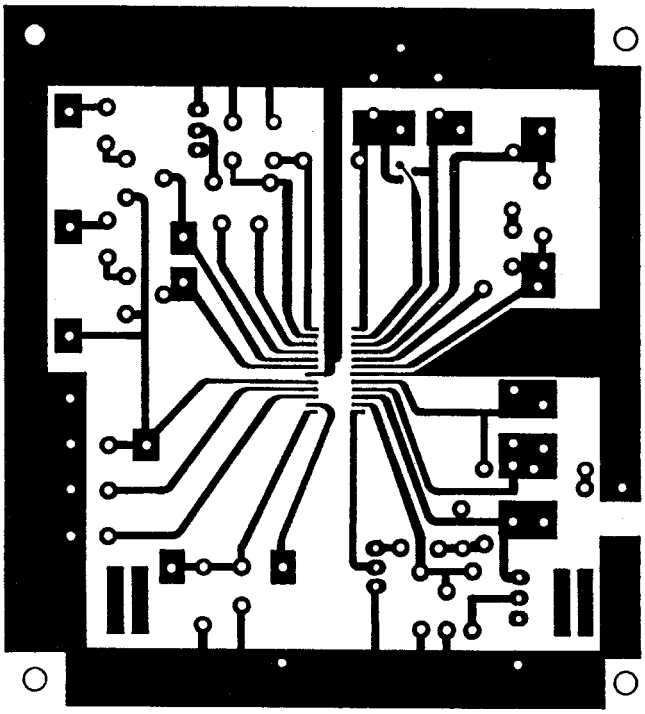
Sanyo Evaluation Board Pattern



Surface
(silk side)

Tone block
(copper foiled side)

Unit (resistance: Ω, capacitance: F)



Copper foiled side

Description of External Components

(Refer to Sample Application Circuit No. 1 for device numbers.)

- R1 (∞ to 40 kΩ): Resistor for ripple filter reference bias. Not needed when no ripple filter is used.

Resistance	$V_{CC}1 - V_{CC}2$
None	1.17 V
150 kΩ	0.73 V
75 kΩ	0.52 V
40 kΩ	0.35 V

The V_{CE} voltage ($V_{CC}1 - V_{CC}2$) of the Tr can be adjusted by changing the resistance value.

- R2 (270 kΩ to 100 kΩ): Resistor for smoothing (shock noise prevention) when power mute is turned on.
- R3, R4 (30 kΩ to 10 kΩ): Volume.
- R5 (5.1 MΩ to 510 kΩ): Resistor for PVSS, output limiter, and non-clipping circuit recovery.
- R6 (510 kΩ to 0 Ω): PVSS output level variable resistor. Not needed when using no PVSS.

Resistance	PVSS V_O
None	–36 dBm
100 kΩ	–25 dBm
300 kΩ	–18 dBm

- R7 (1 MΩ): Pull-down (discharging) resistor for SP/H·P switching.
- R8 (270 kΩ): Pull-up (charging) resistor for SP/H·P switching.
- R9, R10 (510 kΩ to 10 kΩ): H·P output mixing resistors for PVSS. Not needed when using no PVSS.
- R11 (2.2 Ω): Resistor for blocking common amplifier oscillation. Not needed when the common amplifier is turned off.
- R12 (510 kΩ to 0 Ω): Output limiter level variable resistor. Not needed when no output limiter is used.

Resistance	P_O
400 kΩ	400 mW
300 kΩ	290 mW
220 kΩ	200 mW
100 kΩ	110 mW
0	43 mW

The limiter level can be adjusted by changing the resistance value.

- Q1: Ripple filter output Tr (2SB1295 $h_{FE}6$ recommended).
  Not needed when using no ripple filter.
- C1 (4.7 µF to 1.0 µF): LPF capacitor for the ripple filter reference bias. Low-region ripple rejection ratio can be varied by changing the capacitance. Not needed when using no ripple filter.

Capacitance	100 Hz SVRR	1 kHz SVRR
4.7 µF	40 dB	60 dB
2.2 µF	34 dB	54 dB
1.0 µF	28 dB	48 dB

- C2 (0.1 µF to 0.01 µF): Capacitor for smoothing (shock noise prevention) when power mute is turned off.
- C3 (3.3 µF to 0.22 µF): Coupling capacitor for the MIX amplifier output and the BTL amplifier input.
- C4 (100 µF to 0.1 µF): Decoupling capacitor for virtual grounding and high-region noise cleaning.
- C5 (4.7 µF to 1.0 µF): LPF pin for V_{REF} amplifier reference bias.
  Ripple rejection ratio can be varied by changing the capacitance.
- C6 (22 µF to 3.3 µF): LPF capacitor for internal ripple filter reference bias.
  Ripple rejection ratio can be varied by changing the capacitance.
- C7 (33 µF to 10 µF): ALC rectifying capacitor for PVSS, output limiter and non-clipping circuit.

- C8 (0.33 µF to 0.1 µF): Coupling capacitor for PVSS detection input and H·P power output. Not needed when PVSS is not used.
- C9 (0.1 µF to 0.01 µF): Capacitor for SP/H·P switching smoothing (charging/discharging).
- C10 (0.47 µF to 2.2 µF): Capacitor for blocking common amplifier oscillation. Polyester film or ceramic capacitor (of which capacitance specified must be independent of temperature changes) is recommended. Not needed when common amplifier is turned off.
- C11 (22 µF to 47 µF): Ripple filter output capacitor. Also functions as oscillation blocking capacitor.
- C12 (220 µF to 10 µF): Power supply capacitor.
  * Use of a Tantalum capacitor is recommended for C11 and C12, because electrolytic capacitors cause the high-region impedance to increase at low temperatures.

Description of Each System

1. Ripple filter

- Used when the ripple level on the power line is high and a high ripple rejection ratio is needed in the amplifier block. When not needed, pins 1, 23 and 24 must be left open. (Refer to Sample Application Circuit 2.)
- When using a ripple filter, the output Tr V_{CE} voltage and the pin 1 C1 capacitance (LPF capacitor for the reference bias) must be adjusted according to the power supply ripple level.

Power supply  The V_{CE} voltage must be adjusted to be ripple bottom peak voltage +0.1 V or more.

2. MONO amplifier block

- Adds the channel 1 and channel 2 inputs and outputs the addition in single-channel BTL operation.
- Non-clipping and output limiter circuits are built in as output control functions.

1) The output limiter detects the output level from the pin 20 detection input and controls the output level by means of ALC configuration. Adjust the level according to the speaker impedance, the power dissipation capability of the power supply, etc. If not needed, the pin 20 detection input must be left open.

2) The non-clipping circuit prevents large input-caused output clipping (degradation in sound quality). The detection input is connected internally, while the output level depends on the $V_{CC}2$ voltage and is controlled by means of ALC configuration.

3. H·P amplifier block

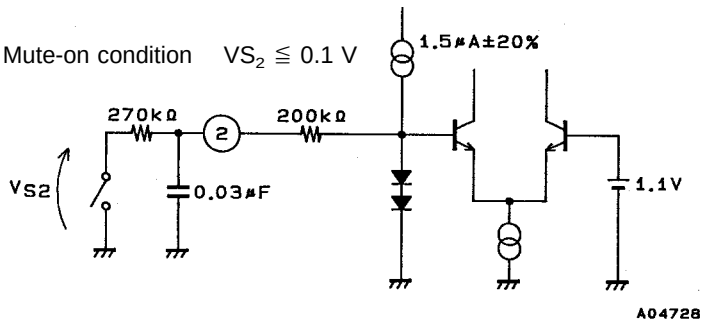
- Pin 11 (PWRC CONT) can be used to create a common amplifierless configuration. (This configuration is recommended when there is a possibility that the jack common pin may be shorted with GND in an application set.)
- The output control function PVSS (Peak Volume Select System) controls the output level by means of ALC configuration (keeping user-friendly volume level, etc.); the level can be varied by an external resistor.

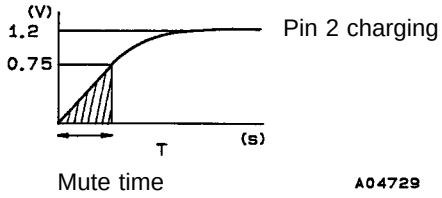
Descriptional of Each Block Switching

1. Power mute switch

- When an application set is microcomputer controlled, the power supply must be turned on/off with mute turned on in order to prevent shock noise. Even if an application set is not microcomputer controlled, the mute-on time for power-on can be set by the capacitance of the external capacitor on pin 2.

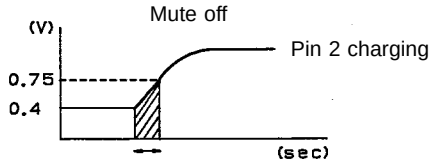
$$\text{Mute-on time} \fallingdotseq \frac{\text{Capacitance} \times 0.75\ \text{V}}{1.5\ \mu\text{A}}$$



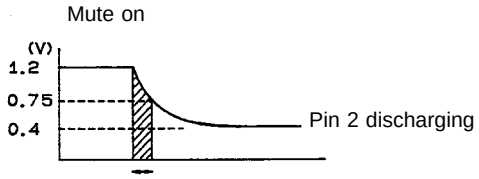


- An equivalent circuit for the mute circuit is shown on the previous page. If the power supply is turned on, the external capacitor is charged by the internal constant current; once the voltage reaches 0.75 V (the switching level), mute turns off and the pin 2 DC voltage stabilizes at approximately 1.2 V. To turn mute on, short through a resistor to pull down pin 2. In this way, smoothing is applied by using an external capacitor and resistor to prevent switching noise when mute is turned on/off.
- The mute-on/off time during normal operation is as shown below.

When 270 kΩ and 0.033 μF are used:



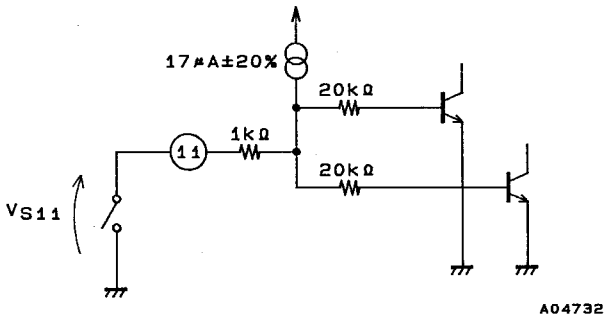
Mute-off time ≒ 8 ms A04730



Mute-on time ≒ 9 ms A04731

2. Common amplifier control switch

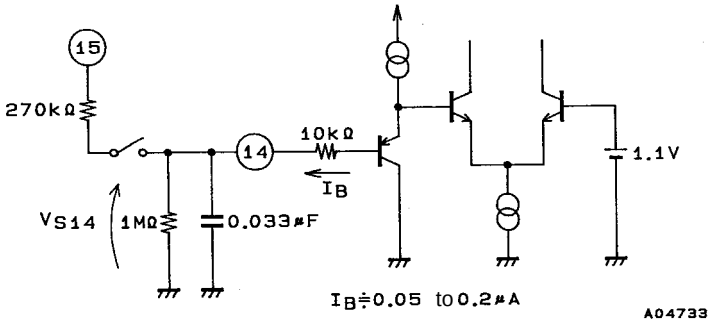
- When the headphone output is connected to other equipment, in an application set in which the common amplifier output (jack common pin) may be connected to GND causing overcurrent to flow from the common amplifier, it is necessary to turn off the common amplifier. In such an application, it is recommended to use the common capacitor scheme shown in Sample Application Circuit 2 where pin 11 is grounded to turn off the common amplifier.
- An equivalent circuit for the switching circuit is shown below.
- PWRC-off condition $V_{S11} \leqq 0.4$ V

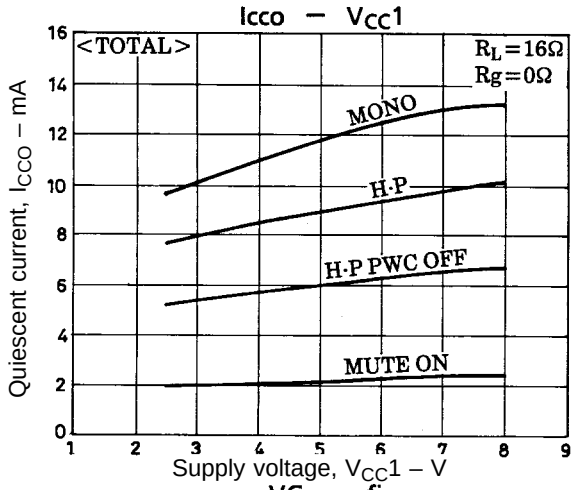


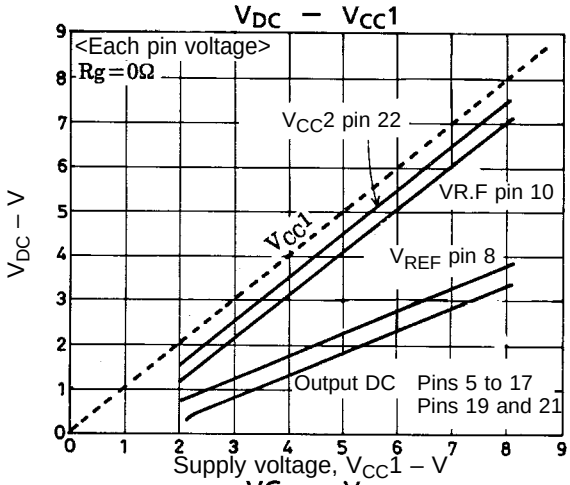
3. H·P/SP switch

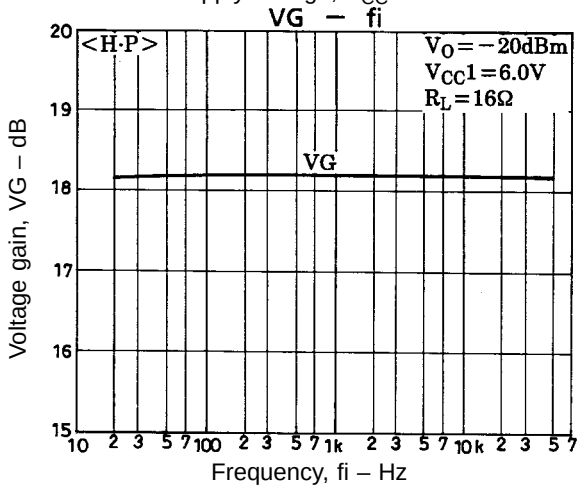
- This circuit uses a headphone jack with a switch to detect the headphone plug-in/out and automatically switch between the H·P amplifier and the MONO amplifier. When the H·P amplifier is operating, the MONO amplifier is turned off, and when the MONO amplifier is operating, the H·P amplifier is turned off.
- Smoothing is applied by using an external capacitor and resistor in order to prevent switching shock noise.
- Open H·P condition

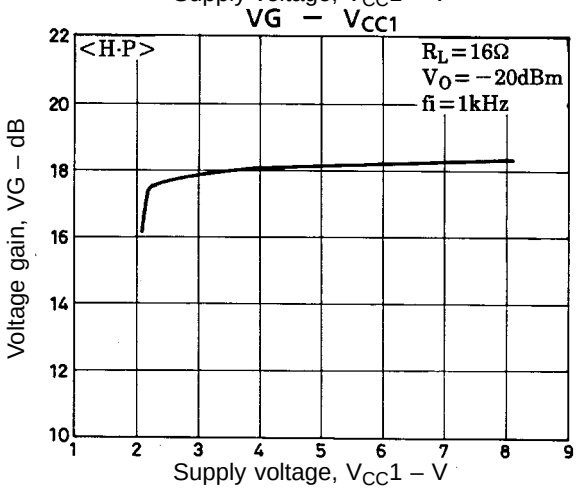
  $V_{S14} \leqq 0.2$ V

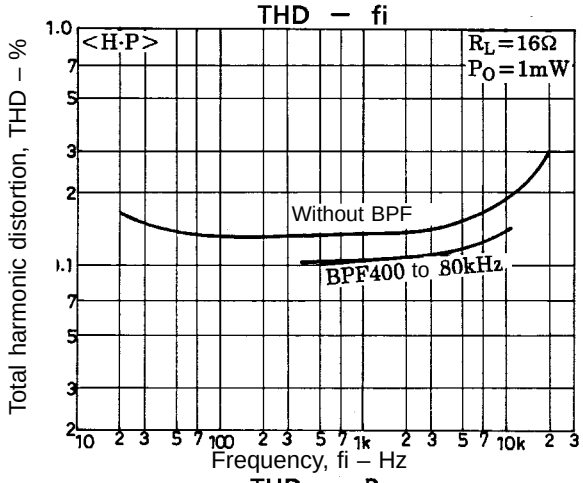


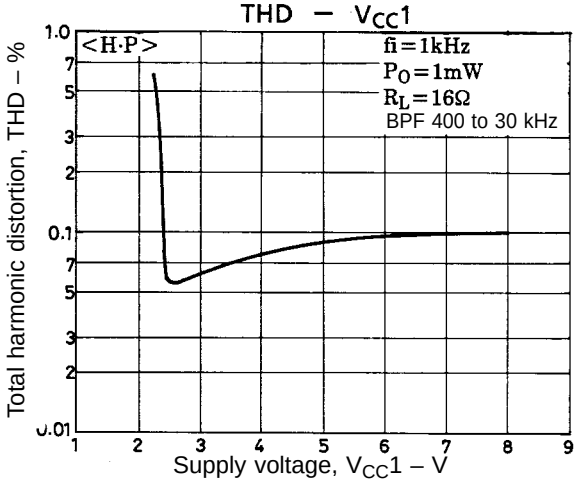

Icco – Vcc1
<TOTAL>
RL=16Ω
Rg=0Ω
MONO
H·P
H·P PWC OFF
MUTE ON
Quiescent current, ICCO – mA
Supply voltage, VCC1 – V

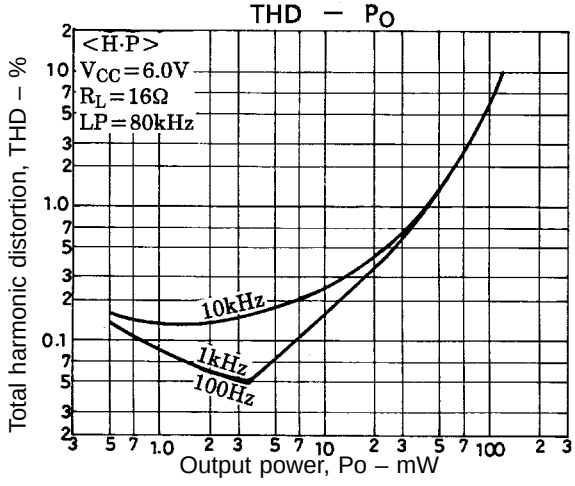

VDC – Vcc1
<Each pin voltage>
Rg=0Ω
VCC2 pin 22
VR.F pin 10
VCC1
VREF pin 8
Output DC Pins 5 to 17
Pins 19 and 21
VDC – V
Supply voltage, VCC1 – V

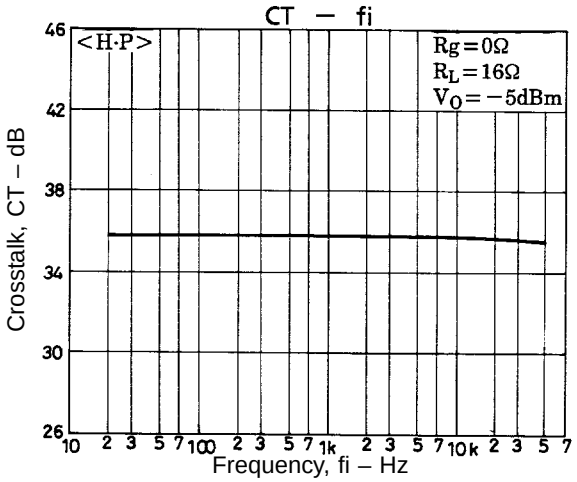

VG – fi
<H·P>
VO=–20dBm
VCC1=6.0V
RL=16Ω
VG
Voltage gain, VG – dB
Frequency, fi – Hz

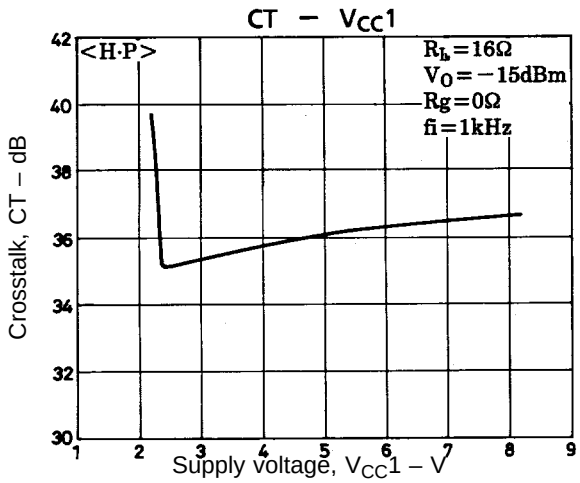

VG – VCC1
<H·P>
RL=16Ω
VO=–20dBm
fi=1kHz
Voltage gain, VG – dB
Supply voltage, VCC1 – V

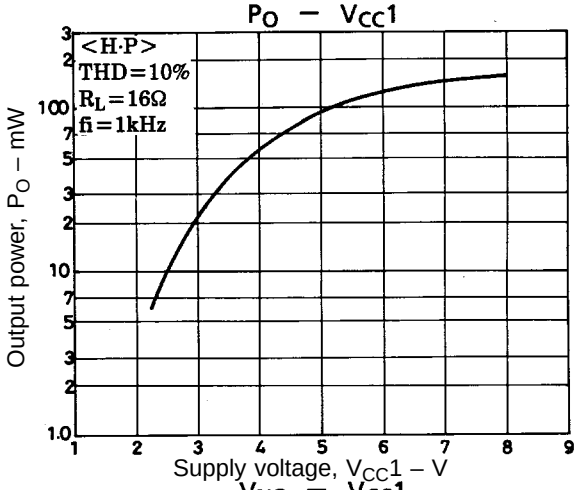

THD – fi
<H·P>
RL=16Ω
PO=1mW
Without BPF
BPF400 to 80kHz
Total harmonic distortion, THD – %
Frequency, fi – Hz

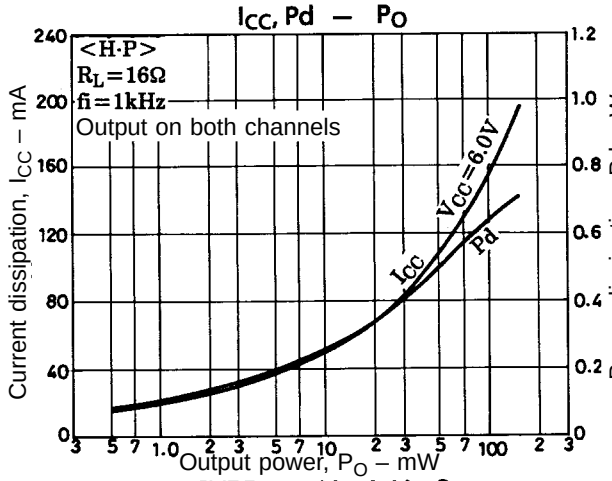

THD – VCC1
<H·P>
fi=1kHz
PO=1mW
RL=16Ω
BPF 400 to 30 kHz
Total harmonic distortion, THD – %
Supply voltage, VCC1 – V

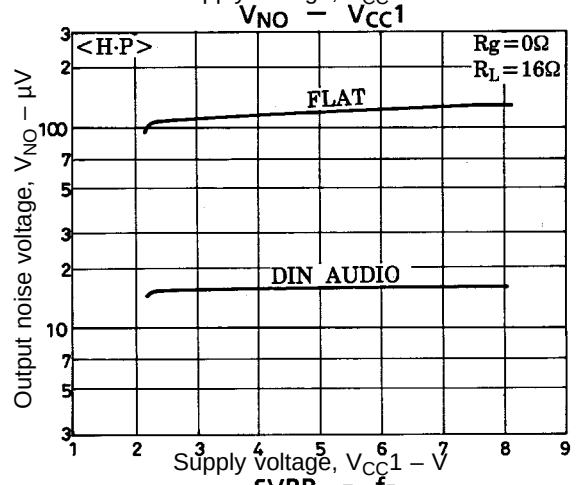

THD – PO
<H·P>
VCC=6.0V
RL=16Ω
LP=80kHz
10kHz
1kHz
100Hz
Total harmonic distortion, THD – %
Output power, Po – mW

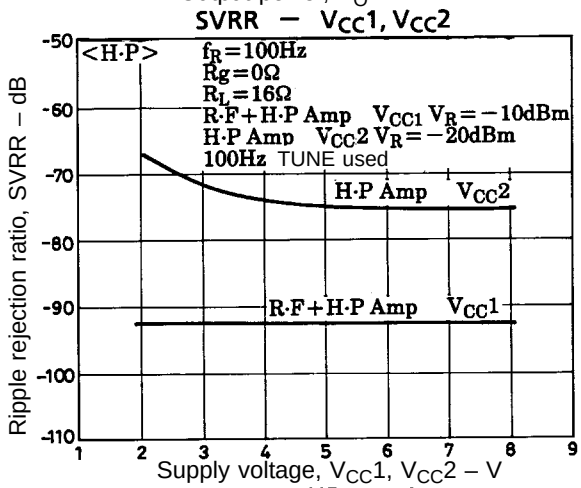

CT – fi
<H·P>
Rg=0Ω
RL=16Ω
VO=–5dBm
Crosstalk, CT – dB
Frequency, fi – Hz

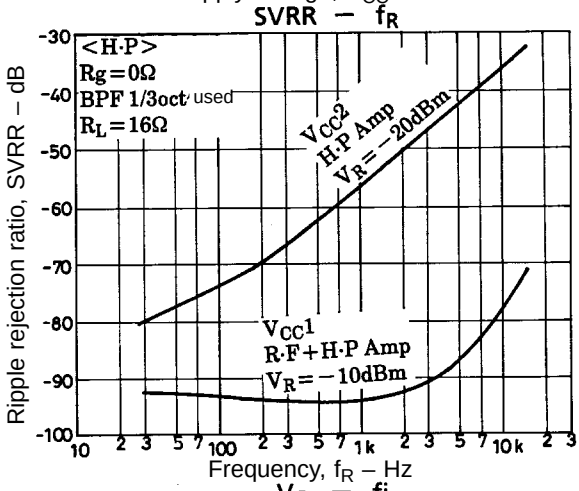

CT – VCC1
<H·P>
RL=16Ω
VO=–15dBm
Rg=0Ω
fi=1kHz
Crosstalk, CT – dB
Supply voltage, VCC1 – V

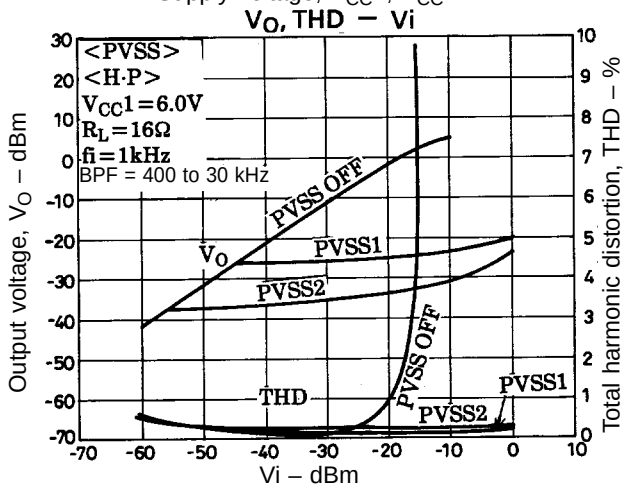

PO – VCC1
<H·P>
THD=10%
RL=16Ω
fi=1kHz
Output power, PO – mW
Supply voltage, VCC1 – V

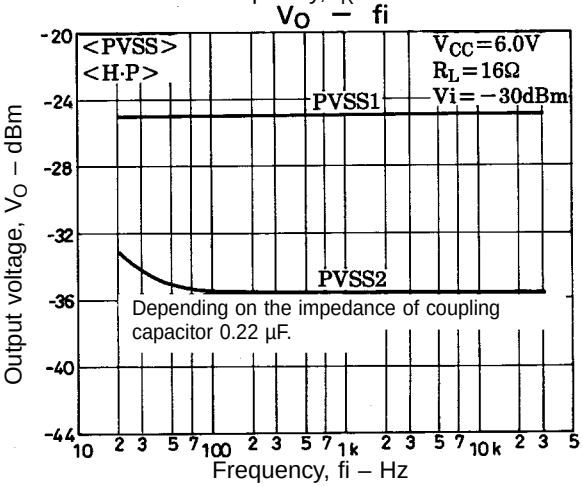

ICC, Pd – PO
<H·P>
RL=16Ω
fi=1kHz
Output on both channels
VCC=6.0V
ICC
Pd
Current dissipation, ICC – mA
Power dissipation, Pd – W
Output power, PO – mW

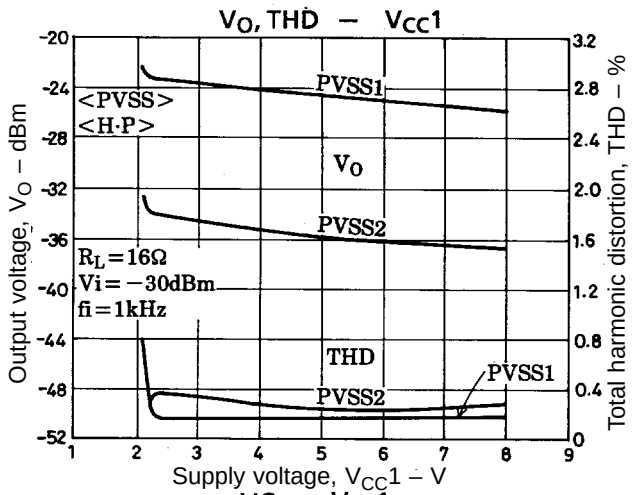

VNO – VCC1
<H·P>
Rg=0Ω
RL=16Ω
FLAT
DIN AUDIO
Output noise voltage, VNO – μV
Supply voltage, VCC1 – V

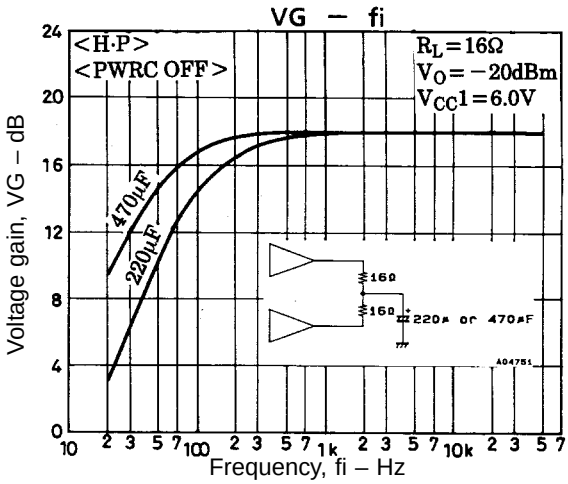

SVRR – VCC1, VCC2
<H·P>
fR=100Hz
Rg=0Ω
RL=16Ω
R·F+H·P Amp VCC1 VR=–10dBm
H·P Amp VCC2 VR=–20dBm
100Hz TUNE used
H·P Amp VCC2
R·F+H·P Amp VCC1
Ripple rejection ratio, SVRR – dB
Supply voltage, VCC1, VCC2 – V

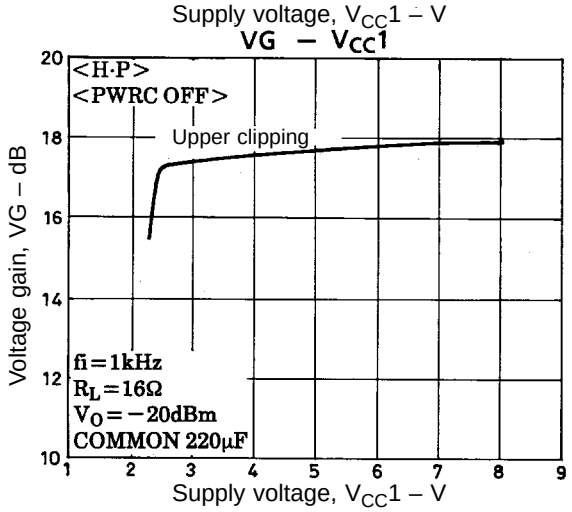

SVRR – fR
<H·P>
Rg=0Ω
BPF 1/3oct used
RL=16Ω
VCC2
H·P Amp
VR=–20dBm
VCC1
R·F+H·P Amp
VR=–10dBm
Ripple rejection ratio, SVRR – dB
Frequency, fR – Hz

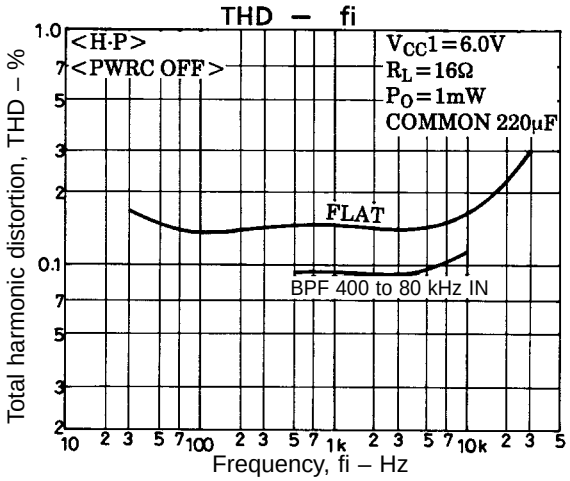

VO, THD – Vi
<PVSS>
<H·P>
VCC1=6.0V
RL=16Ω
fi=1kHz
BPF = 400 to 30 kHz
PVSS OFF
VO
PVSS1
PVSS2
THD
PVSS OFF
PVSS1
PVSS2
Output voltage, VO – dBm
Total harmonic distortion, THD – %
Vi – dBm

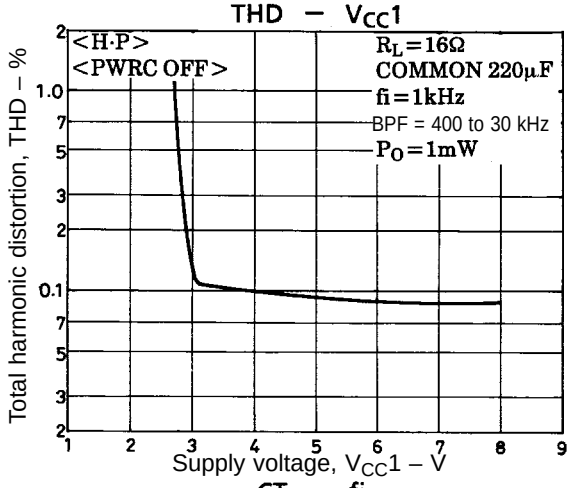

VO – fi
<PVSS>
<H·P>
VCC=6.0V
RL=16Ω
Vi=–30dBm
PVSS1
PVSS2
Depending on the impedance of coupling capacitor 0.22 μF.
Output voltage, VO – dBm
Frequency, fi – Hz

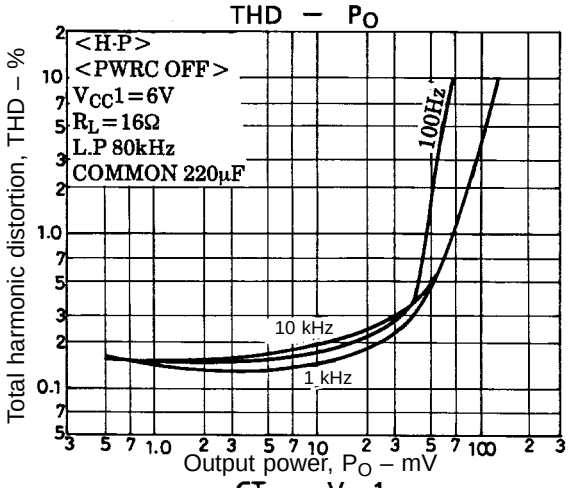

VO, THD – VCC1
<PVSS>
<H·P>
PVSS1
VO
PVSS2
RL=16Ω
Vi=−30dBm
fi=1kHz
THD
PVSS1
PVSS2
Output voltage, VO – dBm
Total harmonic distortion, THD – %
Supply voltage, VCC1 – V

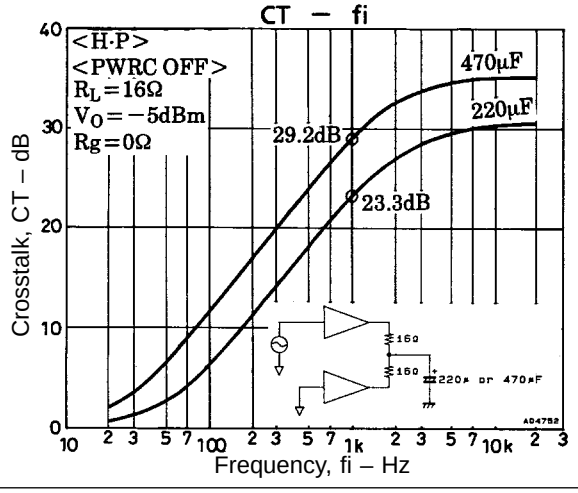

VG – fi
<H·P>
<PWRC OFF>
RL=16Ω
VO=−20dBm
VCC1=6.0V
470µF
220µF
16Ω
16Ω
220µF or 470µF
Voltage gain, VG – dB
Frequency, fi – Hz

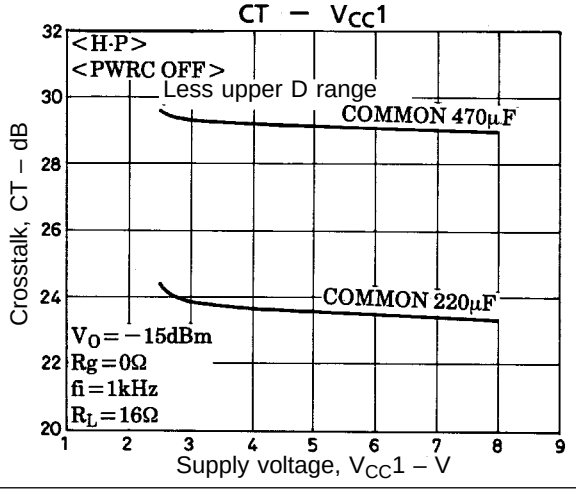

VG – VCC1
<H·P>
<PWRC OFF>
Upper clipping
fi=1kHz
RL=16Ω
VO=−20dBm
COMMON 220µF
Voltage gain, VG – dB
Supply voltage, VCC1 – V

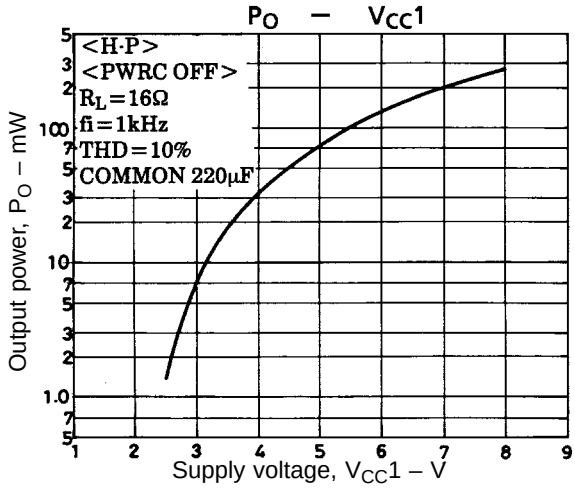

THD – fi
<H·P>
<PWRC OFF>
VCC1=6.0V
RL=16Ω
PO=1mW
COMMON 220µF
FLAT
BPF 400 to 80 kHz IN
Total harmonic distortion, THD – %
Frequency, fi – Hz

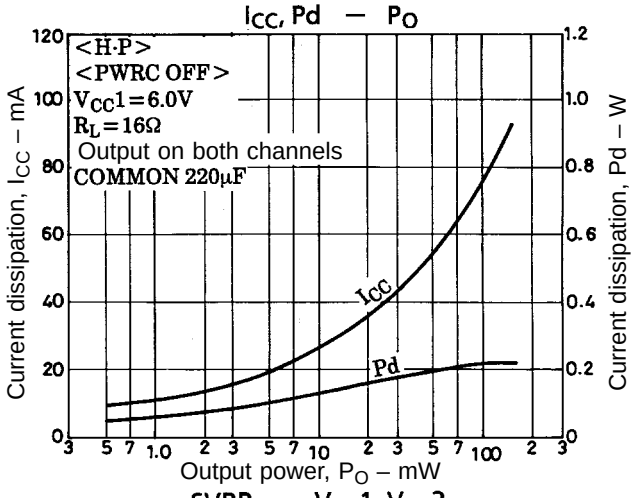

THD – VCC1
<H·P>
<PWRC OFF>
RL=16Ω
COMMON 220µF
fi=1kHz
BPF = 400 to 30 kHz
PO=1mW
Total harmonic distortion, THD – %
Supply voltage, VCC1 – V

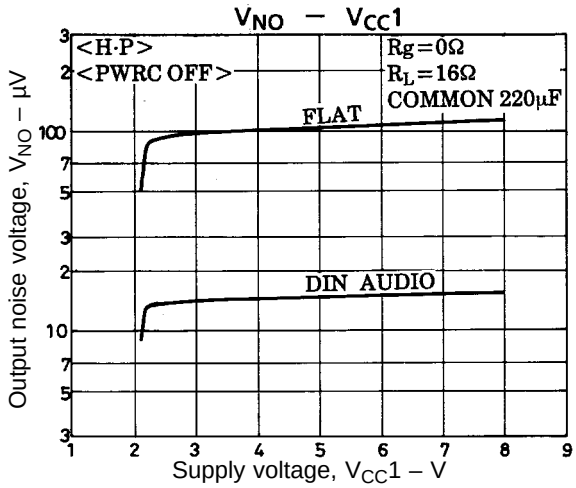

THD – PO
<H·P>
<PWRC OFF>
VCC1=6V
RL=16Ω
L.P 80kHz
COMMON 220µF
100Hz
10 kHz
1 kHz
Total harmonic distortion, THD – %
Output power, PO – mV

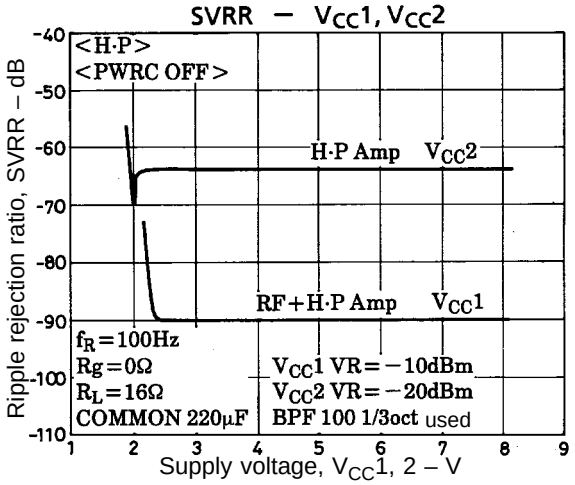

CT – fi
<H·P>
<PWRC OFF>
RL=16Ω
VO=−5dBm
Rg=0Ω
470µF
220µF
29.2dB
23.3dB
16Ω
16Ω
220µF or 470µF
Crosstalk, CT – dB
Frequency, fi – Hz

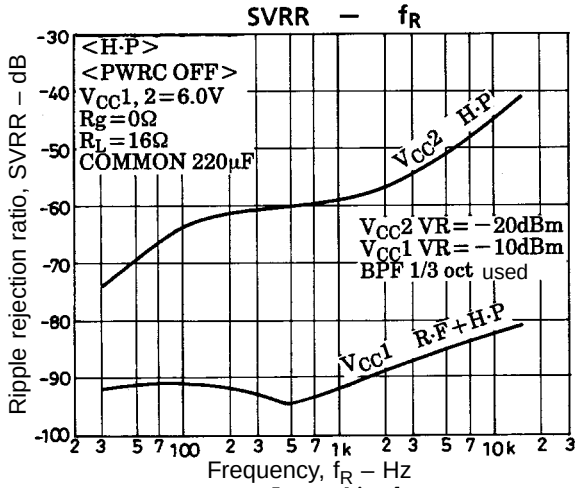

CT – VCC1
<H·P>
<PWRC OFF>
Less upper D range
COMMON 470µF
COMMON 220µF
VO=−15dBm
Rg=0Ω
fi=1kHz
RL=16Ω
Crosstalk, CT – dB
Supply voltage, VCC1 – V

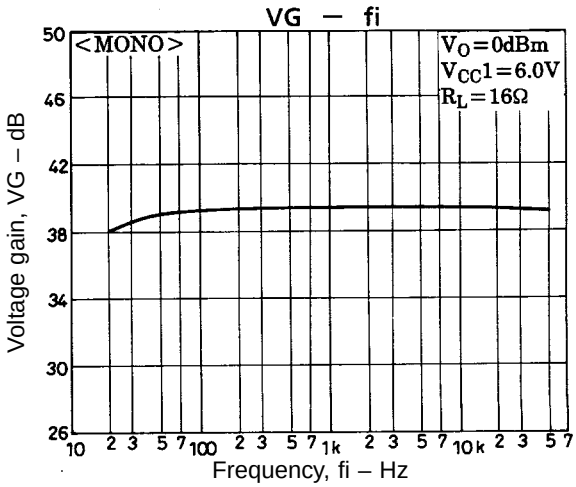

P_O – $V_{CC}1$
<H·P>
<PWRC OFF>
R_L=16Ω
fi=1kHz
THD=10%
COMMON 220μF
Output power, P_O – mW
Supply voltage, $V_{CC}1$ – V

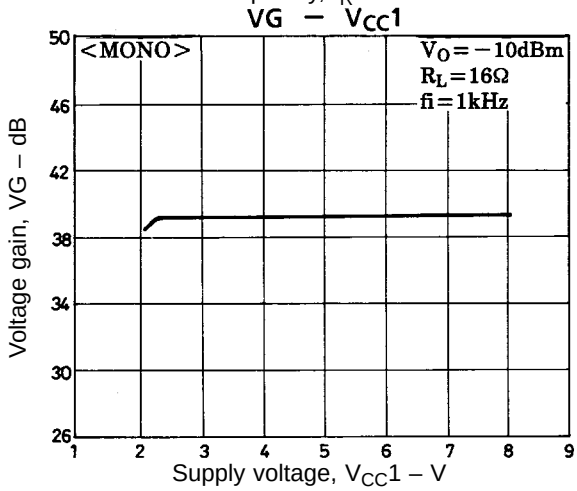

I_{CC}, Pd – P_O
<H·P>
<PWRC OFF>
$V_{CC}1$=6.0V
R_L=16Ω
Output on both channels
COMMON 220μF
Icc
Pd
Current dissipation, I_{CC} – mA
Current dissipation, Pd – W
Output power, P_O – mW

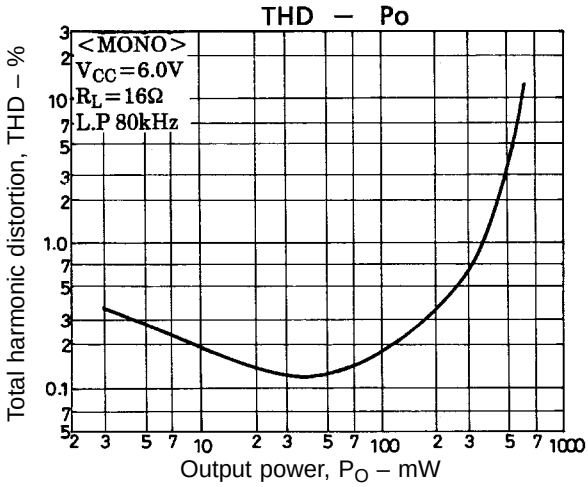

V_{NO} – $V_{CC}1$
<H·P>
<PWRC OFF>
Rg=0Ω
R_L=16Ω
COMMON 220μF
FLAT
DIN AUDIO
Output noise voltage, V_{NO} – μV
Supply voltage, $V_{CC}1$ – V

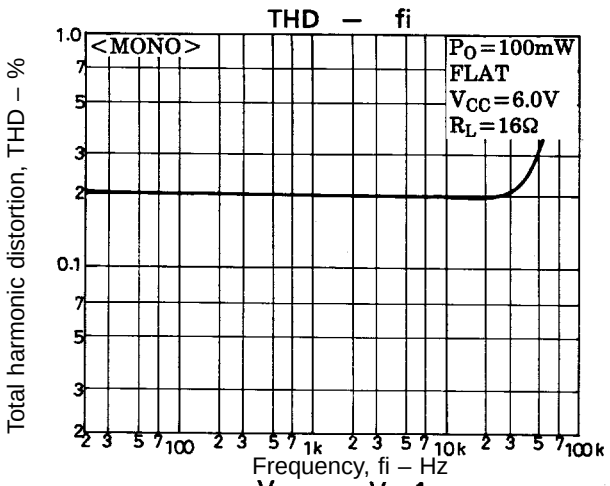

SVRR – $V_{CC}1$, $V_{CC}2$
<H·P>
<PWRC OFF>
H·P Amp $V_{CC}2$
RF+H·P Amp $V_{CC}1$
f_R=100Hz
Rg=0Ω
R_L=16Ω
COMMON 220μF
$V_{CC}1$ VR=−10dBm
$V_{CC}2$ VR=−20dBm
BPF 100 1/3oct used
Ripple rejection ratio, SVRR – dB
Supply voltage, V_{CC}1, 2 – V

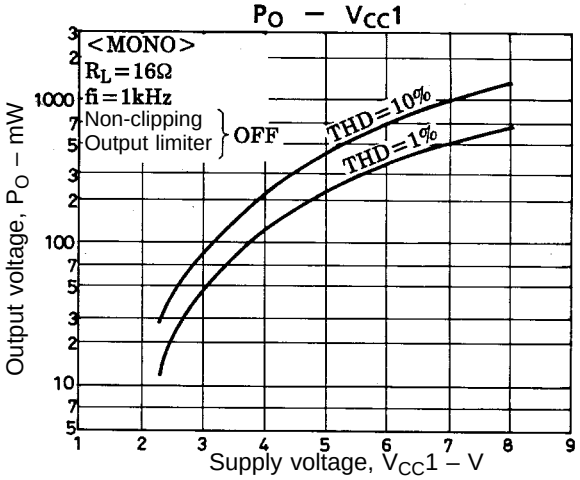

SVRR – f_R
<H·P>
<PWRC OFF>
V_{CC}1, 2=6.0V
Rg=0Ω
R_L=16Ω
COMMON 220μF
$V_{CC}2$ H·P
$V_{CC}2$ VR=−20dBm
$V_{CC}1$ VR=−10dBm
BPF 1/3 oct used
$V_{CC}1$ R·F+H·P
Ripple rejection ratio, SVRR – dB
Frequency, f_R – Hz

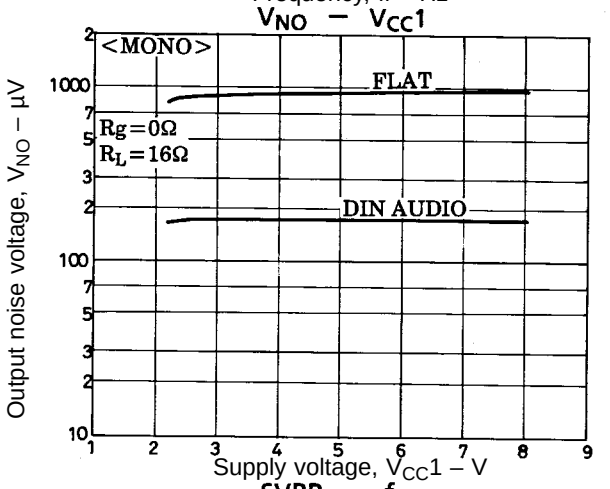

VG – fi
<MONO>
V_O=0dBm
V_{CC}1=6.0V
R_L=16Ω
Voltage gain, VG – dB
Frequency, fi – Hz

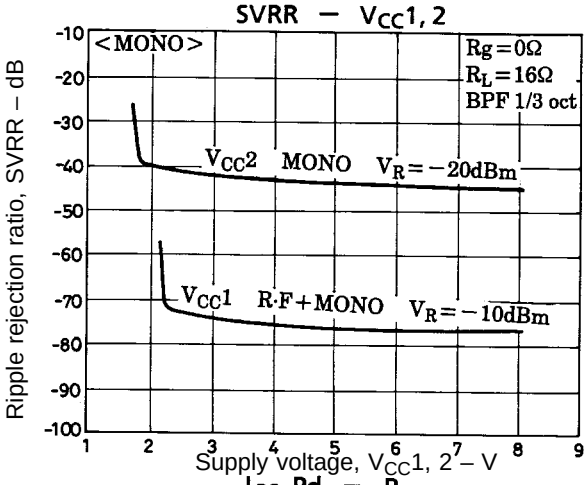

VG – $V_{CC}1$
<MONO>
V_O=−10dBm
R_L=16Ω
fi=1kHz
Voltage gain, VG – dB
Supply voltage, V_{CC}1 – V

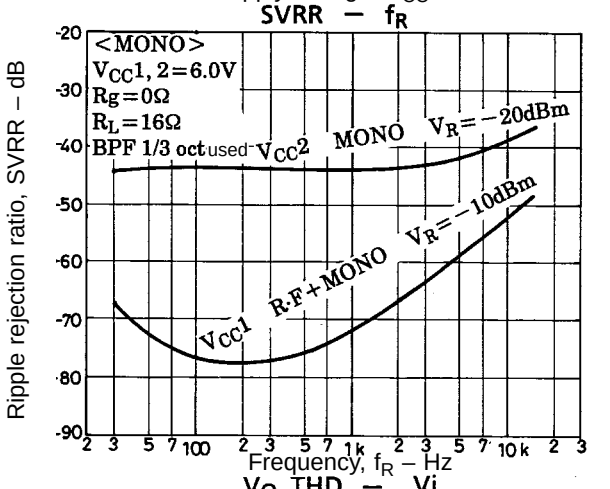

THD – Po
<MONO>
V_{CC}=6.0V
R_L=16Ω
L.P 80kHz
Total harmonic distortion, THD – %
Output power, P_O – mW

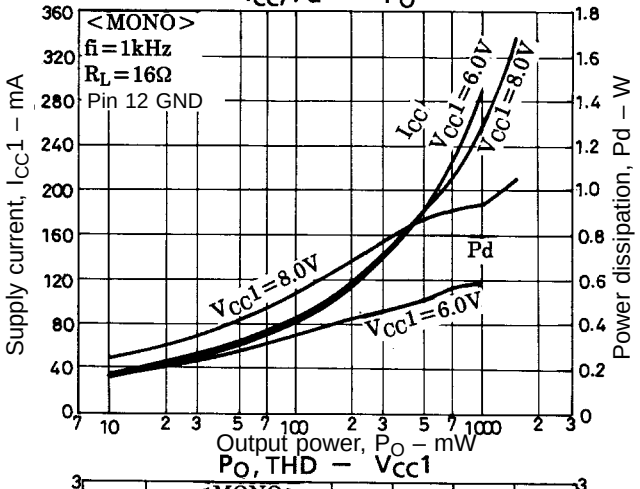

THD – fi
<MONO>
PO=100mW
FLAT
VCC=6.0V
RL=16Ω
Total harmonic distortion, THD – %
Frequency, fi – Hz

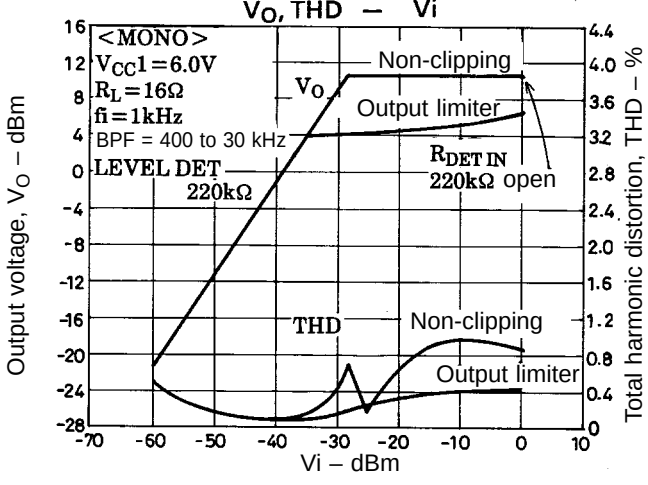

PO – VCC1
<MONO>
RL=16Ω
fi=1kHz
Non-clipping
Output limiter
OFF
THD=10%
THD=1%
Output voltage, PO – mW
Supply voltage, VCC1 – V

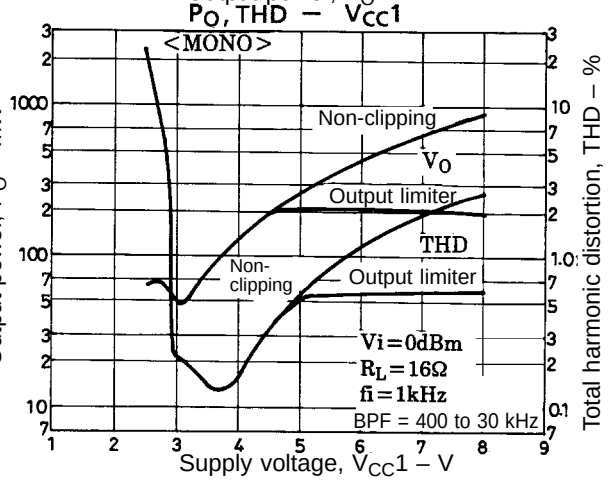

VNO – VCC1
<MONO>
FLAT
Rg=0Ω
RL=16Ω
DIN AUDIO
Output noise voltage, VNO – μV
Supply voltage, VCC1 – V


SVRR – VCC1, 2
<MONO>
Rg=0Ω
RL=16Ω
BPF 1/3 oct
VCC2 MONO VR=–20dBm
VCC1 R·F+MONO VR=–10dBm
Ripple rejection ratio, SVRR – dB
Supply voltage, VCC1, 2 – V

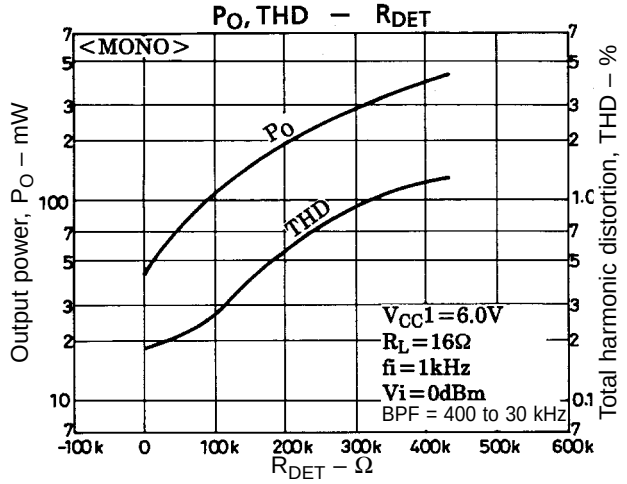

SVRR – fR
<MONO>
VCC1, 2=6.0V
Rg=0Ω
RL=16Ω
BPF 1/3 oct used
VCC2 MONO VR=–20dBm
VCC1 R·F+MONO VR=–10dBm
Ripple rejection ratio, SVRR – dB
Frequency, fR – Hz


ICC, Pd – PO
<MONO>
fi=1kHz
RL=16Ω
Pin 12 GND
ICC
VCC1=6.0V
VCC1=8.0V
Pd
Supply current, ICC1 – mA
Power dissipation, Pd – W
Output power, PO – mW

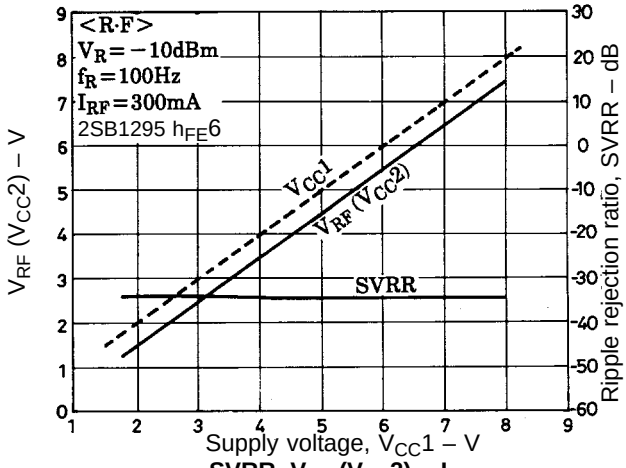

VO, THD – Vi
<MONO>
VCC1=6.0V
RL=16Ω
fi=1kHz
BPF = 400 to 30 kHz
LEVEL DET
220kΩ
RDET IN
220kΩ open
VO
Non-clipping
Output limiter
THD
Non-clipping
Output limiter
Output voltage, VO – dBm
Total harmonic distortion, THD – %
Vi – dBm


PO, THD – VCC1
<MONO>
Non-clipping
VO
Output limiter
THD
Non-clipping
Output limiter
Vi=0dBm
RL=16Ω
fi=1kHz
BPF = 400 to 30 kHz
Output power, PO – mW
Total harmonic distortion, THD – %
Supply voltage, VCC1 – V

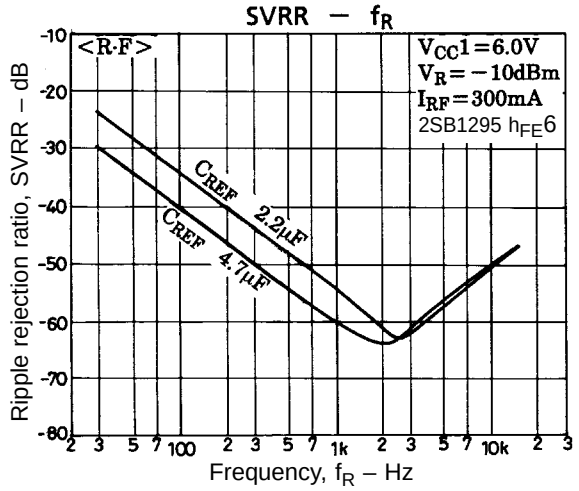
P_O, THD – R_{DET}



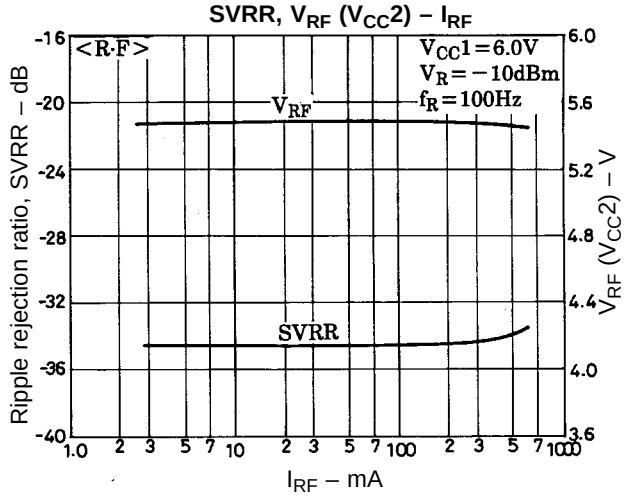
V_{RF} ($V_{CC}2$), SVRR – $V_{CC}1$



SVRR – f_R



SVRR, V_{RF} ($V_{CC}2$) – I_{RF}



SVRR – V_R