19-3185; Rev 1; 3/04

MAXIM

256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers

General Description

The MAX5417/MAX5418/MAX5419 nonvolatile, linear-taper, digital potentiometers perform the function of a mechanical potentiometer, but replace the mechanics with a simple 2-wire digital interface, allowing communication with multiple devices. Each device performs the same function as a discrete potentiometer or variable resistor and has 256 tap points.

The devices feature an internal, nonvolatile EEPROM used to store the wiper position for initialization during power-up. The fast-mode I²C™-compatible serial interface allows communication at data rates up to 400kbps, minimizing board space and reducing interconnection complexity in many applications. Each device is available with one of four factory-preset addresses (see the *Selector Guide*) and features an address input for a total of eight unique address combinations.

The MAX5417/MAX5418/MAX5419 provide three nominal resistance values: 50kΩ (MAX5417), 100kΩ (MAX5418), or 200kΩ (MAX5419). The nominal resistor temperature coefficient is 50ppm/°C end-to-end, and only 5ppm/°C ratiometric. This makes the devices ideal for applications requiring a low-temperature-coefficient variable resistor, such as low-drift, programmable gain-amplifier circuit configurations.

The MAX5417/MAX5418/MAX5419 are available in a 3mm x 3mm 8-pin TDFN package, and are specified over the extended -40°C to +85°C temperature range.

Applications

Mechanical Potentiometer Replacement

Low-Drift Programmable-Gain Amplifiers

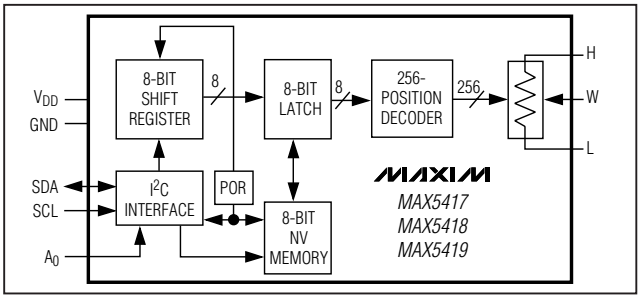
Volume Control

Liquid-Crystal Display (LCD) Contrast Control

Features

- **Power-On Recall of Wiper Position from Nonvolatile Memory**
- **Tiny 3mm x 3mm 8-Pin TDFN Package**
- **50ppm/°C End-to-End Resistance Temperature Coefficient**
- **5ppm/°C Ratiometric Temperature Coefficient**
- **50kΩ/100kΩ/200kΩ Resistor Values**
- **Fast I²C-Compatible Serial Interface**
- **500nA (typ) Static Supply Current**
- **Single-Supply Operation: +2.7V to +5.25V**
- **256 Tap Positions**
- **±0.5 LSB DNL in Voltage-Divider Mode**
- **±0.5 LSB INL in Voltage-Divider Mode**

Functional Diagram



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Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	I²C ADDRESS	R (kΩ)	TOP MARK
MAX5417LETA	-40°C to +85°C	8 TDFN-EP**	010100A_0	50	AIB
MAX5417META*	-40°C to +85°C	8 TDFN-EP**	010101A_0	50	ALS
MAX5417NETA*	-40°C to +85°C	8 TDFN-EP**	010110A_0	50	ALT
MAX5417PETA*	-40°C to +85°C	8 TDFN-EP**	010111A_0	50	ALU
MAX5418LETA	-40°C to +85°C	8 TDFN-EP**	010100A_0	100	AIC
MAX5418META*	-40°C to +85°C	8 TDFN-EP**	010101A_0	100	ALV
MAX5418NETA*	-40°C to +85°C	8 TDFN-EP**	010110A_0	100	ALW
MAX5418PETA*	-40°C to +85°C	8 TDFN-EP**	010111A_0	100	ALX
MAX5419LETA*	-40°C to +85°C	8 TDFN-EP**	010100A_0	200	AID
MAX5419META*	-40°C to +85°C	8 TDFN-EP**	010101A_0	200	ALY
MAX5419NETA*	-40°C to +85°C	8 TDFN-EP**	010110A_0	200	ALZ
MAX5419PETA*	-40°C to +85°C	8 TDFN-EP**	010111A_0	200	AMA

**Future product—contact factory for availability.*
***Exposed pad.*

Pin Configuration appears at end of data sheet.

256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6.0V
All Other Pins to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Continuous Current into H, L, and W
MAX5417 .....±1.3mA
MAX5418 .....±0.6mA
MAX5419 .....±0.3mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, H = V_{DD}, L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (VOLTAGE-DIVIDER MODE)						
Resolution			256			Taps
Integral Nonlinearity	INL	(Note 1)			±0.5	LSB
Differential Nonlinearity	DNL	(Note 1)			±0.5	LSB
End-to-End Temperature Coefficient	TC_R			50		ppm/°C
Ratiometric Temperature Coefficient				5		ppm/°C
Full-Scale Error		MAX5417_, 50Ω		-0.6		LSB
		MAX5418_, 100kΩ		-0.3		
Zero-Scale Error		MAX5417_, 50kΩ		0.6		LSB
		MAX5418_, 100kΩ		0.3		
DC PERFORMANCE (VARIABLE-RESISTOR MODE)						
Integral Nonlinearity (Note 2)	INL	V_{DD} = 3V			±3	LSB
		V_{DD} = 5V			±1.5	
Differential Nonlinearity (Note 2)	DNL	V_{DD} = 3V, MAX5417_, 50kΩ, guaranteed monotonic	-1		+2	LSB
		V_{DD} = 3V, MAX5418_, 100kΩ			±1	
		V_{DD} = 5V			±1	
DC PERFORMANCE (RESISTOR CHARACTERISTICS)						
Wiper Resistance	R_W	(Note 3)		325	675	Ω
Wiper Capacitance	C_W			10		pF
End-to-End Resistance	R_{HL}	MAX5417_	37.5	50	62.5	kΩ
		MAX5418_	75	100	125	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, H = V_{DD}, L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input High Voltage (Note 4)	V_{IH}	V_{DD} = 3.4V to 5.25V	2.4			V
		V_{DD} < 3.4V	0.7 x V_{DD}			
Input Low Voltage	V_{IL}	V_{DD} = 2.7V to 5.25V			0.8	V
Low-Level Output Voltage	V_{OL}	3mA sink current			0.4	V
Input Leakage Current	I_{LEAK}				±1	µA
Input Capacitance				5		pF
DYNAMIC CHARACTERISTICS						
Wiper -3dB Bandwidth (Note 5)		MAX5417		100		kHz
		MAX5418		50		
NONVOLATILE MEMORY						
Data Retention				50		Years
Endurance				200,000		Stores
POWER SUPPLY						
Power-Supply Voltage	V_{DD}		2.70		5.25	V
Standby Current	I_{DD}	Digital inputs = V_{DD} or GND		0.5	1	µA
Programming Current		During nonvolatile write; digital inputs = V_{DD} or GND (Note 6)		200	400	µA

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, H = V_{DD}, L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C. See Figures 1 and 2.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SECTION						
Wiper Settling Time (Note 8)	t_{IL}	MAX5417		500		ns
		MAX5418		600		
DIGITAL SECTION						
SCL Clock Frequency	f_{SCL}				400	kHz
Setup Time for START Condition	t_{SU-STA}		0.6			µs
Hold Time for START Condition	t_{HD-STA}		0.6			µs
CLK High Time	t_{HIGH}		0.6			µs
CLK Low Time	t_{LOW}		1.3			µs

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TIMING CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, H = V_{DD}, L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C. See Figures 1 and 2.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	t_{SU-DAT}		100			ns
Data Hold Time	t_{HD-DAT}		0		0.9	µs
SDA, SCL Rise Time	t_R				300	ns
SDA, SCL Fall Time	t_F				300	ns
Setup Time for STOP Condition	t_{SU-STO}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}	Minimum power-up rate = 0.2V/ms	1.3			µs
Pulse Width of Spike Suppressed	t_{SP}				50	ns
Maximum Capacitive Load for Each Bus Line	C_B	(Note 9)		400		pF
Nonvolatile Store Time		Idle time required after a nonvolatile memory write (Note 10)	30			ms

Note 1: The DNL and INL are measured with the potentiometer configured as a voltage-divider with H = V_{DD} and L = GND. The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.

Note 2: The DNL and INL are measured with the potentiometer configured as a variable resistor. H is unconnected and L = GND. For the 5V condition, the wiper terminal is driven with a source current of 80µA for the 50kΩ configuration, 40µA for the 100kΩ configuration, and 20µA for the 200kΩ configuration. For the 3V condition the wiper terminal is driven with a source current of 40µA for the 50kΩ configuration, 20µA for the 100kΩ configuration, and 10µA for the 200kΩ configuration.

Note 3: The wiper resistance is measured using the source currents given in Note 2.

Note 4: The device draws current in excess of the specified supply current when this input is driven with a voltage greater than 0.7 x V_{DD}. This is due to the complementary metal-oxide semiconductor (CMOS) shunt current (P- and N-channel output devices on simultaneously).

Note 5: Wiper at midscale with a 10pF load. Potentiometer set to midscale, L = GND, an AC source is applied to H, and the output is measured as 3dB lower than the DC W/H value in dB.

Note 6: The programming current operates only during power-up and NV writes.

Note 7: SCL clock period includes rise and fall times t_R and t_F. All digital input signals are specified with t_R = t_F = 2ns and timed from a voltage level of (V_{IL} + V_{IH}) / 2.

Note 8: Wiper settling time is the worst-case 0% to 50% rise time measured between consecutive wiper positions. H = V_{DD}, L = GND, and the wiper terminal is unloaded and measured with a 10pF oscilloscope probe (see the *Typical Operating Characteristics* for the tap-to-tap switching transient).

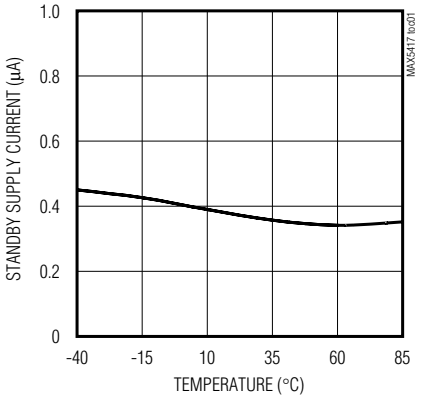
Note 9: An appropriate bus pullup resistance must be selected depending on board capacitance. Refer to the document linked to this web address: www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf

Note 10: The idle time begins from the initiation of the stop pulse.

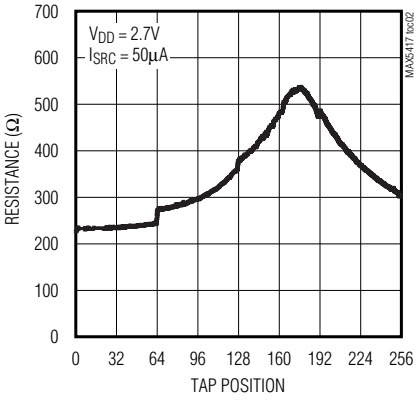
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

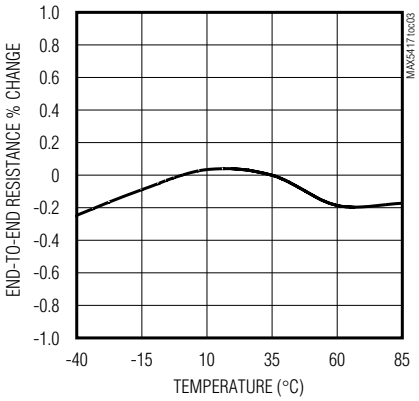
STANDBY SUPPLY CURRENT vs. TEMPERATURE



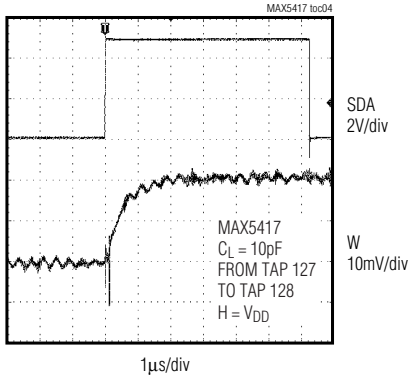
WIPER RESISTANCE vs. TAP POSITION (MAX5417)



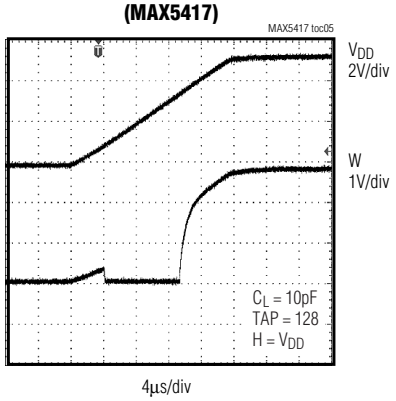
END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



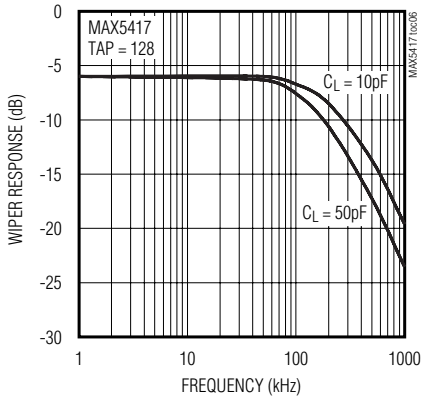
TAP-TO-TAP SWITCHING TRANSIENT



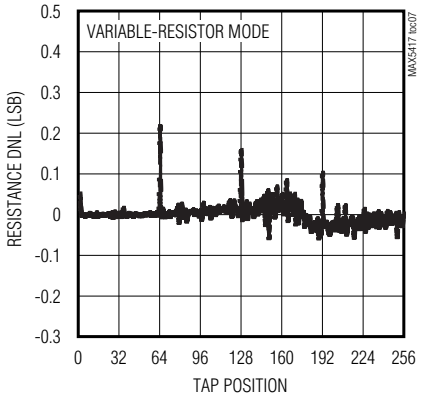
WIPER TRANSIENT AT POWER-ON (MAX5417)



MIDSCALE WIPER RESPONSE vs. FREQUENCY (MAX5417)



DNL vs. TAP POSITION (MAX5417)

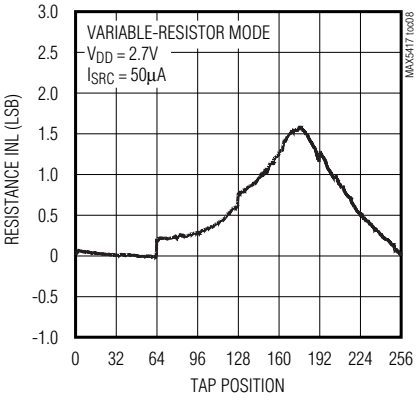


256-Tap, Nonvolatile, I²C-Interface, Digital Potentiometers

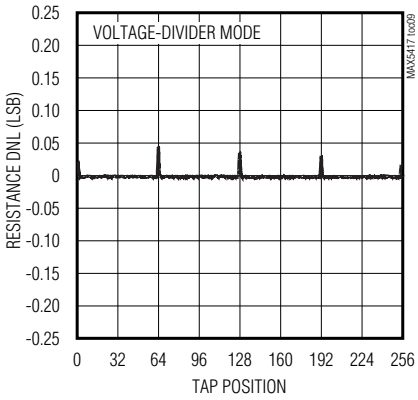
Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

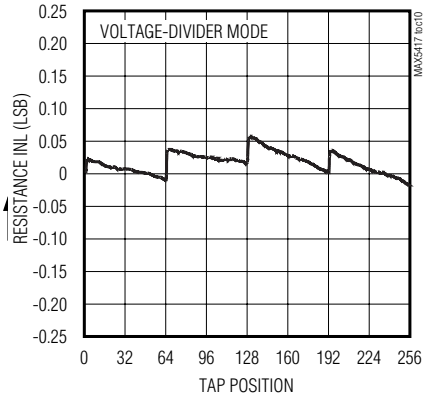
INL vs. TAP POSITION (MAX5417)



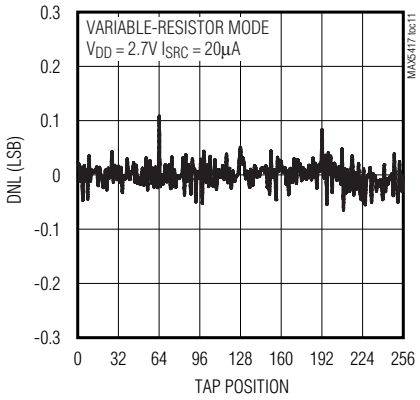
DNL vs. TAP POSITION



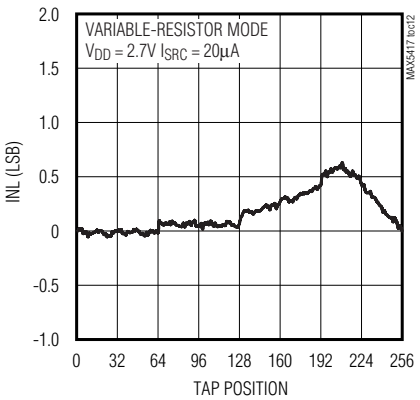
INL vs. TAP POSITION



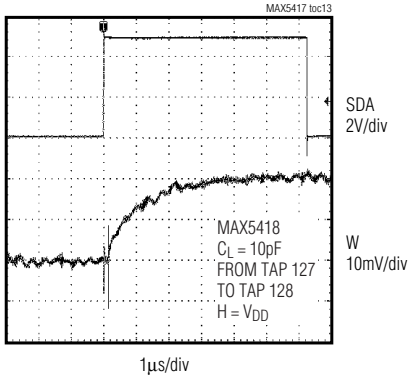
DNL vs. TAP POSITION (MAX5418)



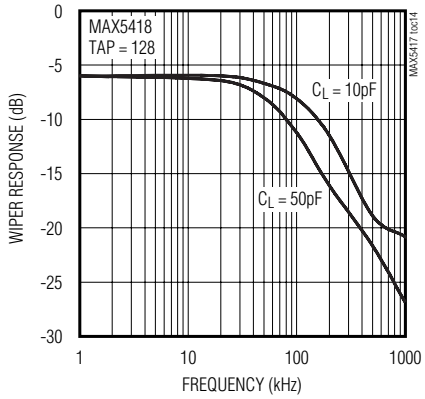
INL vs. TAP POSITION (MAX5418)



TAP-TO-TAP SWITCHING TRANSIENT



MIDSCALE WIPER RESPONSE vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Power-Supply Input. 2.7V to 5.25V voltage range. Bypass with a 0.1µF capacitor from V_{DD} to GND.
2	SCL	I²C-Interface Clock Input
3	SDA	I²C-Interface Data Input
4	A0	Address Input. Sets the A0 bit in the device ID address.
5	GND	Ground
6	L	Low Terminal
7	W	Wiper Terminal
8	H	High Terminal
—	EP	Exposed Pad

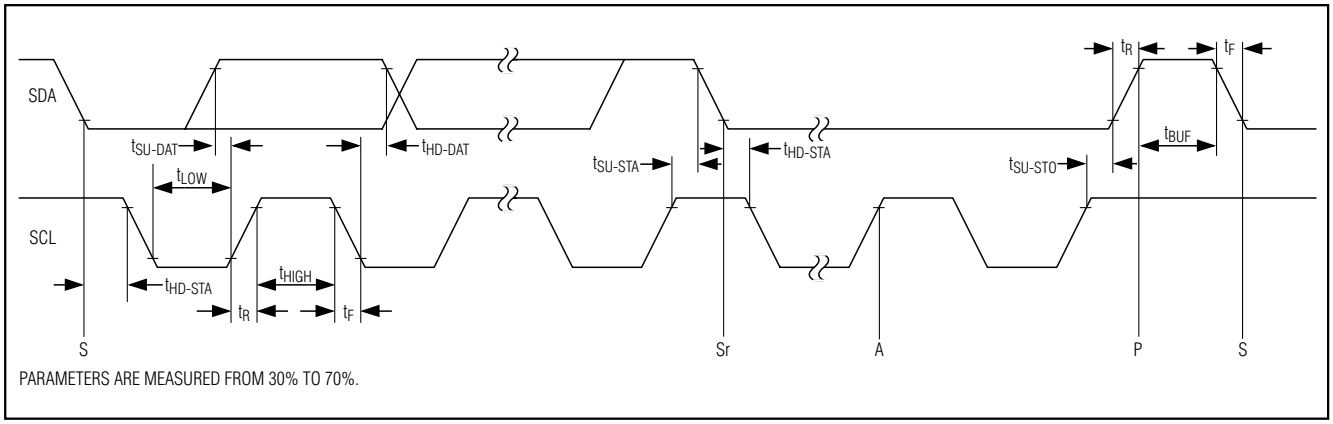


Figure 1. I²C Serial-Interface Timing Diagram

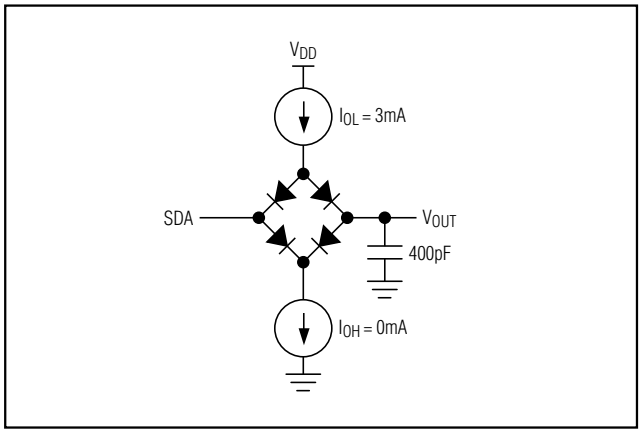


Figure 2. Load Circuit

Detailed Description

The MAX5417/MAX5418/MAX5419 contain a resistor array with 255 resistive elements. The MAX5417 has a total end-to-end resistance of 50kΩ, the MAX5418 has an end-to-end resistance of 100kΩ, and the MAX5419 has an end-to-end resistance of 200kΩ. The MAX5417/MAX5418/MAX5419 allow access to the high, low, and wiper terminals for a standard voltage-divider configuration. H, L, and W can be connected in any desired configuration as long as their voltages fall between GND and V_{DD}.

A simple 2-wire I²C-compatible serial interface moves the wiper among the 256 tap points. A nonvolatile memory stores and recalls the stored wiper position in the nonvolatile memory upon power-up. The nonvolatile memory is guaranteed for 200,000 wiper store cycles and 50 years for wiper data retention.

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Analog Circuitry

The MAX5417/MAX5418/MAX5419 consist of a resistor array with 255 resistive elements; 256 tap points are accessible to the wiper, W, along the resistor string between H and L. The wiper tap point is selected by programming the potentiometer through the 2-wire (I²C) interface. Eight data bits, an address byte, and a control byte program the wiper position. The H and L terminals of the MAX5417/MAX5418/MAX5419 are similar to the two end terminals of a mechanical potentiometer. The MAX5417/MAX5418/MAX5419 feature power-on reset circuitry that loads the wiper position from nonvolatile memory at power-up.

Digital Interface

The MAX5417/MAX5418/MAX5419 feature an internal, nonvolatile EEPROM that stores the wiper state for initialization during power-up. The shift register decodes the control and address bits, routing the data to the proper memory registers. Data can be written to a volatile memory register, immediately updating the wiper position, or data can be written to a nonvolatile register for storage.

The volatile register retains data as long as the device is powered. Once power is removed, the volatile register is cleared. The nonvolatile register retains data even after power is removed. Upon power-up, the power-on reset circuitry controls the transfer of data from the nonvolatile register to the volatile register.

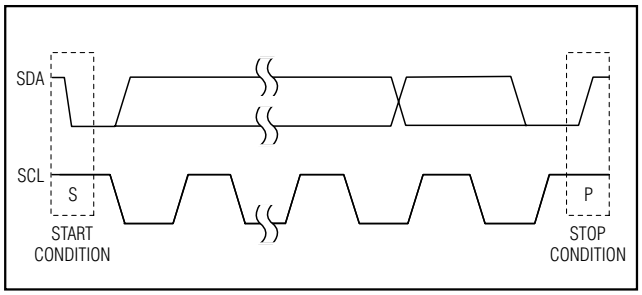

Figure 3. Start and Stop Conditions

Serial Addressing

The MAX5417/MAX5418/MAX5419 operate as a slave that receives data through an I²C- and SMBus™-compatible 2-wire interface. The interface uses a serial data access (SDA) line and a serial clock line (SCL) to achieve communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to the MAX5417/MAX5418/MAX5419, and generates the SCL clock that synchronizes the data transfer (Figure 1).

The MAX5417/MAX5418/MAX5419 SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on the SDA bus. The MAX5417/MAX5418/MAX5419 SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on the SCL bus if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START (S) condition (Figure 3) sent by a master, followed by the MAX5417/MAX5418/MAX5419 7-bit slave address plus the 8th bit (Figure 4), 1 command byte (Figure 7) and 1 data byte, and finally a STOP (P) condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning the SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 5).

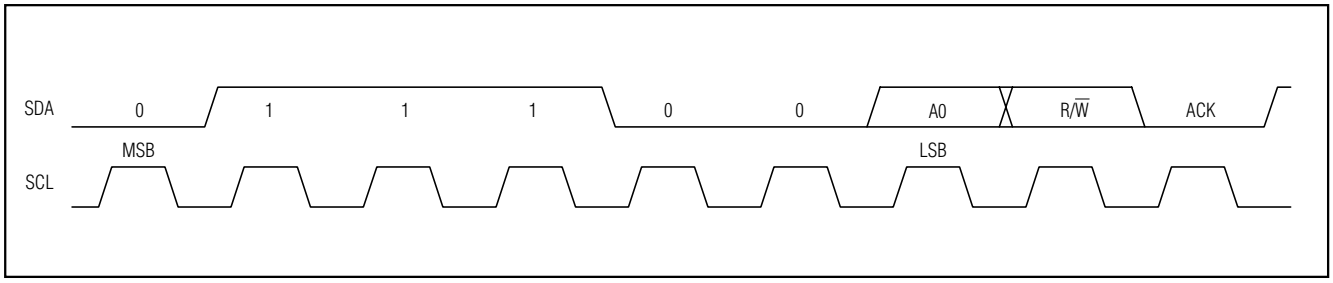

Figure 4. Slave Address

SMBus is a trademark of Intel Corporation.

Table 1. MAX5417/MAX5418/MAX5419 Address Codes

	ADDRESS BYTE							
PART SUFFIX	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**NOP/$\overline{W}$**
L	0	1	0	1	0	0	0	NOP/$\overline{W}$
L	0	1	0	1	0	0	1	NOP/$\overline{W}$
M	0	1	0	1	0	1	0	NOP/$\overline{W}$
M	0	1	0	1	0	1	1	NOP/$\overline{W}$
N	0	1	0	1	1	0	0	NOP/$\overline{W}$
N	0	1	0	1	1	0	1	NOP/$\overline{W}$
P	0	1	0	1	1	1	0	NOP/$\overline{W}$
P	0	1	0	1	1	1	1	NOP/$\overline{W}$

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 6). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5417/MAX5418/MAX5419, the devices generate the acknowledge bit because the MAX5417/MAX5418/MAX5419 are the recipients.

Slave Address

The MAX5417/MAX5418/MAX5419 have a 7-bit-long slave address (Figure 4). The 8th bit following the 7-bit slave address is the NOP/$\overline{W}$ bit. Set the NOP/$\overline{W}$ bit low for a write command and high for a no-operation command.

The MAX5417/MAX5418/MAX5419 are available in one of four possible slave addresses (Table 1). The first 4 bits (MSBs) of the MAX5417/MAX5418/MAX5419 slave addresses are always 0101. The next 2 bits are factory programmed (see Table 1). Connect the A0 input to either GND or V_{DD} to toggle between two unique device addresses for a part. Each device must have a unique address to share the bus. Therefore, a maximum of eight MAX5417/MAX5418/MAX5419 devices can share the same bus.

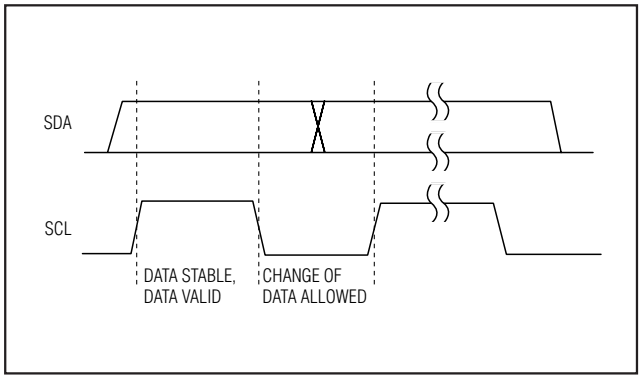

Figure 5. Bit Transfer

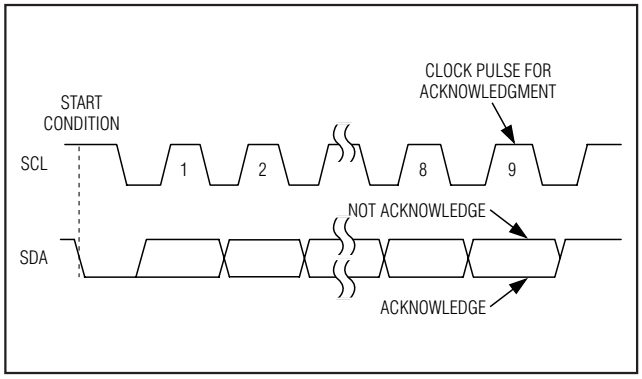

Figure 6. Acknowledge

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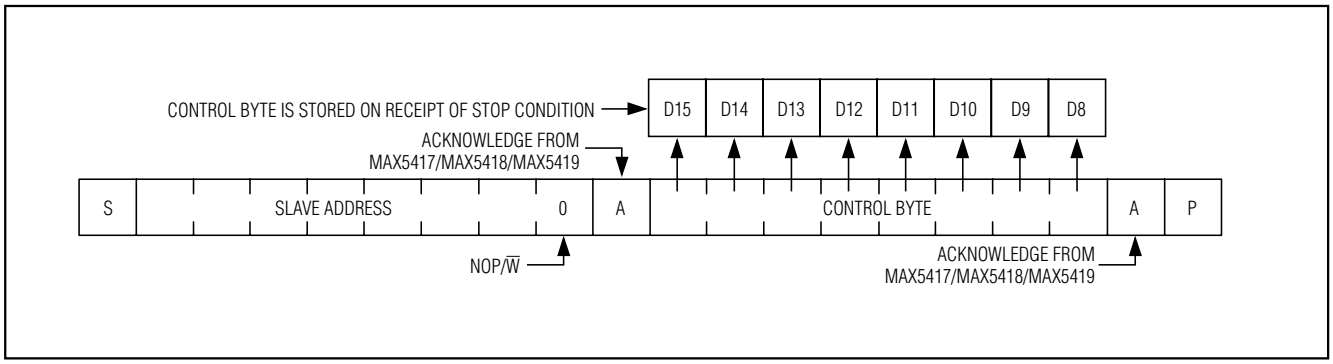

Figure 7. Command Byte Received

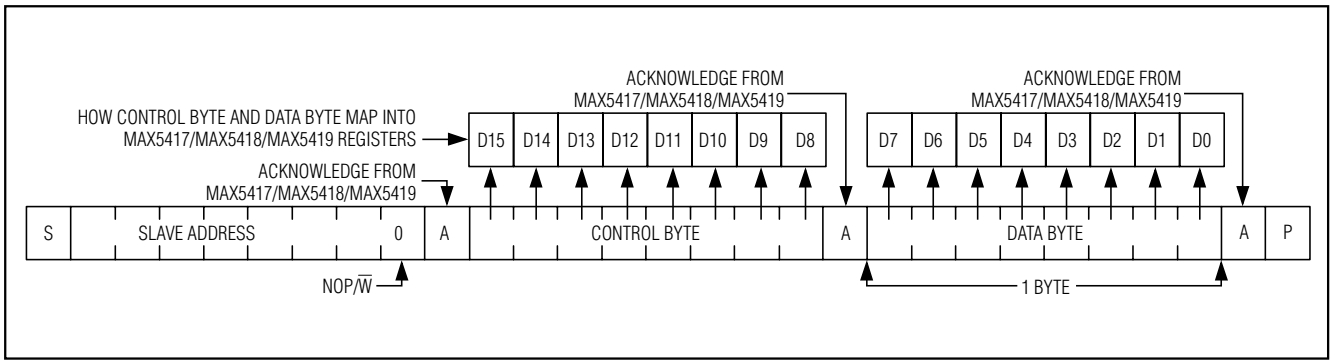

Figure 8. Command and Single Data Byte Received

Message Format for Writing

A write to the MAX5417/MAX5418/MAX5419 consists of the transmission of the device's slave address with the 8th bit set to zero, followed by at least 1 byte of information. The 1st byte of information is the command byte. The bytes received after the command byte are the data bytes. The 1st data byte goes into the internal register of the MAX5417/MAX5418/MAX5419 as selected by the command byte (Figure 8).

Command Byte

Use the command byte to select the source and destination of the wiper data (nonvolatile or volatile memory registers) and swap data between nonvolatile and volatile memory registers (see Table 2).

Command Descriptions

VREG: The data byte writes to the volatile memory register and the wiper position updates with the data in the volatile memory register.

NVREG: The data byte writes to the nonvolatile memory register. The wiper position is unchanged.

NVxREG: Data transfers from the nonvolatile memory register to the volatile memory register (wiper position updates).

VxNVREG: Data transfers from the volatile memory register into the nonvolatile memory register.

Table 2. Command Byte Summary

		ADDRESS BYTE									CONTROL BYTE									DATA BYTE									
SCL CYCLE NUMBER	START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	STOP
		A6	A5	A4	A3	A2	A1	A0		ACK		TX	NV	V	R3	R2	R1	R0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	
VREG		0	1	0	1	A2	A1	A0	0		0	0	0	1	0	0	0	1		D7	D6	D5	D4	D3	D2	D1	D0		
NVREG		0	1	0	1	A2	A1	A0	0		0	0	1	0	0	0	0	1		D7	D6	D5	D4	D3	D2	D1	D0		
NVxVREG		0	1	0	1	A2	A1	A0	0		0	1	1	0	0	0	0	1		D7	D6	D5	D4	D3	D2	D1	D0		
VxNVREG		0	1	0	1	A2	A1	A0	0		0	1	0	1	0	0	0	1		D7	D6	D5	D4	D3	D2	D1	D0		

Nonvolatile Memory

The internal EEPROM consists of an 8-bit nonvolatile register that retains the value written to it before the device is powered down. The nonvolatile register is programmed with the zero-scale value at the factory.

Power-Up

Upon power-up, the MAX5417/MAX5418/MAX5419 load the data stored in the nonvolatile memory register into the volatile memory register, updating the wiper position with the data stored in the nonvolatile memory register. This initialization period takes 10µs.

Standby

The MAX5417/MAX5418/MAX5419 feature a low-power standby. When the device is not being programmed, it goes into standby mode and power consumption is typically 500nA.

Applications Information

The MAX5417/MAX5418/MAX5419 are intended for circuits requiring digitally controlled adjustable resistance, such as LCD contrast control (where voltage biasing adjusts the display contrast), or for programmable filters with adjustable gain and/or cutoff frequency.

Positive LCD Bias Control

Figures 9 and 10 show an application where the voltage-divider or variable resistor is used to make an adjustable, positive LCD bias voltage. The op amp provides buffering and gain to the resistor-divider network made by the potentiometer (Figure 9) or to a fixed resistor and a variable resistor (see Figure 10).

Programmable Filter

Figure 11 shows the configuration for a 1st-order programmable filter. The gain of the filter is adjusted by R2, and the cutoff frequency is adjusted by R3. Use the following equations to calculate the gain (G) and the 3dB cutoff frequency (f_C):

$$G = 1 + \frac{R1}{R2}$$

$$f_C = \frac{1}{2\pi \times R3 \times C}$$

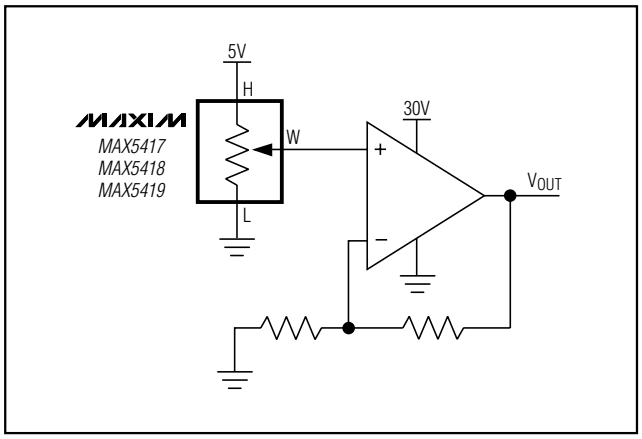

Figure 9. Positive LCD Bias Control Using a Voltage-Divider

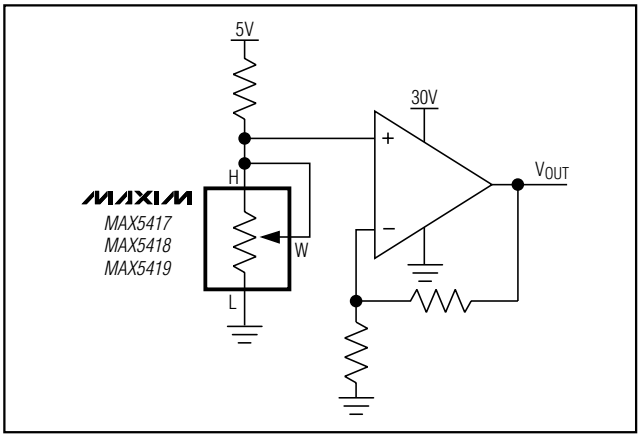

Figure 10. Positive LCD Bias Control Using a Variable Resistor

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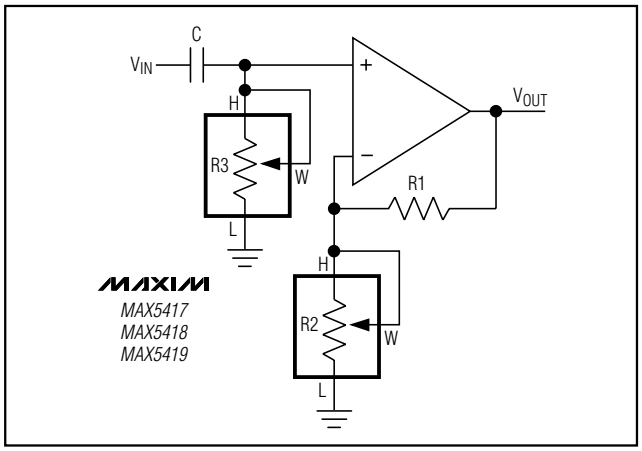


Figure 11. Programmable Filter

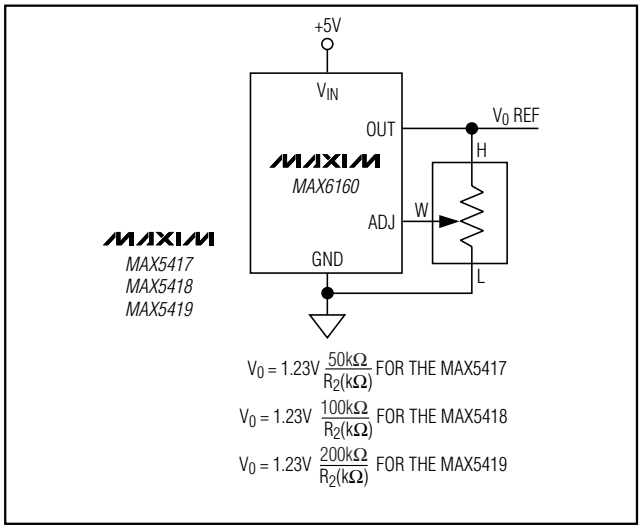


Figure 12. Adjustable Voltage Reference

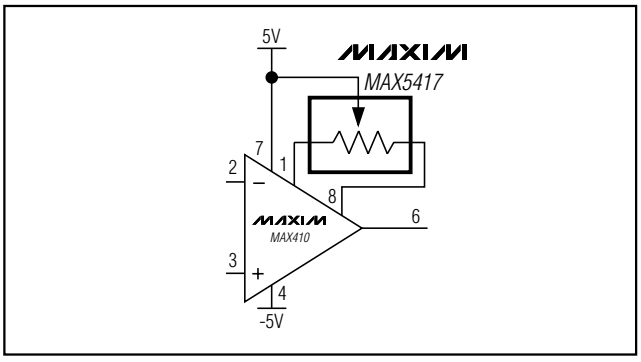
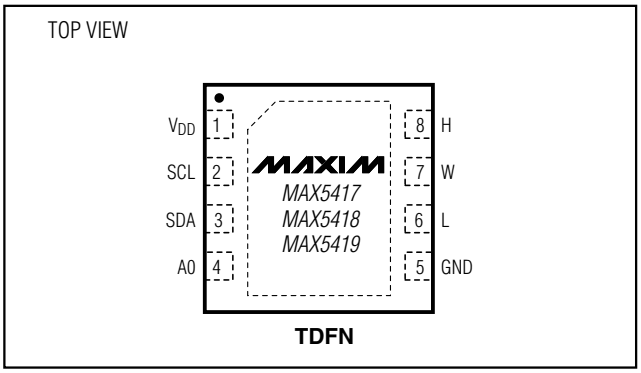


Figure 13. Offset Voltage Adjustment Circuit

Pin Configuration



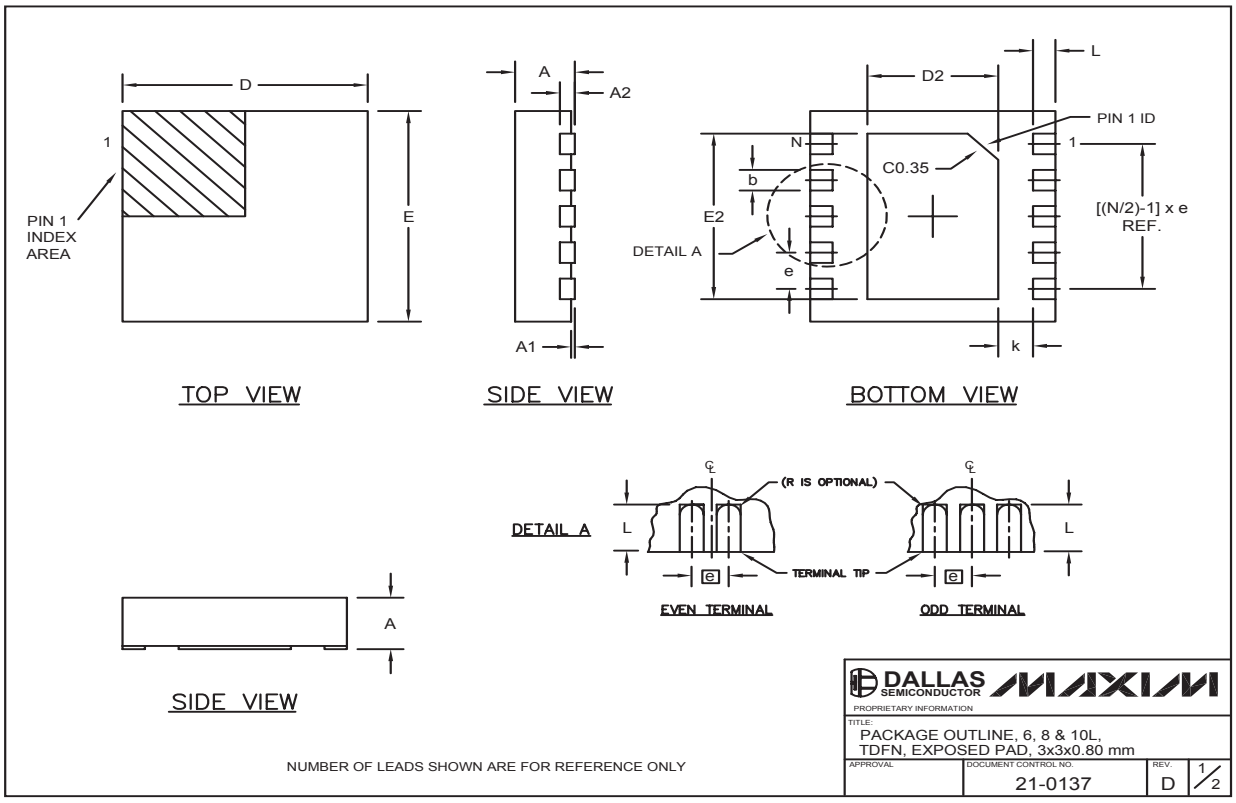
Chip Information

TRANSISTOR COUNT: 4637

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2".
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 6, 8 & 10L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	D	2/2