



ELECTRONICS, INC.
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NTE7030 Integrated Circuit Module, AF PO, 50W, Dual Power Supply

Features:

- Small-Sized Package Allows Audio Sets to be made Slimmer
- Facilitates Thermal Design of Slim Stereo Sets
- Constant-Current Circuit Minimizes Pop Noise During Power ON/OFF
- Possible to Design Electronic Supplementary Circuits:
 - Pop Noise Muting During Power ON/OFF
 - Load Short-Circuit Protector
 - Thermal Shutdown

Absolute Maximum Ratings: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Maximum Supply Voltage, V_{CCmax}	±52V
Junction Temperature, T_J	+150°C
Operating Case Temperature, T_C	+125°C
Storage Temperature Range, T_{stg}	-30° to +125°C
Thermal Resistance, Junction-to-Case, R_{thJC}	1.8°C/W
Available Time for Load Shorted ($V_{CC} = \pm 35V$, $R_L = 8\Omega$, $f = 50\text{Hz}$, $P_O = 50W$), t_s	2sec

Recommended Operating Conditions: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Recommended Supply Voltage, V_{CC}	±35V
Load Resistance, R_L	8Ω

Electrical Characteristics: ($T_A = +25^\circ\text{C}$, $V_{CC} = \pm 35V$, $R_L = 8\Omega$ (Non-Inductive Load), $R_g = 600\Omega$, $V_G = 40\text{dB}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current	I_{CCO}	$V_{CC} = \pm 42V$	10	20	50	mA
Output Power	P_O	THD = 0.4%, $f = 20\text{Hz}$ to 20kHz	50	–	–	W
		$V_{CC} = \pm 31V$, THD = 1%, $R_L = 4\Omega$, $f = 1\text{kHz}$	55	–	–	W
Total Harmonic Distortion	THD	$P_O = 1W$, $f = 1\text{kHz}$	–	–	0.3	%
Frequency Response	f_L, f_H	$P_O = 1W$ +0dB, -3dB	20 to 50k			Hz
Input Resistance	r_i	$P_O = 1W$, $f = 1\text{kHz}$	–	55	–	kΩ
Output Noise Voltage	V_{NO}	$V_{CC} = \pm 42V$, $R_g = 10\text{k}\Omega$, Note 2	–	–	1.2	mV _{rms}
Middle-Point Voltage	V_N	$V_{CC} = \pm 42V$	-70	0	+70	mV

Note 1. For power supply at the time of test, use a constant-voltage power supply unless otherwise specified.

Note 2. The output noise voltage represents the peak value on the RMS scale (V_{TMV}) of average value indicating type. The noise voltage waveform includes no flicker noise.

Pin Connection Diagram
(Front View)

15	Bootstrap
14	(+) V _{CC}
13	Output
12	(-) V _{CC}
11	Compensation
10	I Adjust
9	Emitter Bypass
8	Compensation
7	I Adjust
6	Test Point
5	Bypass
4	Bias
3	Substrate
2	NFB
1	Input

