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6-Channel Audio Processor IC **PT2322**

DESCRIPTION

PT2322 is a 6-Channel Audio Processor IC utilizing CMOS Technology specially designed for audio applications. 6-channel individual input, 6-channel master volume control, 6-channel individual volume trim control, 3-band tone control (treble, middle, and bass), mute function, 3D effect function, tone defeat function are all built into a single chip having the highest performance and reliability with the least components. Furthermore, the pin assignments and application circuit are optimized for easy PCB Layout and cost saving benefits. Housed in 28 pins, DIP or SOP, PT2322 is the ultimate answer to your every audio system needs.

FEATURES

- Very low power consumption (DC=9V)
- I^2C bus control
- 6-channel individual input
- 6-channel master volume control: 0 to -79dB (1dB/step)
- 6-channel individual output TRIM volume control: 0 to -15dB (1dB/step)
- 3-band tone control (Treble, Middle, Bass): ±14dB, 2dB/step
- Mute function
- 3D effect function
- Tone defeat function
- Low noise
- High channel separation
- Low harmonic distortion
- Least external components
- Easy to use
- Available in 28 Pins, DIP or SOP

APPLICATIONS

- Audio/Video system
- Multi-media speakers
- TV system
- PC audio
- AC3 amplifier system

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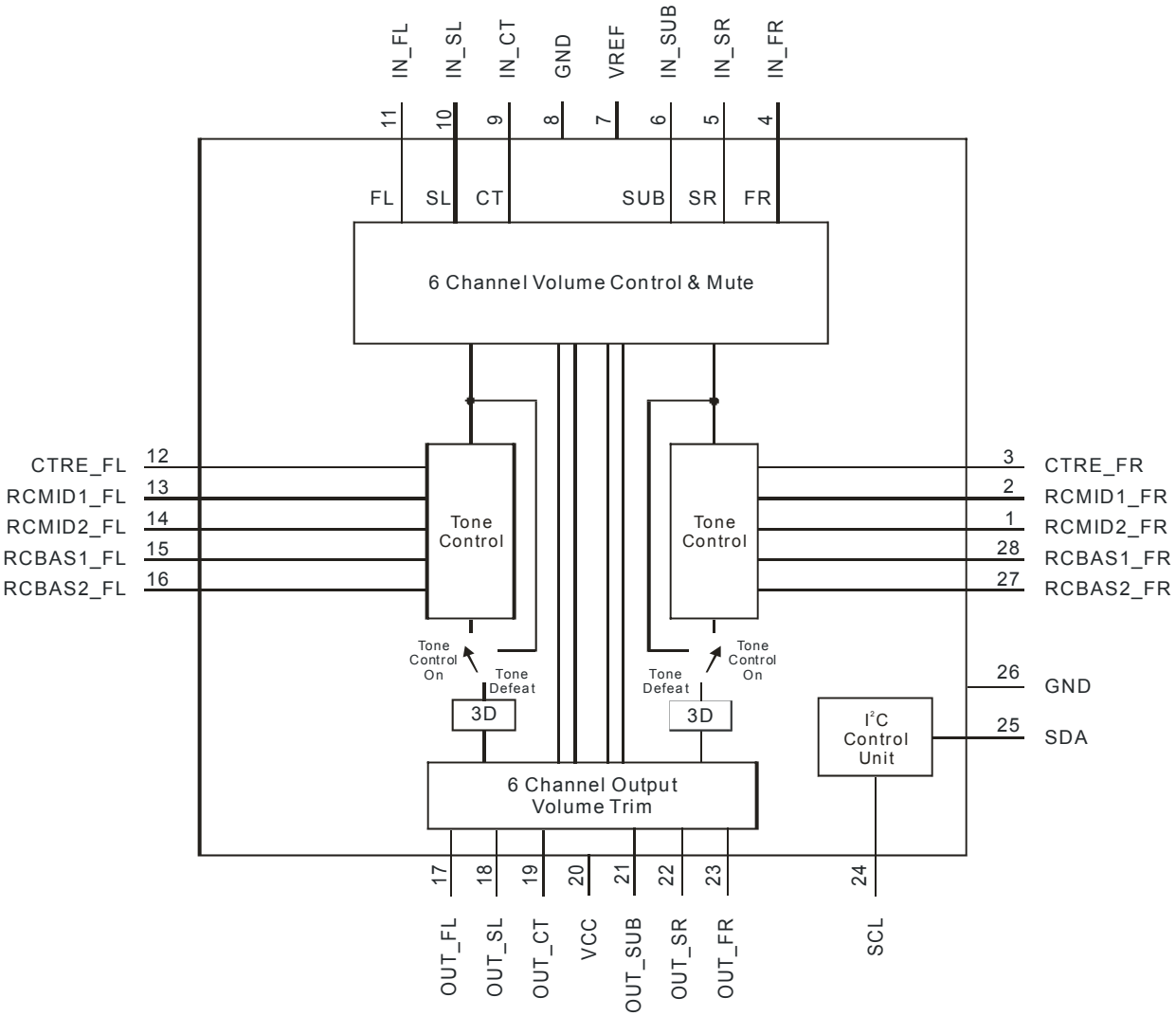
BLOCK DIAGRAM



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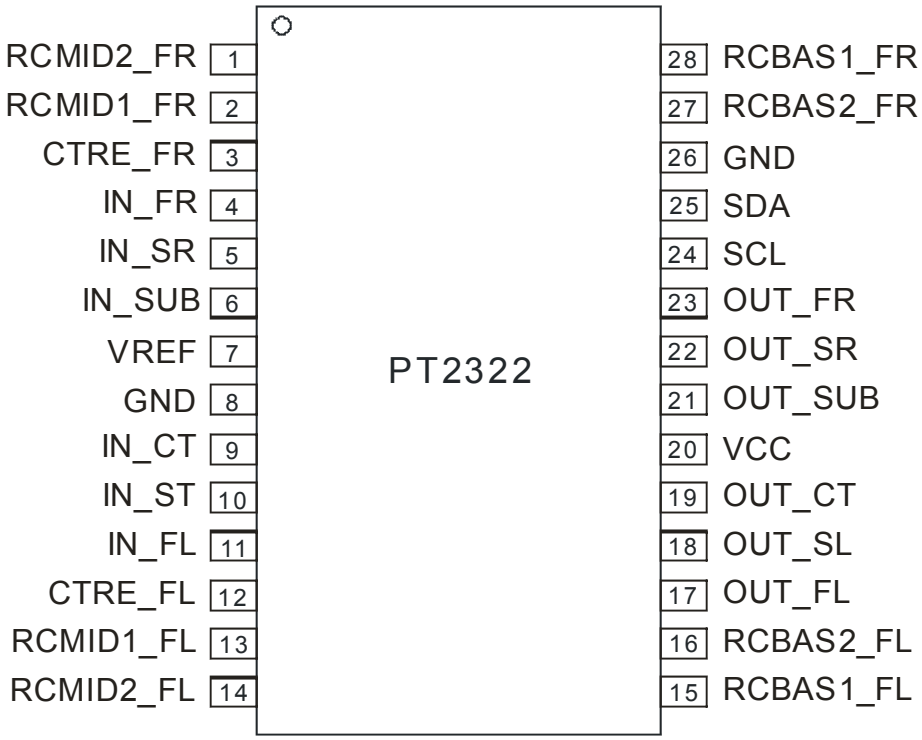
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
RCMID2_FR	-	Right channel tone component pin	1
RCMID1_FR	-	Right channel tone component pin	2
CTRE_FR	-	Right channel tone component pin	3
IN_R1	I	Front right input pin	4
IN_SR	I	Rear right channel input pin	5
IN_SUB	I	Subwoofer channel input pin	6
VREF	O	Reference voltage	7
GND	-	Ground	8, 26
IN_CT	I	Center channel input pin	9
IN_SL	I	Rear left channel input pin	10
IN_FL	I	Front left channel input pin	11
CTRE_FL	-	Left channel tone component pin	12
RCMID1_FL	-	Left channel tone component pin	13
RCMID2_FL	-	Left channel tone component pin	14
RCBAS1_FL	-	Left channel tone component pin	15
RCBAS2_FL	-	Left channel tone component pin	16
OUT_FL	O	Front left channel output pin	17
OUT_SL	O	Rear left channel output pin	18
OUT_CT	O	Center output channel pin	19
VCC	-	Positive power supply	20
OUT_SUB	O	Subwoofer channel output pin	21
OUT_SR	O	Rear right channel output pin	22
OUT_FR	O	Front rear channel output pin	23
SCL	I	I^2C control bus clock input	24
SDA	I	I^2C control bus data input pin	25
RCBAS2_FR	-	Right channel tone component pin	27
RCBAS1_FR	-	Right channel tone component pin	28

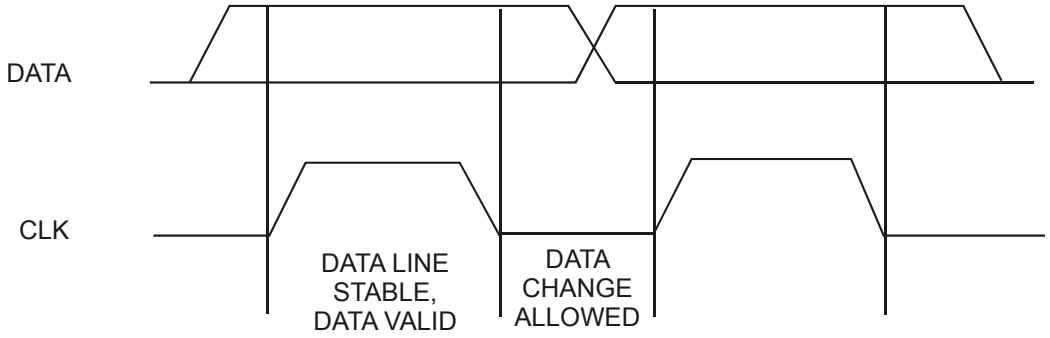
FUNCTION DESCRIPTION

I²C BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2322 via the SDA and SCL. The SDA and SCL make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW States of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

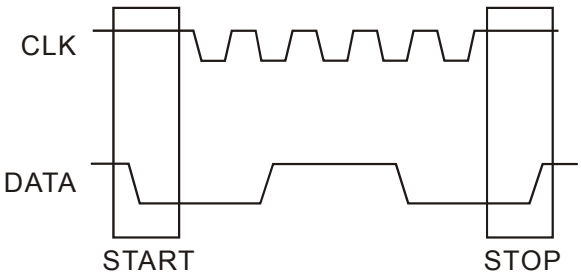
A Start Condition is activated when

1. the SCL is set to HIGH and
2. SDA shifts from HIGH to LOW State.

The Stop Condition is activated when

1. SCL is set to HIGH and
2. SDA shifts from LOW to HIGH State.

Please refer to the timing diagram below.

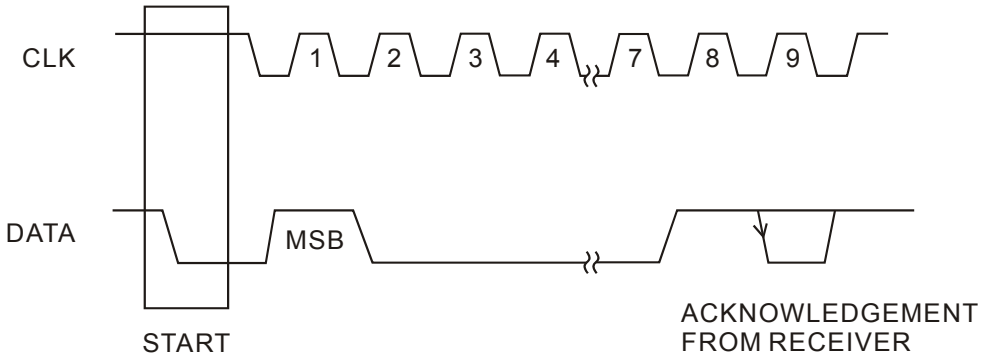


BYTE FORMAT

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the SDA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge Clock Pulse so that the SDA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below. The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.



TRANSMISSION WITHOUT ACKNOWLEDGE

If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

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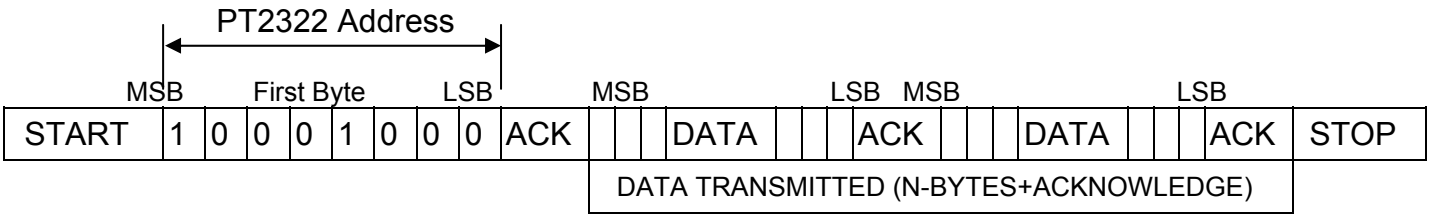
INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start Condition
- A Chip Address Byte including the PT2322 address. The 8th Bit of the Byte must be"0". PT2322 must always acknowledge the end of each transmitted byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition

Please refer to the diagram below:



Notes:
1. ACK=ACKNOWLEDGE
2. Max. Clock Speed=100K BITS/S

SOFTWARE SPECIFICATION

PT2322 Address is shown below.

1 MSB	0	0	0	1	0	0	0 LSB

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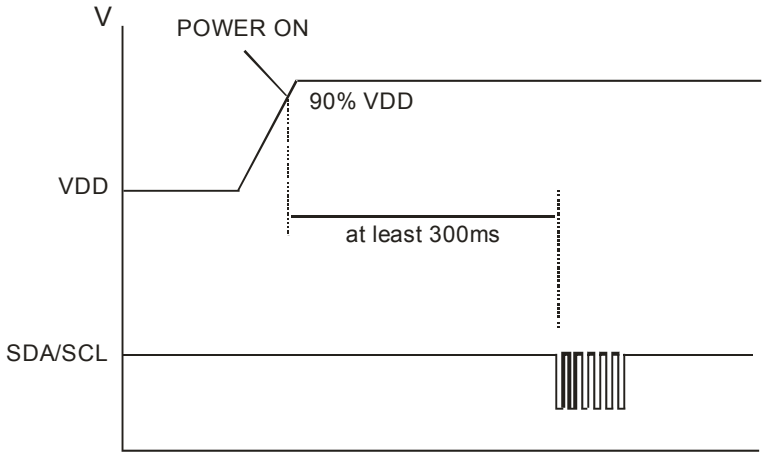
I²C BUS START-UP TIME

After Power is turned ON, PT2322 needs to wait for a short time in order to insure stability. This waiting period is relative to the value of Cref. As the Cref value becomes bigger, the waiting time period for PT2322 to be able to send I²C Bus Signal effectively becomes longer.

For example, if Cref=10μF, after power is turned ON, the waiting time period for PT2322 to send I²C Bus Signal is at least 300ms. If the waiting time period is less than 300ms, I²C Control may fail. Please refer to the diagram below.



FUNCTION DEFINITION

MSB							LSB	Function
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	x	x	x	x	No function
0	0	0	1	E3	E2	E1	E0	Front left channel volume TRIM control
0	0	1	0	E3	E2	E1	E0	Front right channel volume TRIM control
0	0	1	1	E3	E2	E1	E0	Center channel volume TRIM control
0	1	0	0	E3	E2	E1	E0	Rear left channel volume TRIM control
0	1	0	1	E3	E2	E1	E0	Rear right channel volume TRIM control
0	1	1	0	E3	E2	E1	E0	Subwoofer volume TRIM control
0	1	1	1	I1	I0	J1	J0	Function select
1	0	0	0	x	x	x	x	No function
1	0	0	1	G3	G2	G1	G0	Bass tone control
1	0	1	0	K3	K2	K1	K0	Middle tone control
1	0	1	1	H3	H2	H1	H0	Treble tone control
1	1	0	0	0	C2	C1	C0	Input SW
1	1	0	1	A3	A2	A1	A0	Master volume control (-1dB Step)
1	1	1	0	0	B2	B1	B0	Master volume control (-10dB Step)
1	1	1	1	1	1	1	1	

FUNCTION SELECT BITS

I1=0	Mute Off	I1=1	Mute On
I0=0	3D On	I0=1	3D Off
J1=0	Tone Control ON	J1=1	TONE Defeat
J0=0	No Function	J0=1	No Function

INPUT SWITCH

After power is turned ON, PT2322 must send a Code - “11000111” (C7H) - to activate Input SW.

MASTER VOLUME CONTROL BITS

A3	A2(B2)	A1(B1)	A0(B0)	Attenuation (dB)
0	0	0	0	0 (0)
0	0	0	1	-1 (-10)
0	0	1	0	-2 (-20)
0	0	1	1	-3 (-30)
0	1	0	0	-4 (-40)
0	1	0	1	-5 (-50)
0	1	1	0	-6 (-60)
0	1	1	1	-7 (-70)
1	0	0	0	-8 (x)
1	0	0	1	-9 (x)

Note: A=-1dB/Step, B=-10dB/Step

TONE CONTROL BITS

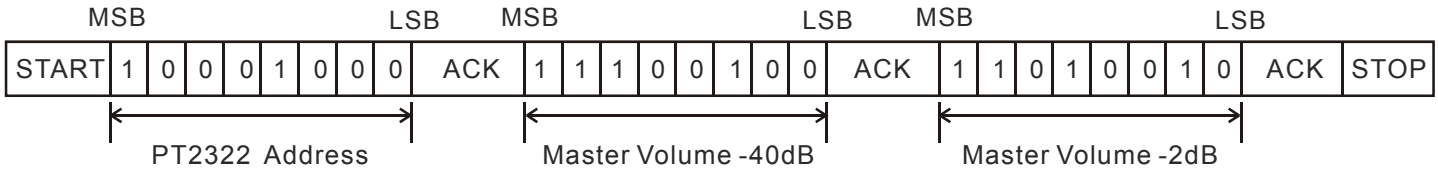
G3/K3/H3	G2/K2/H2	G1/K1/H1	G0/K0/H0	Attenuation (dB)
0	0	0	0	-14
0	0	0	1	-12
0	0	1	0	-10
0	0	1	1	-8
0	1	0	0	-6
0	1	0	1	-4
0	1	1	0	-2
0	1	1	1	0
1	0	0	0	+14
1	0	0	1	+12
1	0	1	0	+10
1	0	1	1	+8
1	1	0	0	+6
1	1	0	1	+4
1	1	1	0	+2
1	1	1	1	0

Note: G=Bass, K=Middle, H=Treble

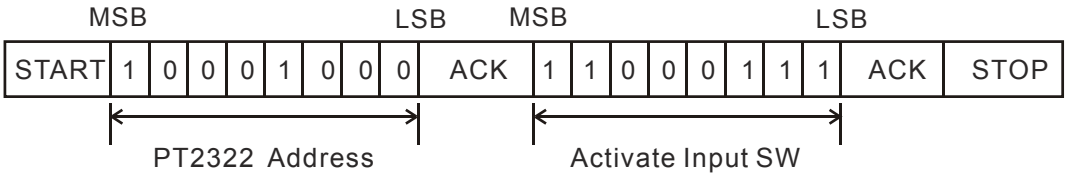
CHANNEL TRIM VOLUME CONTROL BITS

E3	E2	E1	E0	Attenuation (dB)
0	0	0	0	0
0	0	0	1	-1
0	0	1	0	-2
0	0	1	1	-3
0	1	0	0	-4
0	1	0	1	-5
0	1	1	0	-6
0	1	1	1	-7
1	0	0	0	-8
1	0	0	1	-9
1	0	1	0	-10
1	0	1	1	-11
1	1	0	0	-12
1	1	0	1	-13
1	1	1	0	-14
1	1	1	1	-15

For example, if we set the Master Volume Control to -42dB, the data string will be:



After Power is turned on, PT2322 must send a code – 11000111 (C7H) to activate input SW.



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PT2322 PROGRAMMING PROCEDURE

1. In order to ensure exact operation under any operating voltage, it is recommended an instruction to clear REGISTER “FFH” must be transmitted first, then sending a code “C7H” to activate input SW. Please refer to the following diagram.

Start	1	0	0	0	1	0	0	0	Ack	1	1	1	1	1	1	1	1	Ack	Stop
					PT2322 Address														
													Clear Register						

2. The PT2322 function register does not have any default settings. After clearing the register, an initial value must send in order to each register, If a register does has not been set, it is possible cause no sound will be output.

Start	1	0	0	0	1	0	0	0	Ack	1	1	0	0	0	1	1	1	Ack	Stop
					PT2322 Address														
													6 Channel Input						

3. When adjusting the volume of PT2322, it is necessary to send a multiple of 10dB followed by a 1dB code to the attenuator in sequence. If this sequence is not followed, or if only a 10dB or 1dB value is sent, the IC may not operate normally. Please refer to the diagram below.

Master volume setting of -42dB：

Start	1	0	0	0	1	0	0	0	Ack	1	1	1	0	0	1	0	0	ACK	1	1	0	1	0	0	1	0	Ack	Stop
					PT2322 Address								-40dB										-2dB					

Start	1	0	0	0	1	0	0	0	Ack	1	1	0	1	0	0	1	0	Ack	1	1	1	0	0	1	0	0	ACK	Stop
					PT2322 Address								-2dB										-40dB					

The two methods shown above are both acceptable.

Warning! The following transmission method is not permitted.

Send only 10dB attenuation value

Start	1	0	0	0	1	0	0	0	Ack	1	1	1	0	0	1	0	0	ACK	Stop
					PT2322 Address									-40dB					

Send only 1dB attenuation value

Start	1	0	0	0	1	0	0	0	Ack	1	1	0	1	0	0	1	0	ACK	Stop
					PT2322 Address									-2dB					

Do not send a 10dB code without simultaneously with a 1dB code or in combination with other instruction codes.

Start	1	0	0	0	1	0	0	0	Ack	1	1	0	1	0	0	1	0	Ack	1	0	1	1	1	1	1	0	ACK	1	1	1	0	0	1	0	0	ACK	Stop
								PT2322 Address						-2dB										Treble+2dB										-40dB				

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ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Ratings	Unit
Operating supply voltage	Vs	15	V
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstg	-65 ~ +150	℃

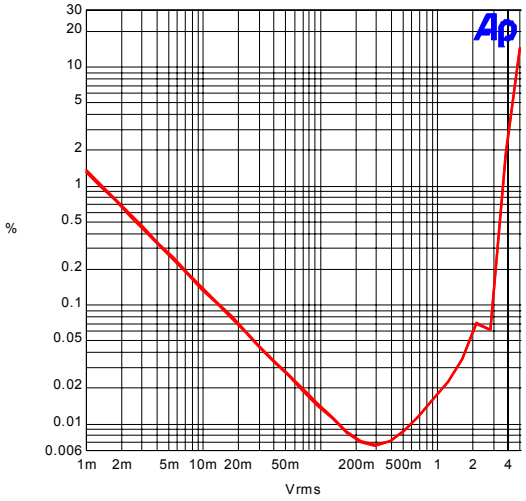
ELECTRONICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, VDD=12V, R_L=47KΩ, Rg=20Ω, all volume and tone=0dB, F=1KHz)

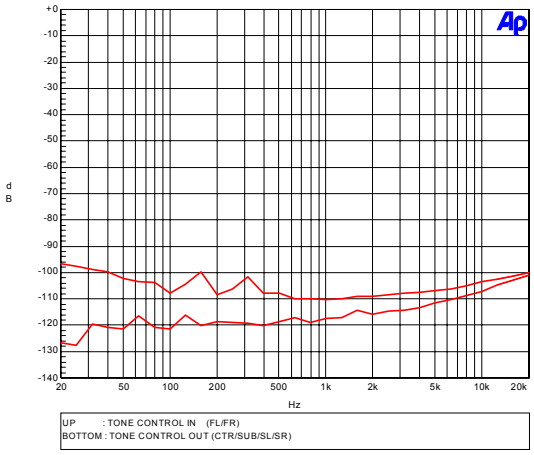
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
Supply voltage	VDD		5		12	V
Supply current	IS		25	35	40	mA
Main Volume						
Input impedance	RIN	FL, FR, CENTER, SUB, SL, SR	35	50	65	KΩ
MAX input level	VCL	Volume=0dB,THD=1%		4		Vrms
Channel separation	SC		100	107		dB
Input SW separation	SIN	BW=22~22KHz	85	90		dB
Control range	Crange			79		dB
Min. attenuation	Avmin			0		dB
Max. attenuation	Avmax			-79		dB
Step resolution	Astep			1		dB
Step drift	EA	Volume=0~-50dB	-1.5	0	+1.5	dB
Channel level balance	GERR	Volume=0~-50dB	-1.5	0	+1.5	dB
Individual Volume Trim						
Control range	Crange			15		dB
Min. attenuation	Avmin			0		dB
Max. attenuation	Avmax			-15		dB
Step resolution	Sstep			1		dB
Step drift	EA		-1	0	+1	dB
Channel level balance	GERR	Volume=0~-15dB	-1	0	+1	dB
Mute						
Output mute	AMUTE	A-weighting	77	90		dB

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Tone Control						
Treble						
Control range	Gt	Boost/Cut	±12	±14	±16	dB
Resolution	Tstep			2		dB
Midrange						
Control range	Gm	Boost/Cut	±12	±14	±16	dB
Resolution	Mstep			2		dB
Bass						
Control range	Gb	Boost/Cut	±12	±14	±16	dB
Resolution	Bstep			2		dB
6CH Audio Output						
Total harmonics distortion	THD	Volume=0dB, INPUT=0.2Vrms	0.005	0.007	0.01	%
Noise output	Noise	FL/FR A-weighting, ONE=0dB		13	18	μV
		SL, SR, CTR, SUB CH A-weighting		7	10	μV
Signal to noise ratio	S/N	0dB=1Vrms, A-weighting	95	98	105	dBV
Output resistance	Ro	Vout=1Vrms		300	400	Ω
Volume gain	Go		-1	0	+1	dB
Max. output level	VOMAX	FL/FR CH THD=1%	3.3	3.5	3.8	Vrms
		SL, SR, CTR, SUB CH, THD=1%	3.6	3.8	3.9	
Recommended min. load	RLoad		10			KΩ
I^2C Bus						
Input low level	VIL		0		2	V
Input high level	VIH		3.5		VDD	V
Bus initial time	TINIT	Cref=10μF		250	300	ms

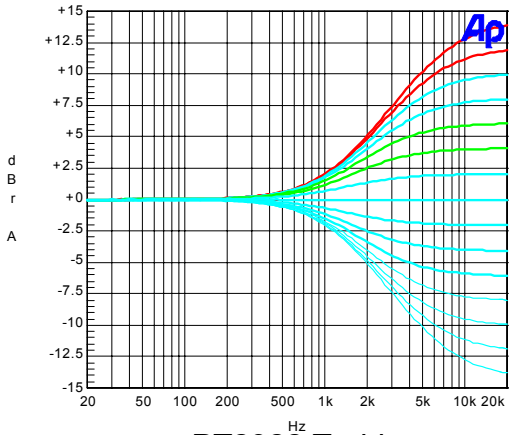
PT2322 ELECTRICAL CHARACTERISTICS CHART



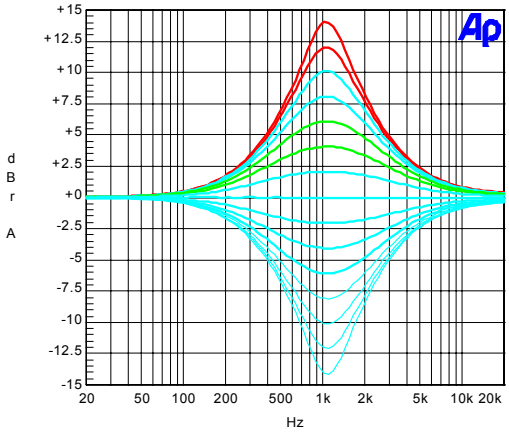
THD vs Output Level



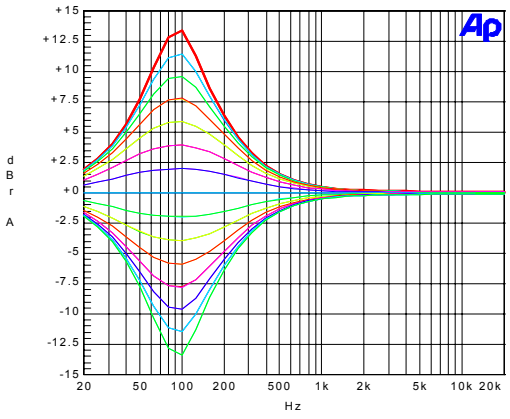
L/R Channel Separation



PT2322 Treble

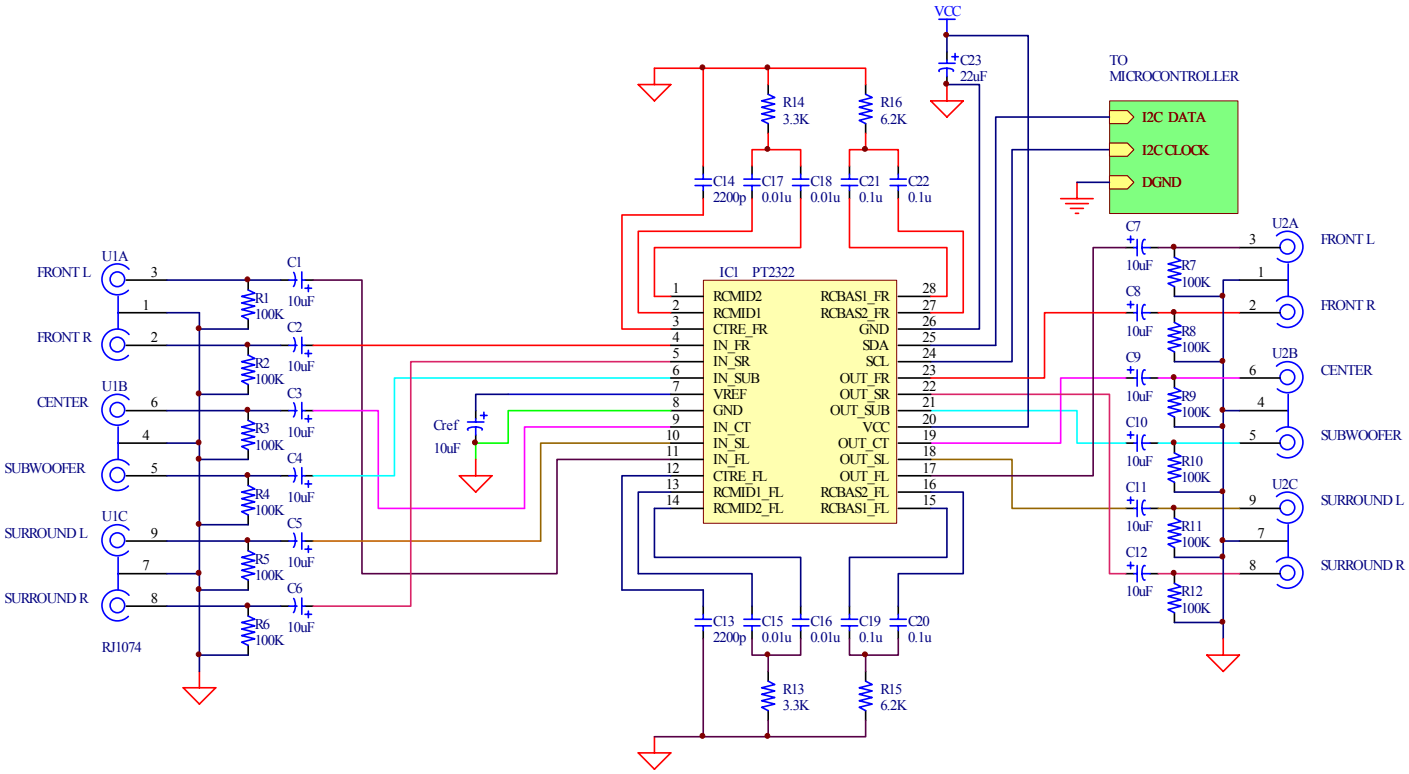


PT2322 Midrange



PT2322 Bass

APPLICATION CIRCUIT



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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2322	28 Pins, DIP, 600mil	PT2322
PT2322-S	28 Pins, SOP, 330mil	PT2322-S
PT2322 (L)	28 Pins, DIP, 600mil	PT2322
PT2322-S (L)	28 Pins, SOP, 330mil	PT2322-S

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

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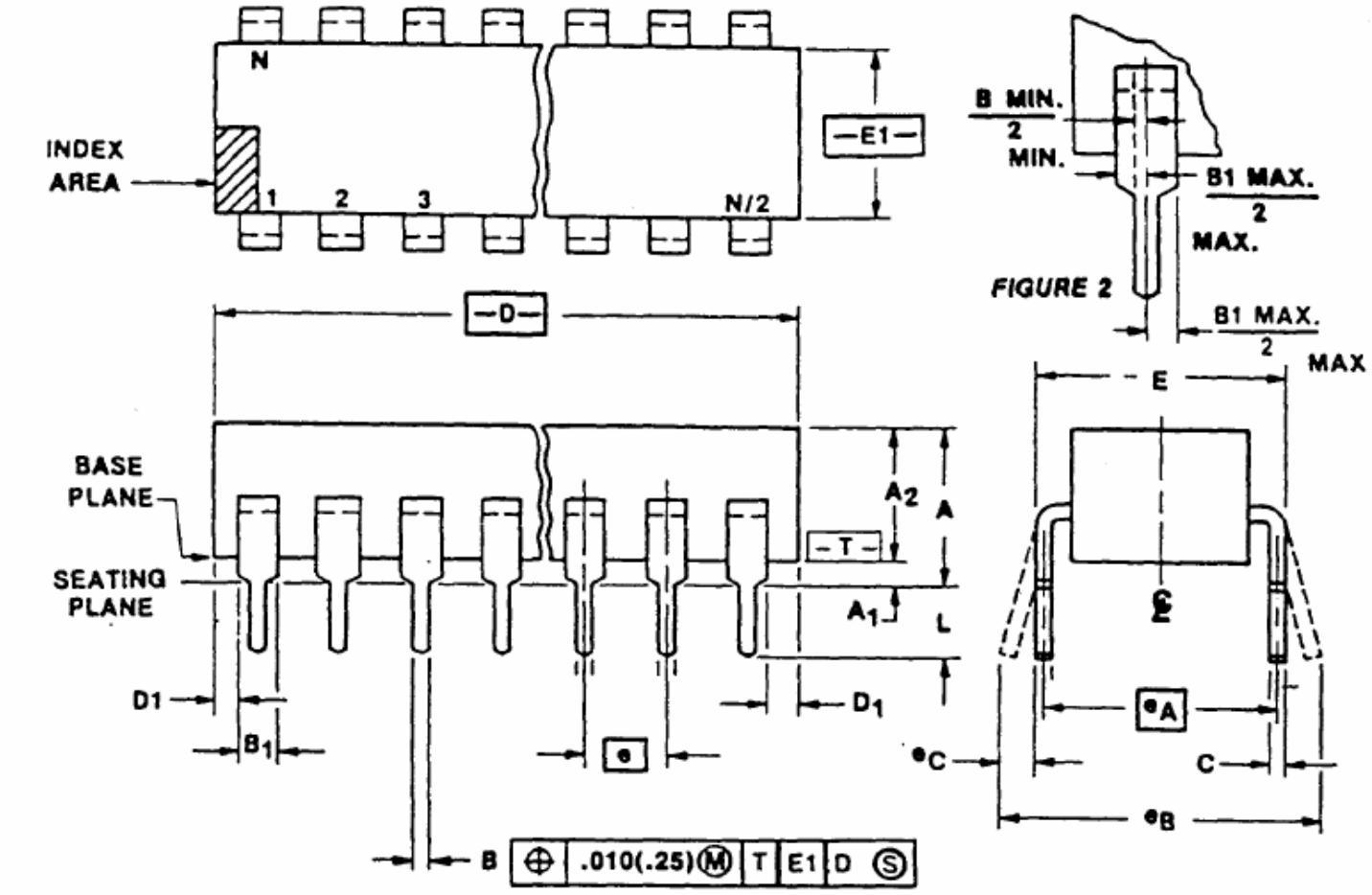
PACKAGE INFORMATION

28 PINS, DIP, 600MIL

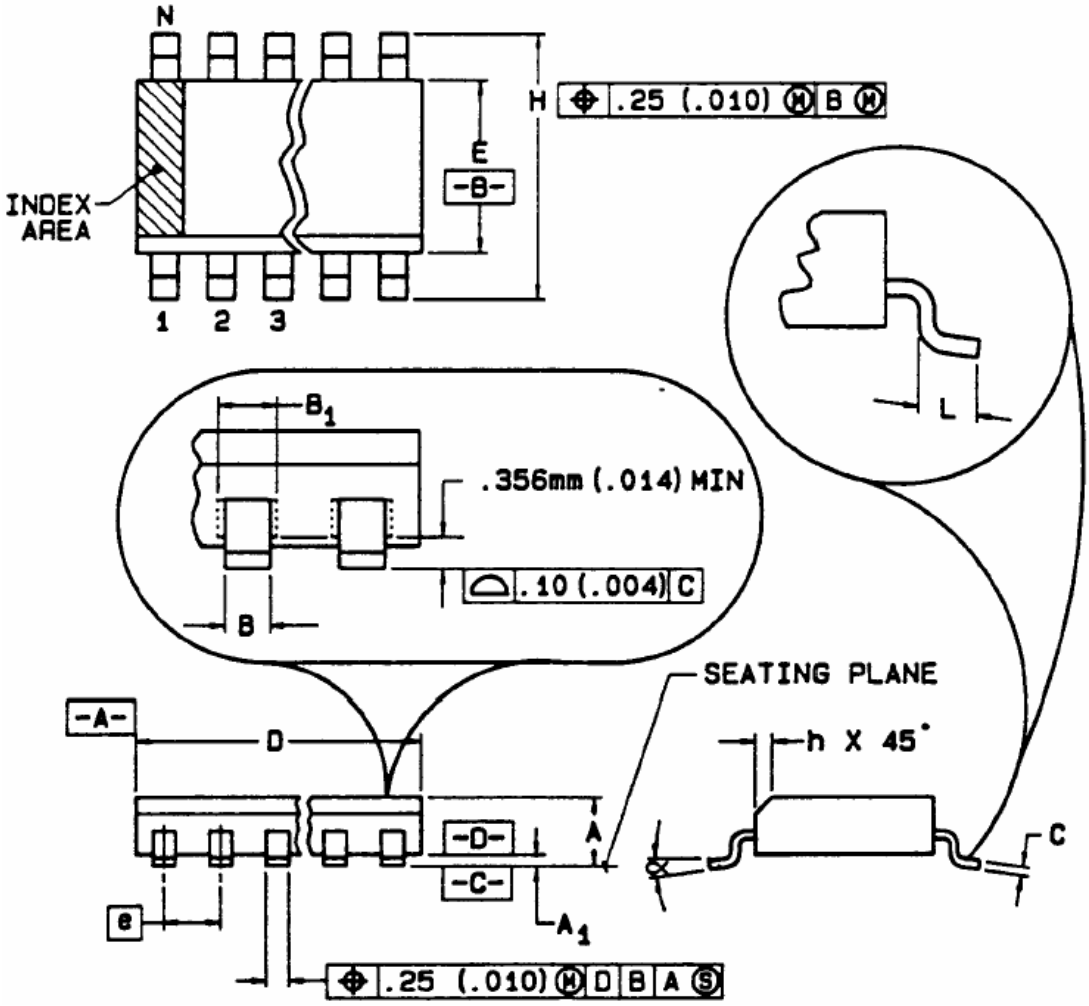


Symbol	Min.	Nom.	Max.
A	-	-	6.35
A1	0.39	-	-
A2	3.18	-	4.95
B	0.356	-	0.558
B1	0.77	-	1.77
C	0.204	-	0.381
D	35.1	--	39.7
D1	0.13	-	-
E	15.24	-	15.87
E1	12.32	-	14.73
e	2.54 BSC.		
eA	15.24 BSC.		
eB	-	-	17.78
L	2.93	-	5.08

Notes:
1. Controlling dimension: MILLIMETER
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D” & “E1” dimensions, for ceramic packages, include allowance for glass overrun and meniscus and lid to base mismatch.
5. “D” & “E1” dimensions for plastic package, do not includes mold flash or protrusion. Mold flash or protrusions shall Not exceed 0.01 inch. (0.25mm).
6. “E” and “eA” measured with the leads constrained to be perpendicular to plane T.
7. “eB” and “eC” are measured at the lead tips with the loads un-constrained. “eC” must be zero or greater.
8. “N” is the maximum quantity of lead positions. (N=28)
9. Corner leads (1, N, N/2, and N/2+1) may be configured as shown in Figure 2.
10. Pointed our rounded leads tips are preferred to ease insertion.
11. For automatic insertion, any rained irregularity on the top surface (step, mess, etc.) shall b symmetrical about the lateral and longitudinal package centerlines.
12. Refer JEDEC MS-011 Variation AB.

JEDEC is the trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.

28 PINS, SOP, 330MIL



Symbol	Min.	Nom.	Max.
A	2.55	-	3.05
A1	0.05	-	0.35
B	0.35	-	0.50
B1	0.35	-	0.609
C	0.14	-	0.32
D	17.70	-	18.50
E	8.23	-	8.90
e	1.27 BSC.		
H	11.50	-	12.70
h	0.25	-	0.75
L	0.40	-	1.27
θ	0°		8°

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. “D” is a reference datum.
3. “A” and “B” are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of terminal for soldering to a substrate.
6. N is the number of the terminal positions (N=28)
7. A transition in lead width from B to B1 is not required. A transition in lead width can occur below 0.356mm (0.014 inch) from the seating plane if the resulting lead width falls within B.
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MO-059 Variation AD

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