TDA2075A

STEREO CLASS-T DIGITAL AUDIO AMPLIFIER DRIVER USING DIGITAL POWER PROCESSING™ TECHNOLOGY

Preliminary Information **Revision 0.9 – October 2005**

GENERAL DESCRIPTION

The TDA2075A is a two-channel, amplifier driver, that uses Tripath's proprietary Digital Power Processing (DPP™) technology. The TDA2075A offers higher integration over previous Tripath amplifiers driver chipsets while providing exceptional audio performance for real world applications. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

The TDA2075A is typically configured as a split-supply, single-ended, stereo amplifier. The TDA2075A can also be configured single-supply, single-ended, stereo amplifier, via external component choice. For applications that require bridged output drive, please refer to the TDA1400.

Applications

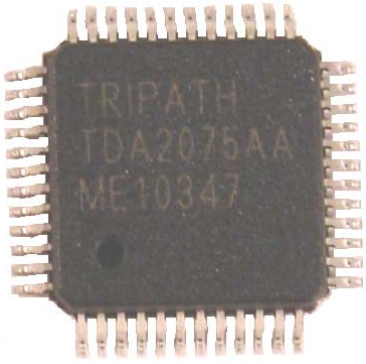
- Powered DVD Players
- Mini-Compo Systems
- Audio/Video Amplifiers & Receivers
- Multimedia Speakers

Benefits

- Reduced system cost with smaller/less expensive power supply and heat sink
- Signal fidelity equal to high quality Class-AB amplifiers
- High dynamic range compatible with digital media such as CD and DVD

Features

- Class-T architecture with proprietary DPP
- "Audiophile" Sound Quality
- Full Audio Bandwidth, 20Hz to 20kHz
- High Efficiency
- Supports wide range of output power levels and output loads by changing supply voltage and external Mosfets
- Compatible with unregulated power supplies
- Output over-current protection
- Over- and under-voltage protection
- Over-temperature protection
- 48-Pin LQFP Package



Absolute Maximum Ratings (Note 1)

SYMBOL	PARAMETER	Value	UNITS
V5	5V Power Supply	6	V
V_{logic}	Input logic level	V5 + 0.3	V
V10	10V Power Supply	12	V
T_{STORE}	Storage Temperature Range	-55º to 150º	°C
VPP, VNN	Supply Voltage (Note 5)	+/-70	V
T_A	Operating Free-air Temperature Range	-40º to 85º	°C
T_J	Junction Temperature	150º	°C
ESD_{HB}	ESD Susceptibility – Human Body Model (Note 2) All pins	2000	V
ESD_{MM}	ESD Susceptibility – Machine Model (Note 3) All pins	200	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. See the table below for Operating Conditions.
Note 2: Human body model, 100pF discharged through a 1.5KΩ resistor.
Note 3: Machine model, 220pF – 240pF discharged through all pins.

Operating Conditions (Note 4)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V5	5V Power Supply	4.5	5	5.5	V
V10	10V Power Supply	9	10	11	V
T_A	Operating Temperature Range	-40	25	85	°C
VPP	Positive Supply Voltage (note 5)	15		65	V
VNN	Negative Supply Voltage (note 5)	-15		-65	V

Note 4: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.
Note 5: The supply limitation is based on the internal over-current detection circuit. This limitation is subject to additional characterization. In addition, depending on feedback configuration, the TDA2075A can be used in single-supply applications, in which case, the negative supply, VNN, is not needed.

Thermal Characteristics

SYMBOL	PARAMETER	Value	UNITS
θ_{JA}	Junction-to-ambient Thermal Resistance (still air)	TBD	C/W

Electrical Characteristics TDA2075A (Note 6)

T_A = 25 °C. See Application/Test Circuit on page 7. Unless otherwise noted, the supply voltages are V5=5V, V10=10V, and VPP=|VNN|=40V.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
I_{5Q}	Quiescent Current (Mute = 0V)			50		mA
I_{10Q}	Quiescent Current (Mute = 0V)	FETs: FQP13N10, FQP12P10 R_{BBM} = 20.0kΩ		60		mA
I_{VPPQ}	Quiescent Current (Mute = 0V)	FETs: FQP13N10, FQP12P10 R_{BBM} = 20.0kΩ		40		mA
I_{VNNQ}	Quiescent Current (Mute = 0V)	FETs: FQP13N10, FQP12P10 R_{BBM} = 20.0kΩ		40		mA
I_{5MUTE}	Mute Supply Current (Mute = 5V)			50		mA
V_{TOC}	Over Current Sense Voltage Threshold	+/-5V Common Mode Voltage +/-40V Common Mode Voltage	TBD TBD	0.55 0.55	TBD TBD	V
$I_{VPPSENSE}$	VPPSENSE Threshold Currents	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 TBD TBD	138 135 55 52	TBD TBD 	µA µA µA µA
$V_{VPPSENSE}$	Threshold Voltages with R_{VPP1} = R_{VPP2} = 402KΩ (Note 7)	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 TBD TBD	55.5 54.3 22.1 20.9	TBD TBD 	V V V V
$I_{VNNSENSE}$	VNNSENSE Threshold Currents	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 TBD TBD	138 135 51 48	TBD TBD 	µA µA µA µA
$V_{VNNSENSE}$	Threshold Voltages with R_{VNN1} = 402KΩ R_{VNN2} = 1.2MΩ (Note 7)	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 TBD TBD	55.5 54.3 20.5 19.3	TBD TBD 	V V V V

Note 6: Minimum and maximum limits are guaranteed but may not be 100% tested.

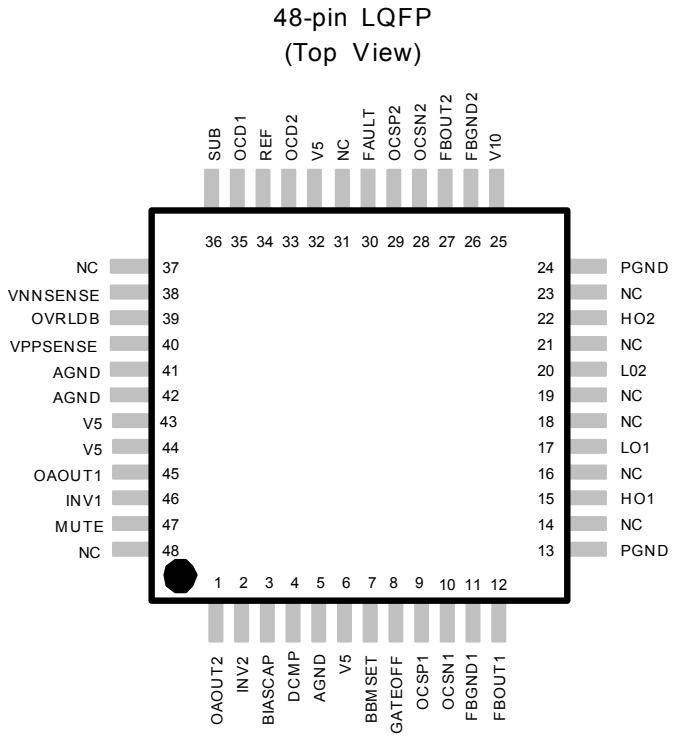
Note 7: These supply voltages are calculated using the $I_{VPPSENSE}$ and $I_{VNNSENSE}$ values shown in the Electrical Characteristics table. The typical voltage values shown are calculated using a R_{VPP} and R_{VNN} values without any tolerance variation. The minimum and maximum voltage limits shown include either a +1% or –1% (+1% for Over-voltage turn on and Under-voltage turn off, -1% for Over-voltage turn off and Under-voltage turn on) variation of R_{VPP} or R_{VNN} off the nominal 402kohm and 1.2Mohm values. These voltage specifications are examples to show both typical and worst case voltage ranges for the given R_{VPP} and R_{VNN} resistor values. Please refer to the Application Information section for a more detailed description of how to calculate the over and under voltage trip voltages for a given resistor value.

Performance Characteristics

T_A = 25 °C. Unless otherwise noted, the supply voltages are V5 = 5V, V10 = 10V, and VPP = |VNN| = 40V, the input frequency is 1kHz and the measurement bandwidth is 20kHz. See Application/Test Circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_{OUT}	Output Power (continuous output)	THD+N = 0.1%, R_L = 4Ω THD+N = 1%, R_L = 4Ω THD+N = 10%, R_L = 4Ω THD+N = 0.1%, R_L = 6Ω THD+N = 1%, R_L = 6Ω THD+N = 10%, R_L = 6Ω THD+N = 0.1%, R_L = 8Ω THD+N = 1%, R_L = 8Ω THD+N = 10%, R_L = 8Ω		145 160 200 105 115 150 80 90 115		W W W W W W W W W
THD + N	Total Harmonic Distortion Plus Noise	P_{OUT} = 60W, R_L = 8Ω		0.01		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), R_L = 8Ω P_{OUT} = 25W/Channel		0.03		%
SNR	Signal-to-Noise Ratio	A Weighted, R_L = 4Ω, P_{OUT} = 200W/Channel		104.4		dB
η	Power Efficiency	P_{OUT} = 115W/Channel, R_L = 8Ω		92		%
A_V	Amplifier Gain	P_{OUT} = 10W/Channel, R_L = 8Ω See Application / Test Circuit		20.09		V/V
A_{VERROR}	Channel to Channel Gain Error	P_{OUT} = 10W/Channel, R_L = 8Ω See Application / Test Circuit			0.5	dB
e_{NOUT}	Output Noise Voltage	A-Weighted, input shorted R_{FBC} = 10kΩ, R_{FBB} = 1.1kΩ, and R_{FBA} = 1.0kΩ		170		μV
V_{OFFSET}	Output Offset Voltage	No Load, Mute = Logic Low 1% R_{FBA}, R_{FBB} and R_{FBC} resistors	-1.0		1.0	V

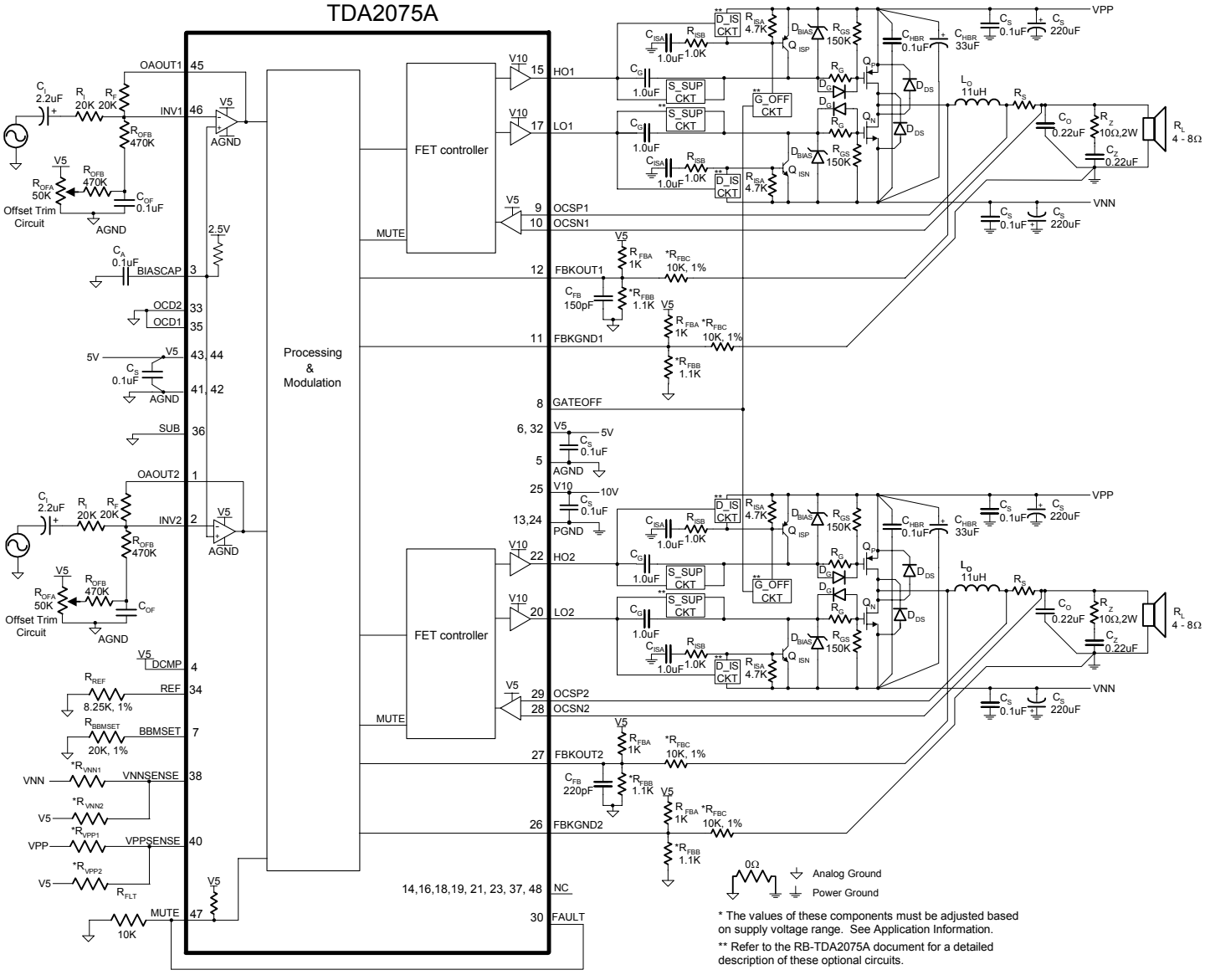
TDA2075A Pinout



Pin Description

Pin	Function	Description
1	OAOUT2	Output of inverting-input stage (Channel 2)
2	INV2	Negative input of inverting op-amp with 2.5VDC of bias (Channel 2)
3	BIASCAP	Bandgap reference times two (typically 2.5VDC). Used to set the common mode voltage for the input op amps. This pin is not capable of driving external circuitry.
4	DCMP	Internal mode selection. This pin must be connected to 0V or 5V for proper device operation. Typically, this pin is connected to V5.
5	AGND	Analog Ground
6	V5	5 Volt power supply input.
7	BBMSET	Break-before-make timing control to prevent shoot-through in the output MOSFETs. Please refer to the Application Information for additional information.
8	GATEOFF	10V under-voltage fault pin (requires pull-up resistor)
9, 10	OCSP1, OCSN1	Over-current detect pins (Channel 1)
11	FBKGND1	Ground Kelvin feedback (Channel 1)
12	FBKOUT1	Negative switching feedback (Channel 1)
13	PGND	Power Ground
15	HO1	High side gate drive output (Channel 1)
17	L01	Low side gate drive output (Channel 1)
20	LO2	Low side gate drive output (Channel 2)
22	HO2	High side gate drive output (Channel 2)
24	PGND	Power Ground
25	V10	10 Volt power supply input. Used for gate drive circuitry.
26	FBKGND2	Ground Kelvin feedback (Channel 2)
27	FBKOUT2	Negative switching feedback (Channel 2)
28, 29	OCSN2, OCSP2	Over-current detect pins (Channel 2)
30	FAULT	A logic high output indicates an under-voltage (5V or 10V), over-current or over-temperature condition (requires pull-down resistor).
32	V5	5 Volt power supply input.
33	OCD2	Over-Current Detect pin (Channel 2). This pin must be connected to AGND for proper device operation.
34	REF	Internal bandgap reference voltage; approximately 1.0 VDC.
35	OCD1	Over-Current Detect pin (Channel 1). This pin must be connected to AGND for proper device operation.
36	SUB	Substrate (connect to AGND)
38	VNNSENSE	Negative supply voltage sense input. This pin is used for both over and under voltage sensing for the VNN supply.
39	OVRLDB	A logic low output indicates the input signal has overloaded the amplifier.
40	VPPSENSE	Positive supply voltage sense input. This pin is used for both over and under voltage sensing for the VPP supply.
41	AGND	Analog Ground
42	AGND	Analog Ground
43	V5	5 Volt power supply input.
44	V5	5 Volt power supply input.
45	OAOUT1	Output of inverting-input stage (Channel 1)
46	INV1	Negative input of inverting op-amp with 2.5VDC of bias (Channel 1)
47	MUTE	When set to logic high, both channels are in idle mode. When low (grounded), both channels are fully operational (connect to FAULT pin).
14,16,18, 19,21,23, 31,37,48	NC	Not Connected internally. These pins may be grounded or left floating on the PCB layout.

Application / Test Circuit



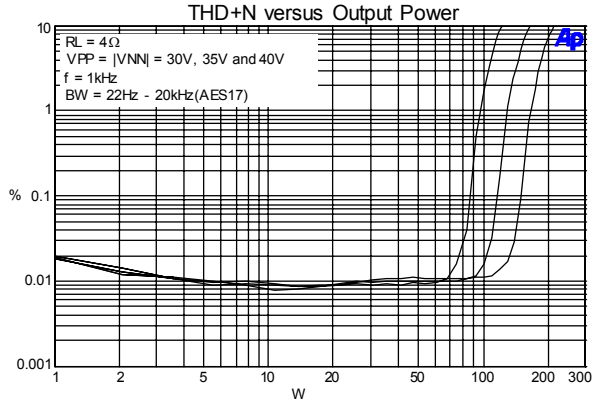
External Components Description (Refer to the Application/Test Circuit)

Components	Description
R_I	Inverting input resistance to provide AC gain in conjunction with R_F. This input is biased at the BIASCAP voltage (approximately 2.5VDC).
R_F	Feedback resistor to set AC gain in conjunction with R_I. Please refer to the Amplifier Gain paragraph, in the Application Information section.
C_I	AC input coupling capacitor which, in conjunction with R_I, forms a high-pass filter at $f_C = 1/(2\pi R_I C_I)$.
R_{FBA}	Feedback divider resistor connected to V5. This value of this resistor depends on the supply voltage setting and helps set the TDA2075A gain in conjunction with R_I, R_F, R_{FBA}, and R_{FBC}. Please see the Modulator Feedback Design paragraphs in the Application Information Section.
R_{FBB}	Feedback divider resistor connected to AGND. This value of this resistor depends on the supply voltage setting and helps set the TDA2075A gain in conjunction with R_I, R_F, R_{FBA}, and R_{FBC}. Please see the Modulator Feedback Design paragraphs in the Application Information Section.
R_{FBC}	Feedback resistor connected from either the OUT1 (OUT2) to FBKOUT1 (FBKOUT2) or PGND1 (PGND2) to FBKGND1 (FBKGND2). The value of this resistor depends on the supply voltage setting and helps set the TDA2075A gain in conjunction with R_I, R_F, R_{FBA}, and R_{FBB}. It should be noted that R_{FBC} must have a power rating of greater than $P_{DISS} = VPP^2/(2R_{FBC})$. Please see the Modulator Feedback Design paragraphs in the Application Information Section.
C_{FB}	Feedback delay capacitor that both lowers the idle switching frequency and filters very high frequency noise from the feedback signal, which improves amplifier performance. The value of C_{FB} should be different for channel 1 and channel 2 to minimize noise coupling between the channels. Please refer to the Application / Test Circuit.
R_{OFA}	Potentiometer used to manually trim the DC offset on the output of the TDA2075A.
R_{OFB}	Resistor that limits the DC offset trim range and allows for precise adjustment.
C_{OF}	Capacitor that filters the manual DC offset trim voltage.
R_{REF}	Bias resistor. Locate close to pin 34 and ground to plane with a low impedance connection to pins 41 and 42.
R_{BBMSET}	Bias current setting resistor for the BBM setting. Locate close to pin 7 and ground directly to pin 5. See Application Information on how to determine the value for R_{BBM}.
C_A	BIASCAP decoupling capacitor. Locate close to pin 3 and ground to plane with a low impedance connection to pins 41 and 42.
C_S	Supply decoupling capacitor for the power pins. For optimum performance, these components should be located close to the TDA2075A and returned to their respective ground as shown in the Application Circuit.
R_{VNN1}	Main overvoltage and undervoltage sense resistor for the negative supply (VNN). Please refer to the Electrical Characteristics Section for the trip points as well as the hysteresis band. Also, please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection. When using a single power supply, this circuit can be defeated by connecting a 16KΩ resistor to AGND.
R_{VNN2}	Secondary overvoltage and undervoltage sense resistor for the negative supply (VNN). This resistor accounts for the internal $V_{NNSENSE}$ bias of 1.25V. Nominal resistor value should be three times that of R_{VNN1}. Please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection. When using a single power supply, omit R_{VNN2}.
R_{VPP1}	Main overvoltage and undervoltage sense resistor for the positive supply (VPP). Please refer to the Electrical Characteristics Section for the trip points as well as the hysteresis band. Also, please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection.
R_{VPP2}	Secondary overvoltage and undervoltage sense resistor for the positive supply

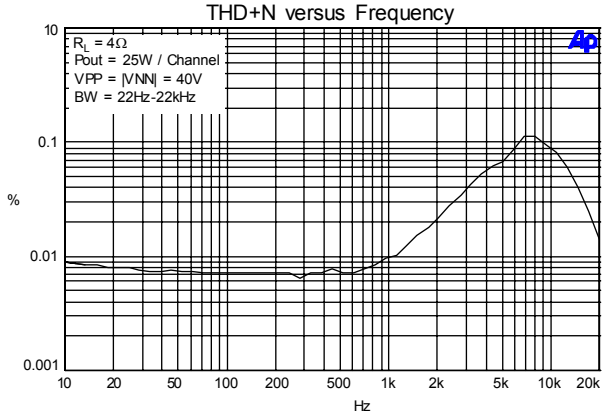
	(VPP). This resistor accounts for the internal $V_{PPSENSE}$ bias of 2.5V. Nominal resistor value should be equal to that of R_{VPP1}. Please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection.
R_S	Over-current sense resistor. Please refer to the section, Setting the Over-current Threshold, in the Application Information for a discussion of how to choose the value of R_S to obtain a specific current limit trip point.
C_{HBR}	Supply decoupling for the high current Half-bridge supply pins. These components must be located as close to the output MOSFETs as possible to minimize output ringing which causes power supply overshoot. By reducing overshoot, these capacitors maximize both the TDA2075A and output MOSFET reliability. These capacitors should have good high frequency performance including low ESR and low ESL. In addition, the capacitor rating must be twice the maximum VPP voltage. Panasonic EB capacitors are ideal for the bulk storage (nominally 33uF) due to their high ripple current and high frequency design.
R_G	Gate resistor, which is used to control the MOSFET rise/ fall times. This resistor serves to dampen the parasitics at the MOSFET gates, which, in turn, minimizes ringing and output overshoots. The typical power rating is 1/2 watt.
D_G	Gate diode, which adds additional BBM and serves to match the unequal rise and fall times of Q_N and Q_P. An ultra-fast diode with a current rating of at least 200mA should be used.
D_{BIAS}	Diode that keeps the gate capacitor biased at the proper voltage when the supply voltage decreases.
C_G	Gate capacitor that ac-couples the TDA2075A from the high voltage MOSFETs.
$R_{ISA,}$ R_{ISB}	Bias resistors for the increasing supply circuits.
C_{ISA}	Bias capacitor for the increasing supply circuits.
Q_{ISP}	P-channel bipolar transistor for the circuit which charges the high side gate capacitors, C_G, to VPP, in the case where the VPP supply increases in magnitude.
Q_{ISN}	N-channel bipolar transistor for the circuit which charges the low side gate capacitors, C_G, to VNN, in the case where the VNN supply increases in magnitude.
C_Z	Zobel capacitor, which in conjunction with R_Z, terminates the output filter at high frequencies. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs.
Q_P	P-channel power-MOSFET of the output stage.
Q_N	N-channel power-MOSFET of the output stage.
R_Z	Zobel resistor, which in conjunction with C_Z, terminates the output filter at high frequencies. The combination of R_Z and C_Z minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with increasing frequency. Depending on the program material, the power rating of R_Z may need to be adjusted. The typical power rating is 2 watts.
L_O	Output inductor, which in conjunction with C_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$.
C_O	Output capacitor, which, in conjunction with L_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order low-pass filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / 2\sqrt{L_O C_O}$. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs.
D_{DS}	These diodes must be connected from either the drain of the p-channel MOSFET to the source of the n-channel MOSFET, or the source of the p-channel MOSFET to the drain of the n-channel MOSFET. This diode absorbs any high frequency overshoots caused by the output inductor L_O during high output current conditions. In order for this diode to be effective it must be connected directly to the two MOSFETs. An ultra-fast recovery diode that can sustain the entire supply voltage should be used here. In most applications a 100V or greater diode must be used.
R_{GS}	Resistor that turns Q_N and Q_P off when no signal is present.
R_{FLT}	Pull-down resistor for the open-drain Fault circuit.

Typical Performance Characteristics

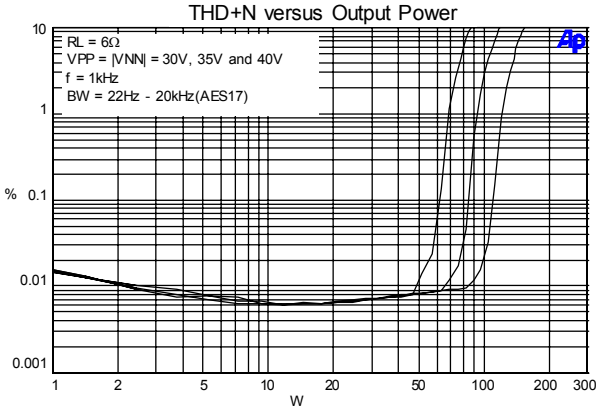
THD+N versus Output Power



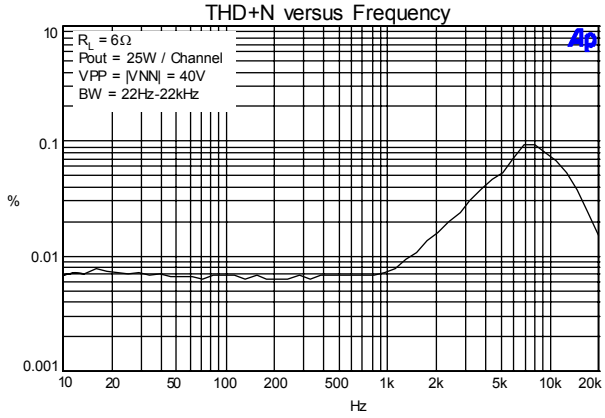
THD+N versus Frequency



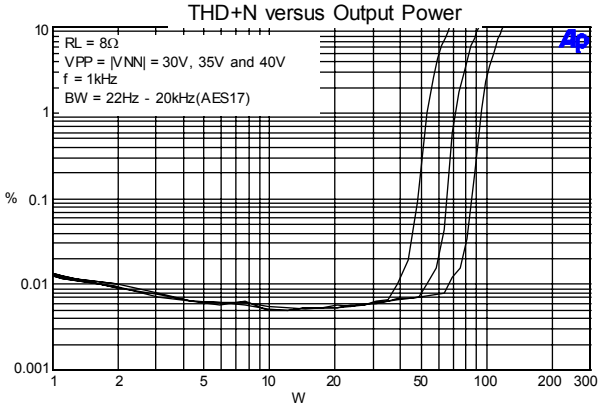
THD+N versus Output Power



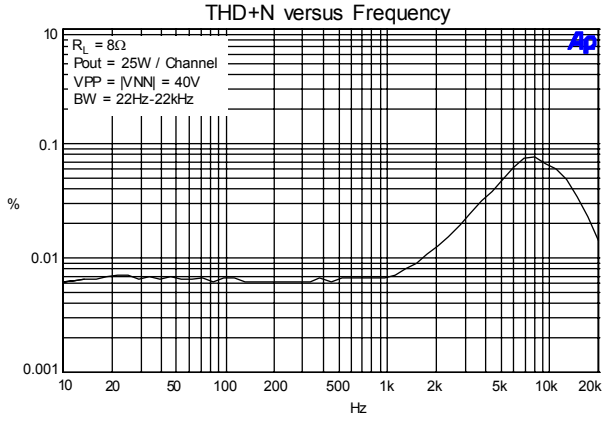
THD+N versus Frequency



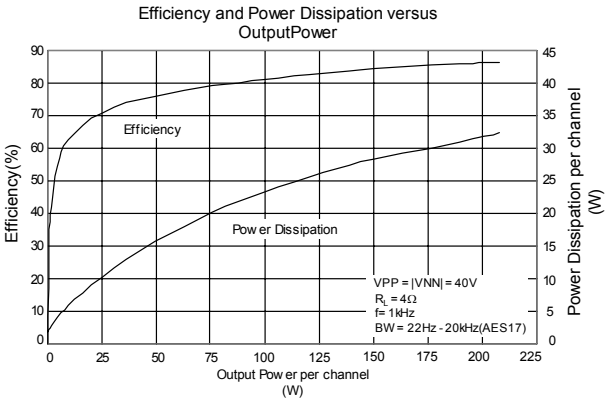
THD+N versus Output Power

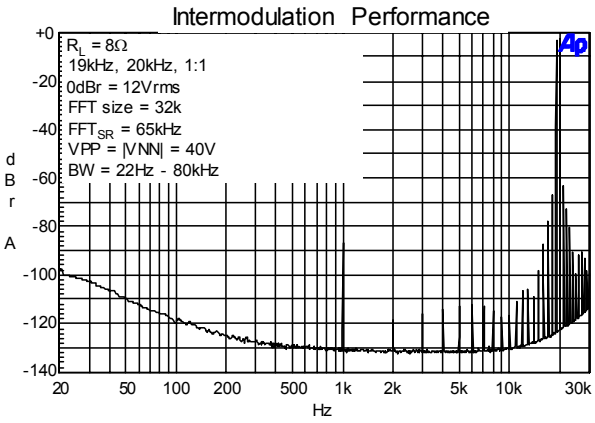


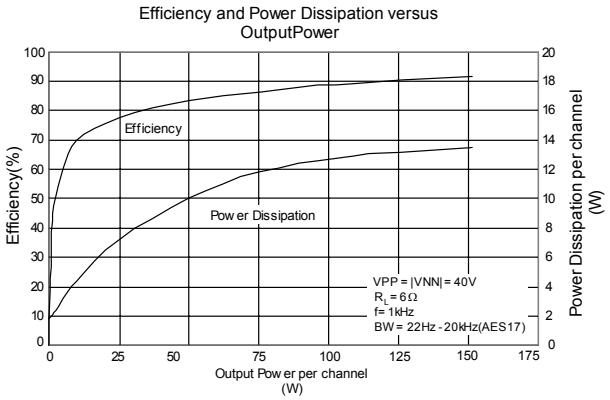
THD+N versus Frequency

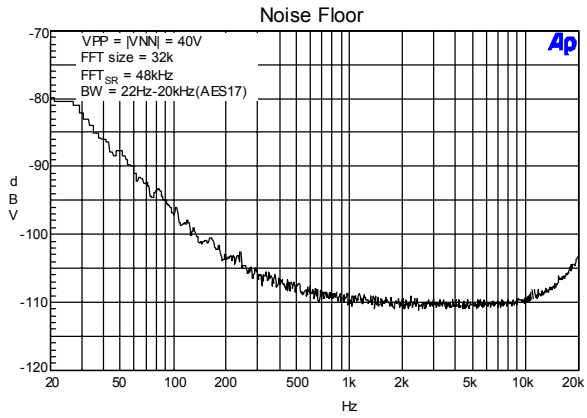


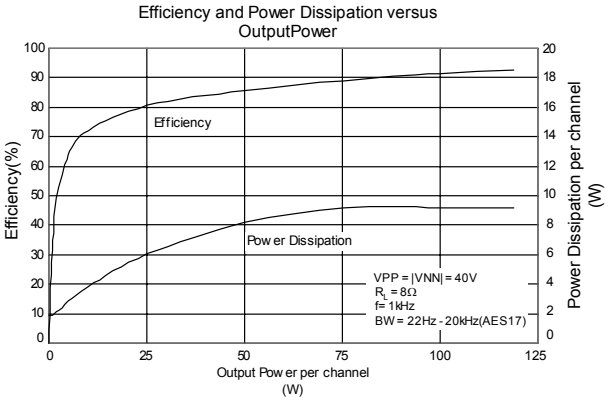
Typical Performance Characteristics

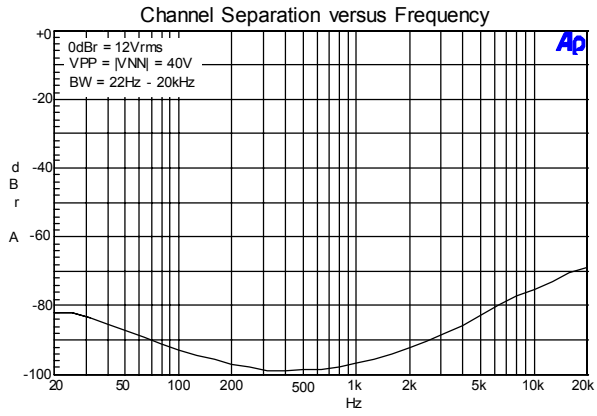












Application Information

Figure 1 is a simplified diagram of one channel (Channel 1) of a TDA2075A amplifier to assist in understanding its operation.

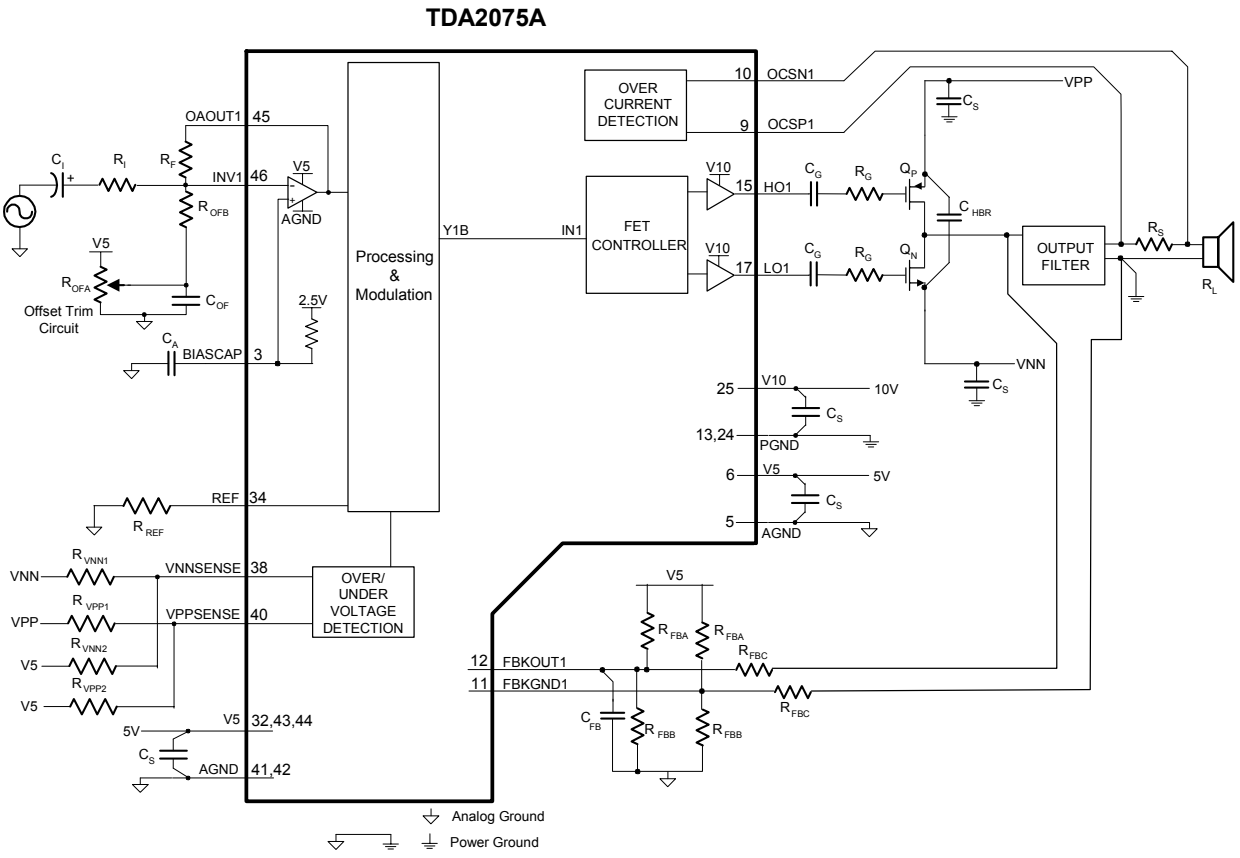


Figure 1: Simplified TDA2075A Amplifier

TDA2075A Basic Amplifier Operation

The audio input signal is fed to the processor internal to the TDA2075A, where a switching pattern is generated. The average idle (no input) switching frequency is approximately 700kHz. With an input signal, the pattern is spread spectrum and varies between approximately 200kHz and 1.5MHz depending on input signal level and frequency. These switching patterns are inputted to a MOSFET driver and then outputted to HO1 and LO1 which are ac-coupled to a complementary pair of power MOSFETs. The output of the MOSFETs is a power-amplified version of the switching pattern that switches between VPP and VNN. This signal is then low-pass filtered to obtain an amplified reproduction of the audio input signal.

The processor is operated from a 5-volt supply while the FET driver is operated from a 10-volt supply. The FET driver inserts a “break-before-make” dead time between the turn-off of one transistor and the turn-on of the other in order to minimize shoot-through currents in the external MOSFETs. The dead time can be programmed by adjusting R_{BBMSET}. Feedback information from the output of the complementary FETs is supplied to the processor via FBKOUT1. Additional feedback information to account for ground bounce is supplied via FBKGND1.

Complementary MOSFETs are used to formulate a half-bridge configuration for the power stage of the amplifier. The gate capacitors, C_G, are used to ac-couple the FET driver to the complementary MOSFETs. The gate resistors, R_G, are used to control MOSFET slew rate and thereby minimize voltage overshoots.

Circuit Board Layout

The TDA2075A is a power (high current) amplifier that operates at relatively high switching frequencies. The output of the amplifier switches between VPP and VNN at high speeds while driving large currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Since the amplifier must drive the inductive LC output filter and speaker loads, the amplifier outputs can be pulled above the supply voltage and below ground by the energy in the output inductance. To avoid subjecting the TDA2075A and the complementary MOSFETs to potentially damaging voltage stress, it is critical to have a good printed circuit board layout. It is recommended that Tripath's layout and application circuit be used for all applications and only be deviated from after careful analysis of the effects of any changes. Please refer to the TDA2075A reference board document, RB-TDA2075A, available on the Tripath website, at www.tripath.com.

The trace that connects the drain of the p-channel output MOSFET to the drain of the n-channel output MOSFET is very important. This connection should be as wide and short as possible. A jumper wire of 16 gauge or more can be used in parallel with the trace to reduce any trace resistance or inductance. Any resistance or inductance on this trace can cause the switching output to over/undershoot potentially causing damage to both the TDA2075A and the output MOSFETs.

The following components are important to place near the TDA2075A or output MOSFET pins. The recommendations are ranked in order of layout importance, either for proper device operation or performance considerations.

- The capacitors, $C_{HBR,}$ provide high frequency bypassing of the amplifier power supplies and will serve to reduce spikes across the supply rails. Please note that both MOSFET half-bridges must be decoupled separately. In addition, the voltage rating for C_{HBR} should be at least 150V as this capacitor is exposed to the full supply range, VPP-VNN.

- C_{FB} removes very high frequency components from the amplifier feedback signals and lowers the output switching frequency by delaying the feedback signals. In addition, the value of C_{FB} is different for channel 1 and channel 2 to keep the average switching frequency difference greater than 40kHz. This minimizes in-band audio noise. The capacitors, C_{FB}, should be surface mount types, located on the "solder" side of the board as close to their respective TDA2075A pins as possible.

- D_{DS} should be placed as close to the drain and source of the output MOSFETs as possible with direct routing either from the drain of the p-channel MOSFET to the source of the n-channel MOSFET or from the source of the p-channel MOSFET to the drain of the n-channel MOSFET. The output over/undershoots are very high-speed transients. If these diodes are placed too far away from the MOSFETs, they will be ineffective.

- To minimize noise pickup and minimize THD+N, R_{FBA}, R_{FBB}, and R_{FBC} should be located as close to the TDA2075A as possible. Make sure that the routing of the high voltage feedback lines is kept far away from the input op amps or significant noise coupling may occur. It is best to shield the high voltage feedback lines by using a ground plane around these traces as well as the input section. The feedback and feedback ground traces should be routed together in parallel.

- The main supply decoupling capacitors, C_S, should be located close to the output devices, Q_N and Q_P. These will absorb energy when D_{SD} and D_{DS} conduct. Also, the bulk decoupling capacitors, C_S, will shunt energy generated by the main supply lead trace inductance.

Some components are not sensitive to location but are very sensitive to layout and trace routing.

- For proper over-current detection, the sense lines connected to R_S must be kelvin connected directly from the terminals of R_S back to OCSP1 (OCSP2) and OCSN1 (OCSN2). The traces should be run in parallel back to the TDA2075A pins without deviation. Improper layout with respect to R_S will result in premature over-current detection due to additional IR losses.

- To maximize the damping factor and reduce distortion and noise, the modulator feedback connections should be routed directly to the pins of the output inductors. L_O.

- The output filter capacitor, C_O, and zobel capacitor, C_Z, should be star connected with the load return. The output ground feedback signal should be taken from this star point.

- The modulator feedback resistors, R_{FBA} and R_{FBB}, should all be grounded and attached to 5V together. These connections will serve to minimize common mode noise via the differential feedback.

- The feedback signals that come directly from the output inductors are high voltage and high frequency in nature. If they are routed close to the input nodes, INV1 and INV2, the high impedance inverting op-amp pins will pick up noise. This coupling will result in significant background noise, especially when the input is AC coupled to ground, or an external source such as a CD player or signal generator is connected. Thus, care should be taken such that the feedback lines are not routed near any of the input section.

- To minimize the possibility of any noise pickup, the trace lengths of INV1 and INV2 should be kept as short as possible. This is most easily accomplished by locating the input resistors, R_I and the input stage feedback resistors, R_F as close to the TDA2075A as possible. In addition, the offset trim resistor, R_{OFB}, which connects to either INV1, or INV2, should be located close to the TDA2075A input section.

TDA2075A Grounding

Proper grounding techniques are required to maximize TDA2075A functionality and performance. Parametric parameters such as THD+N, Noise Floor and Crosstalk can be adversely affected if proper grounding techniques are not implemented on the PCB layout. The following discussion highlights some recommendations about grounding both with respect to the TDA2075A as well as general “audio system” design rules.

The TDA2075A is divided into three sections: the input processor section, the FET driver section, and the complementary output MOSFETs (high voltage) section. On the TDA2075A evaluation board, the ground is also divided into distinct sections, Analog Ground (AGND) and Power Ground (PGND). To minimize ground loops and keep the audio noise floor as low as possible, the two grounds must be only connected at a single point.

The ground for the 5V supply is referred to as the analog ground and must be connected to pins 5, 41, and 42 on the TDA2075A. Additionally, any external input circuitry such as preamps, or active filters, should be referenced to the analog ground. The substrate, pin 36, should also be connected to the analog ground.

For the power section, Tripath has traditionally used a “star” grounding scheme. Thus, the load ground returns and the power supply decoupling traces are routed separately back to the power supply. In addition, any type of shield or chassis connection would be connected directly to the ground star located at the power supply. These precautions will both minimize audible noise and enhance the crosstalk performance of the TDA2075A. It is possible to use a low impedance ground plane for PGND as well. But the ground plane must be contiguous or ground currents from each channel can create crosstalk issues. To minimize these issues, the FBKOUT1 (FBKOUT2) lines should be routed directly from the PGND side of the load.

The TDA2075A incorporates a differential feedback system to minimize the effects of ground bounce and cancel out common mode ground noise. Therefore, the feedback from the output ground for each channel needs to be properly sensed. This can be accomplished by connecting the output ground “sensing” trace directly to the star formed by the output ground return, output capacitor, C_O, and the zobel capacitor, C_Z. Refer to the Application / Test Circuit for a schematic description.

TDA2075A Amplifier Gain

The gain of the TDA2075A is the product of the input stage gain and the modulator gain for the TDA2075A. Please refer to the sections, Input Stage Design, and Modulator Feedback Design, for a complete explanation of how to determine the external component values.

$$A_{V\ TDA2075A} = A_{V\ INPUTSTAGE} * A_{V\ MODULATOR}$$

$$A_{V\ TDA2075A} \approx -\frac{R_F}{R_I}\left(\frac{R_{FBC} * (R_{FBA} + R_{FBB})}{R_{FBA} * R_{FBB}} + 1\right)$$

For example, using a TDA2075A with the following external components,

R_I = 20kΩ
R_F = 20kΩ
R_{FBA} = 1kΩ
R_{FBB} = 1.1kΩ
R_{FBC} = 10.0kΩ

$$A_{V\ TDA2075A} \approx -\frac{20k\,\Omega}{20k\,\Omega}\left(\frac{10.0k\,\Omega * (1.0k\,\Omega + 1.1k\,\Omega)}{1.0k\,\Omega * 1.1k\,\Omega} + 1\right) = -20.09\ \frac{V}{V}$$

Input Stage Design

The TDA2075A input stage is configured as an inverting amplifier, allowing the system designer flexibility in setting the input stage gain and frequency response. Figure 2 shows a typical application where the input stage is a constant gain inverting amplifier. The input stage gain should be set so that the maximum input signal level will drive the input stage output to 4Vpp.

The gain of the input stage, above the low frequency high pass filter point, is that of a simple inverting amplifier:

$$A_{VINPUTSTAGE} = -\frac{R_F}{R_I}$$

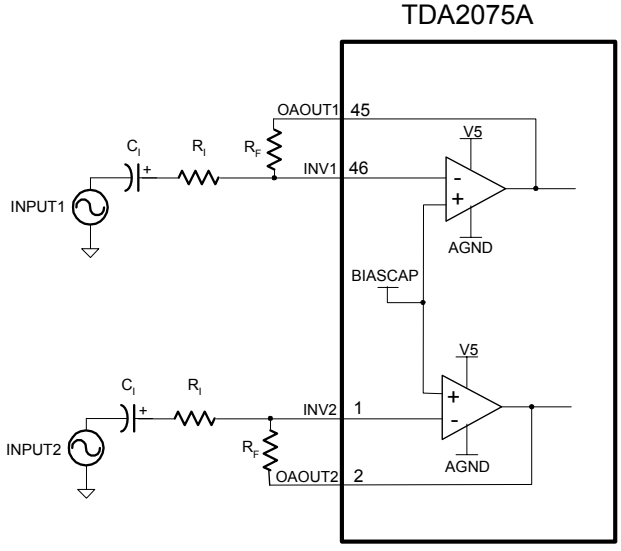


Figure 2: TDA2075A Input Stage

Input Capacitor Selection

C_I can be calculated once a value for R_I has been determined. C_I and R_I determine the input low-frequency pole. Typically this pole is set below 10Hz to minimize attenuation at 20Hz. C_{IN} is calculated according to:

$$C_I = 1 / (2\pi \times F_P \times R_I)$$

where: R_I = Input resistor value in ohms (typically 20kΩ)
F_P = Input low frequency pole (typically 3.6Hz)

Modulator Feedback Design

The modulator converts the signal from the input stage to the high-voltage output signal. The optimum gain of the modulator is determined from the maximum allowable feedback level for the modulator and maximum supply voltages for the power stage. Depending on the maximum supply voltage, the feedback ratio will need to be adjusted to maximize performance. The values of R_{FBA}, R_{FBB} and R_{FBC} (see explanation below) define the gain of the modulator. Once these values are chosen, based on the maximum supply voltage, the gain of the modulator will be fixed.

For the best signal-to-noise ratio and lowest distortion, the maximum modulator feedback voltage should be approximately 4Vpp. The modulator feedback resistor R_{FBC} should be adjusted so that the modulator feedback voltage is approximately 4Vpp. This will keep the gain of the modulator as low as possible and still allow headroom so that the feedback signal does not clip the modulator feedback stage. Increasing the value of R_{FBC} will increase the modulator gain. Sometimes increasing the value of R_{FBC} may be necessary to achieve full power for the amplifier since the input stage will clip at approximately 4Vpp. This will ensure that the input stage doesn't clip before the output stage.

Figure 3 shows how the feedback from the output of the amplifier is returned to the input of the modulator. The input to the modulator (FBKOUT1/FBKGND1 for channel 1) can be viewed as inputs to an inverting differential amplifier. R_{FBA} and R_{FBB} bias the feedback signal to approximately 2.5V and R_{FBC} scales the large OUT1/OUT2 signal to down to 4Vpp.

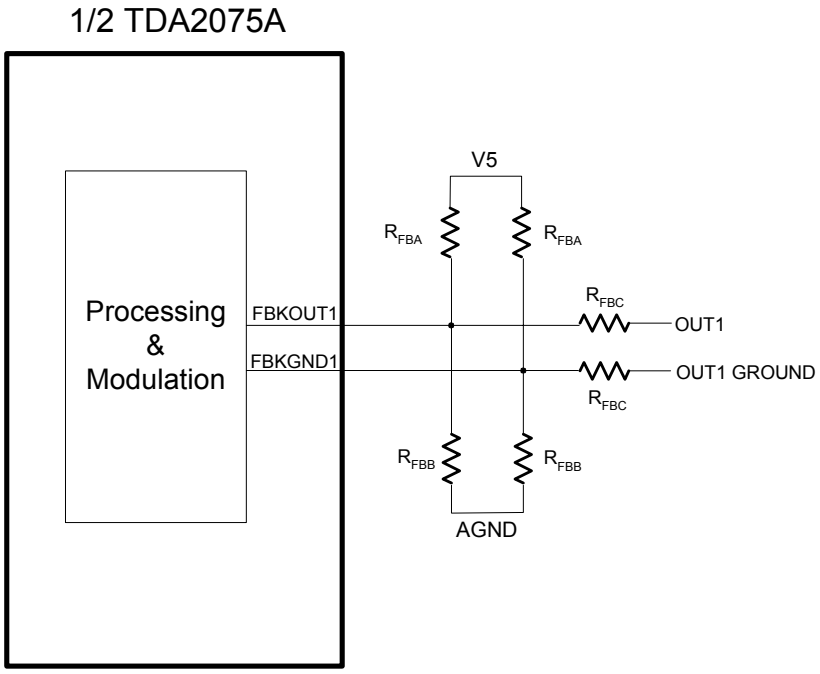


Figure 3: Modulator Feedback

For **SPLIT-SUPPLY** operation:

The modulator feedback resistors are:

$$R_{FBA} = \text{User specified, typically } 1K\Omega$$

$$R_{FBB} = \frac{R_{FBA} * VPP}{(VPP - 4)}$$

$$R_{FBC} = \frac{R_{FBA} * VPP}{4}$$

$$A_{V\text{ - MODULATOR}} \approx \frac{R_{FBC} * (R_{FBA} + R_{FBB})}{R_{FBA} * R_{FBB}} + 1$$

The above equations assume that VPP=|VNN|.

For example, in a system with a **SPLIT-SUPPLY** of VPP_{MAX}=40V and VNN_{MAX}=-40V,

R_{FBA} = 1kΩ, 1%
R_{FBB} = 1.111kΩ, use 1.1kΩ, 1%
R_{FBC} = 10.0kΩ, use 10.0kΩ, 1%

The resultant modulator gain is:

$$A_{V\text{ - MODULATOR}} \approx \frac{10.0k\,\Omega * (1.0k\,\Omega + 1.1k\,\Omega)}{1.0k\,\Omega * 1.1k\,\Omega} + 1 = 20.09V/V$$

For **SINGLE-SUPPLY** operation:

The modulator feedback resistors are:

$$R_{FBB} = \text{User specified, typically } 1K\Omega$$

$$R_{FBC} = 350 * VPP - 1000$$

$$R_{FBB} = \frac{2333.33 * R_{FBC}}{(1000 + R_{FBC})}$$

$$A_{V\text{ - MODULATOR}} \approx \frac{R_{FBC} * (R_{FBA} + R_{FBB})}{R_{FBA} * R_{FBB}} + 1$$

For example, in a system with a **SINGLE-SUPPLY** of VPP_{MAX} = 40V,

R_{FBA} = 2.17kΩ, use 2.15kΩ, 1%
R_{FBB} = 1kΩ, 1%
R_{FBC} = 13.0kΩ, use 13.0kΩ, 1%

The resultant modulator gain is:

$$A_{V\text{ - MODULATOR}} \approx \frac{13.0k\,\Omega * (1.0k\,\Omega + 2.15k\,\Omega)}{1.0k\,\Omega * 2.15k\,\Omega} + 1 = 20.05V/V$$

DC Offset

While the DC offset voltages that appear at the speaker terminals of a TDA2075A amplifier are typically small, Tripath recommends that all offsets be removed with the circuit shown in Figure 4. It should be noted that the DC voltage on the output of a muted TDA2075A with no load is approximately 2.5V. This offset does not need to be nulled. The output impedance of the amplifier in mute mode is approximately 10KΩ thus explaining why the DC voltage drops to essentially zero when a typical load is connected.

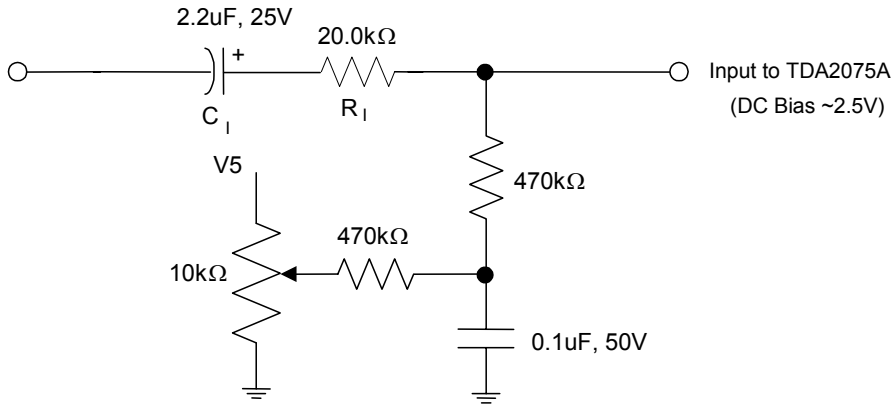


Figure 4: Offset Adjustment

Mute

When a logic high signal is supplied to MUTE, both amplifier channels are muted (complementary MOSFETs are turned off). When a logic level low is supplied to MUTE, both amplifiers are fully operational. There is a delay of approximately 240 milliseconds between the de-assertion of MUTE and the un-muting of the TDA2075A.

Turn-on & Turn-off Noise

If turn-on or turn-off noise is present in a TDA2075A amplifier, the cause is frequently due to other circuitry external to the TDA2075A. The TDA2075A has additional circuitry, as compared to previous Tripath amplifiers, which virtually eliminate any transients during power up and power down. While the TDA2075A has sophisticated circuitry to suppress turn-on and turn-off transients, the combination of the power supply and other audio circuitry with the TDA2075A in a particular application may exhibit audible transients. It is recommended that MUTE is active (pulled high) during power up and power down to minimize any audible transients caused by audio circuitry that precedes the TDA2075A.

Over-current Protection

The TDA2075A has over-current protection circuitry to protect itself and the output transistors from short-circuit conditions. The TDA2075A senses the voltage across resistor R_S to detect an over-current condition. Resistor R_S is in series with the load just after the low pass filter. The voltage is measured via OCSP1 and OCSN1 for channel 1 and OCSP2 and OCSN2 for channel 2. The OCS* pins must be Kelvin connected for proper operation. See “Circuit Board Layout” in Application Information for details.

When the voltage across R_S becomes greater than V_{TOC} (typically 0.5V), the TDA2075A will shut off the output stages of its amplifiers. The occurrence of an over-current condition also causes the TDA2075A Fault pin (pin 30) to go high. It is recommended that the Fault pin be connected externally to the mute pin to mute the processor during an over-current condition. The Fault circuitry is an open drain configuration and requires a pull-down resistor. The removal of the over-current condition returns the amplifier to normal operation.

Setting Over-current Threshold

R_S determines the value of the over-current threshold, I_{SC}:

$I_{SC} = V_{TOC}/R_S$ where R_S is in Ω's
V_{TOC} = Over-current sense threshold voltage (See Electrical Characteristics Table)
= 0.55V typically

For example, to set an I_{SC} of 11A, R_S will be 50mΩ.

Over- and Under-Voltage Protection

The TDA2075A senses the power rails through external resistor networks connected to VNNSENSE and VPPSENSE. The over- and under-voltage limits are determined by the values of the resistors in the networks, as described in the table "Test/Application Circuit Component Values". If the supply voltage falls outside the upper and lower limits determined by the resistor networks, the TDA2075A shuts off the output stages of the amplifiers. The removal of the over-voltage or under-voltage condition returns the TDA2075A to normal operation. Please note that trip points specified in the Electrical Characteristics table are at 25°C and may change over temperature.

The TDA2075A has built-in over and under voltage protection for both the VPP and VNN supply rails. The nominal operating voltage will typically be chosen as the supply "center point." This allows the supply voltage to fluctuate, both above and below, the nominal supply voltage.

VPPSENSE (pin 40) performs the over and undervoltage sensing for the positive supply, VPP. VNNSENSE (pin 38) performs the same function for the negative supply, VNN. When the current through VPPSENSE (or VNNSENSE) goes below or above the values shown in the Electrical Characteristics section (caused by changing the power supply voltage), the TDA2075A will be muted. VPPSENSE is internally biased at 2.5V and VNNSENSE is biased at 1.25V. In a single-supply application, VNNSENSE should be disabled by connecting a 16KΩ resistor for pin 38 to AGND.

Once the supply comes back into the supply voltage operating range (as defined by the supply sense resistors), the TDA2075A will automatically be un-muted and will begin to amplify. There is a hysteresis range on both the VPPSENSE and VNNSENSE pins. If the amplifier is powered up in the hysteresis band, the amplifier will be muted. Therefore, the usable supply range is the difference between the over-voltage turn-off and under-voltage turn-off for both the VPP and VNN supplies. It should be noted that the supply voltage must be outside of the user defined supply range for greater than 200mS for the TDA2075A to be muted.

Figure 5 shows the proper connection for the Over / Under voltage sense circuit for both the VPPSENSE and VNNSENSE pins.

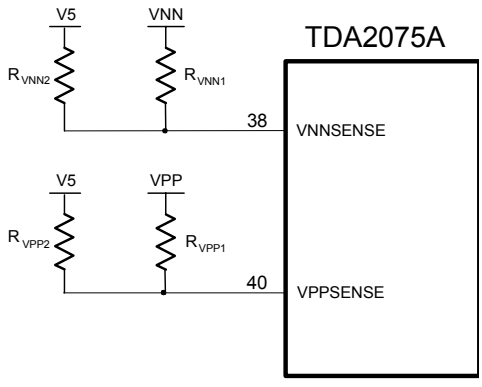


Figure 5: Over / Under voltage sense circuit

The equation for calculating R_{VPP1} is as follows:

$$R_{VPP1} = \frac{VPP}{I_{VPPSENSE}}$$

Set $R_{VPP2} = R_{VPP1}$.

The equation for calculating $R_{VNNSENSE}$ is as follows:

$$R_{VNN1} = \frac{VNN}{I_{VNNSENSE}}$$

Set $R_{VNN2} = 3 \times R_{VNN1}$.

$I_{VPPSENSE}$ or $I_{VNNSENSE}$ can be any of the currents shown in the Electrical Characteristics table for VPPSENSE and VNNSENSE, respectively.

The two resistors, R_{VPP2} and R_{VNN2} compensate for the internal bias points. Thus, R_{VPP1} and R_{VNN1} can be used for the direct calculation of the actual VPP and VNN trip voltages without considering the effect of R_{VPP2} and R_{VNN2}.

Using the resistor values from above, the actual minimum over voltage turn off points will be:

$$VPP_{MIN\_OV\_TUR\ N\_OFF} = R_{VPP1} \times I_{VPPSENSE\ (MIN\_OV\_TU\ RN\_OFF)}$$
$$VNN_{MIN\_OV\_TUR\ N\_OFF} = -(R_{VNN1} \times I_{VNNSENSE\ (MIN\_OV\_TU\ RN\_OFF)})$$

The other three trip points can be calculated using the same formula but inserting the appropriate $I_{VPPSENSE}$ (or $I_{VNNSENSE}$) current value. As stated earlier, the usable supply range is the difference between the minimum overvoltage turn off and maximum under voltage turn-off for both the VPP and VNN supplies.

$$VPP_{RANGE} = VPP_{MIN\_OV\_TUR\ N\_OFF} - VPP_{MAX\_UV\_TUR\ N\_OFF}$$
$$VNN_{RANGE} = VNN_{MIN\_OV\_TUR\ N\_OFF} - VNN_{MAX\_UV\_TUR\ N\_OFF}$$

Output Transistor Selection

The key parameters to consider when selecting what n-channel and p-channel MOSFETs to use with the TDA2075A are drain-source breakdown voltage (BVdss), gate charge (Qg), and on-resistance ($R_{DS(ON)}$).

The BVdss rating of the MOSFET needs to be selected to accommodate the voltage swing between V_{SPOS} and V_{SNEG} as well as any voltage peaks caused by voltage ringing due to switching transients. With a 'good' circuit board layout, a BVdss that is 50% higher than the VPP to VNN voltage swing is a reasonable starting point. The BVdss rating should be verified by measuring the actual voltages experienced by the MOSFET in the final circuit.

Ideally a low Qg (total gate charge) and low $R_{DS(ON)}$ are desired for the best amplifier performance. Unfortunately, these are conflicting requirements since $R_{DS(ON)}$ is inversely proportional to Qg for a typical MOSFET. The design trade-off is one of cost versus performance. A lower $R_{DS(ON)}$ means lower $I^2R_{DS(ON)}$ losses but the associated higher Qg translates into higher switching losses (losses = Qg x 10 x 1.2MHz). A lower $R_{DS(ON)}$ also means a larger silicon die and higher cost. A higher $R_{DS(ON)}$ means lower cost and lower switching losses but higher I^2R_{DSON} losses.

Gate Resistor Selection

The gate resistors, R_G, are used to control MOSFET switching rise/fall times and thereby minimize voltage overshoots. They also dissipate a portion of the power resulting from moving the gate charge

each time the MOSFET is switched. If R_G is too small, excessive heat can be generated in the driver. Large gate resistors lead to slower MOSFET switching edges which require a larger break-before-make (BBM) delay.

Break-Before-Make (BBM) Timing Control

The complementary half-bridge power MOSFETs require a deadtime between when one transistor is turned off and the other is turned on (break-before-make) in order to minimize shoot through currents. The TDA2075A has an analog input pin that controls the break-before-make timing of the output transistors. Connecting R_{BBM} from the BBMSET pin (pin 7) to analog ground creates a current that defines the BBM setting by the following equation.

BBM (nsec) = 2 X R_{BBM} + 7 where R_{BBM} is in kΩ's and 5kΩ < R_{BBM}* < 100kΩ

* An R_{BBM} of 0Ω will yield a BBM setting of 0nsec.

There is tradeoff involved in making this setting. As the delay is reduced, distortion levels improve but shoot-through and power dissipation increase. All typical curves and performance information were done with using a R_{BBM}. The actual amount of BBM required is dependent upon other component values and circuit board layout, the value selected should be verified in the actual application circuit/board. It should also be verified under maximum temperature and power conditions since shoot-through in the output MOSFETs can increase under these conditions, possibly requiring a higher BBM setting than at room temperature.

Recommended MOSFETs

The following devices are capable of achieving full performance, both in terms of distortion and efficiency, for the specified load impedance and voltage range. Additional devices will be added as subsequent characterization is completed.

Device Information – Recommended MOSFETs

Part Number	Manufacturer	BV_{DSS} (V)	I_D (A)	Q_g (nC)	$R_{DS(on)}$ (Ω)	Package
FQP13N10	Fairchild Semiconductor	100	12.8	12	0.142	TO220
FQP12P10	Fairchild Semiconductor	-100	-11.5	21	0.240	TO220

Output Filter Design

One advantage of Tripath amplifiers over PWM solutions is the ability to use higher-cutoff-frequency filters. This means load-dependent peaking/droop in the 20kHz audio band potentially caused by the filter can be made negligible. This is especially important for applications where the user may select a 6-Ohm or 8-Ohm speaker. Furthermore, speakers are not purely resistive loads and the impedance they present changes over frequency and from speaker model to speaker model.

Tripath recommends designing the filter as a 2nd order LC filter. Tripath has obtained good results with L_F = 11uH and C_F = 0.22uF.

The core material of the output filter inductor has an effect on the distortion levels produced by a TDA2075A amplifier. Tripath recommends low-mu type-2 iron powder cores because of their low loss and high linearity (available from Micrometals, www.micrometals.com). Please refer to the RB-TDA2075A for the specific core used.

Tripath also recommends that an RC damper be used after the LC low-pass filter. No-load operation of a TDA2075A amplifier can create significant peaking in the LC filter, which produces strong resonant currents that can overheat the output MOSFETs and/or other components. The RC dampens the peaking and prevents problems. Tripath has obtained good results with R_Z = 20Ω and C_Z = 0.22uF.

Low-frequency Power Supply Pumping

A potentially troublesome phenomenon in single-ended switching amplifiers is power supply pumping. This phenomenon is caused by current from the output filter inductor flowing into the power supply output filter capacitors in the opposite direction as a DC load would drain current from them. Under certain conditions (usually low-frequency input signals), this current can cause the supply voltage to "pump" (increase in magnitude) and eventually cause over-voltage/under-voltage shut down. Moreover, since over/under-voltage are not "latched" shutdowns, the effect would be an amplifier that oscillates between on and off states. If a DC offset on the order of 0.3V is allowed to develop on the output of the amplifier (see "DC Offset Adjust"), the supplies can be boosted to the point where the amplifier's over-voltage protection triggers.

One solution to the pumping issue is to use large power supply capacitors to absorb the pumped supply current without significant voltage boost. The low-frequency pole used at the input to the amplifier determines the value of the capacitor required. This works for AC signals only.

A no-cost solution to the pumping problem uses the fact that music has low frequency information that is correlated in both channels (it is in phase). This information can be used to eliminate boost by putting the two channels of a TDA2075A amplifier out of phase with each other. This works because each channel is pumping out of phase with the other, and the net effect is a cancellation of pumping currents in the power supply. The phase of the audio signals needs to be corrected by connecting one of the speakers in the opposite polarity as the other channel.

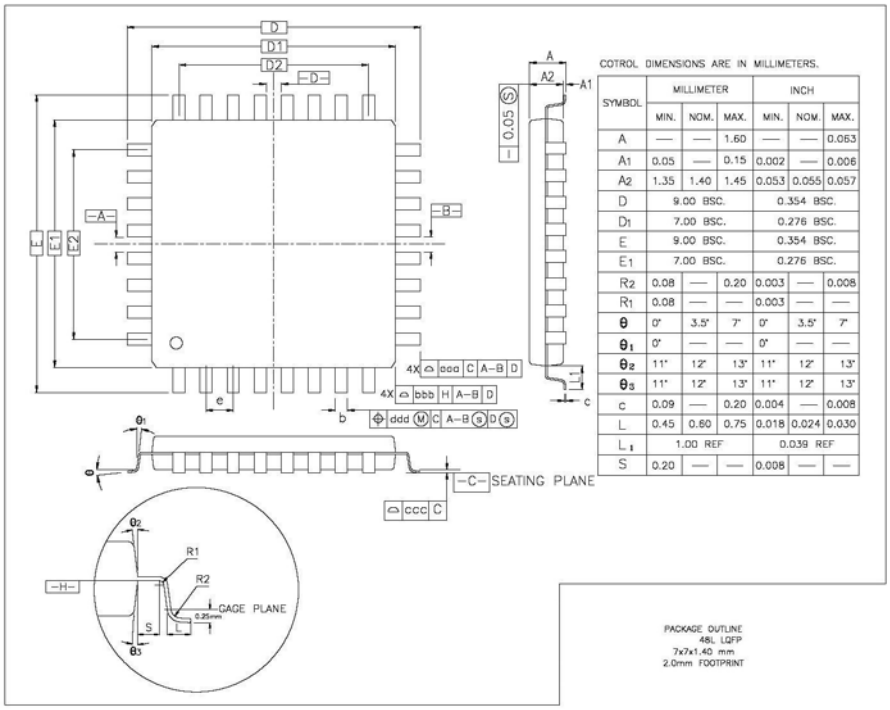
Performance Measurements of a TDA2075A Amplifier

Tripath amplifiers operate by modulating the input signal with a high-frequency switching pattern. This signal is sent through a low-pass filter (external to the TDA2075A) that demodulates it to recover an amplified version of the audio input. The frequency of the switching pattern is spread spectrum and typically varies between 200kHz and 1.5MHz, which is well above the 20Hz – 22kHz audio band. The pattern itself does not alter or distort the audio input signal but it does introduce some inaudible noise components.

The measurements of certain performance parameters, particularly those that have anything to do with noise, like THD+N, are significantly affected by the design of the low-pass filter used on the output of the TDA2075A and also the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just past the audio band or the bandwidth of the measurement instrument ends there, some of the inaudible noise components introduced by the Tripath amplifier switching pattern will get integrated into the measurement, degrading it.

Tripath amplifiers do not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters can increase distortion due to inductor non-linearity. Multi-pole filters require relatively large inductors, and inductor non-linearity increases with inductor value.

Package Information



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

PACKAGE OUTLINE
48L LQFP
7x7x1.40 mm
2.0mm FOOTPRINT

SYMBOL	32L						44L						48L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018	0.17	0.20	0.27	0.007	0.008	0.011	0.17	0.20	0.27	0.007	0.008	0.011
e	0.80 BSC.			0.031 BSC.			0.50 BSC.			0.020 BSC.			0.50 BSC.			0.020 BSC.		
D2	5.60			0.220			5.00			0.197			5.50			0.217		
E2	5.60			0.220			5.00			0.197			5.50			0.217		
TOLERANCES OF FORM AND POSITION																		
aaa	0.20			0.008			0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.10			0.003			0.08			0.003			0.08			0.003		
ddd	0.20			0.008			0.08			0.003			0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 44L WERE BASE ON THOSE OF 48L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

PACKAGE OUTLINE
32/44/48L LQFP
7x7x1.40 mm
2.0mm FOOTPRINT

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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