

DATA SHEET

TDA8586

**Power amplifier with load detection
and auto BTL/SE selection**

Preliminary specification
Supersedes data of 1998 May 25
File under Integrated Circuits, IC01

1999 Apr 08

Power amplifier with load detection and auto BTL/SE selection

TDA8586

FEATURES

General

- Operating voltage from 8 to 18 V
- Low distortion
- Few external components, fixed gain
- Automatic mode selection (SE or BTL) depending on connected 'rear' loads
- Can be used as a stereo amplifier in Bridge-Tied Load (BTL) or quad Single-Ended (SE) amplifiers
- Single-ended mode without loudspeaker capacitor
- Soft clipping, to guarantee good clip behaviour with inductive loads
- Mute and standby mode with one-pin operation
- Diagnostic information for Dynamic Distortion Detector (DDD), high temperature (140 °C) mode of operation and short-circuit
- No switch-on/off pops when switching between standby and mute and from mute to on
- Load detection on 'rear' channels when switching from standby to mute
- Fast mute on supply voltage drops (low V_P mute).

Protection

- Short-circuit proof to ground, positive supply voltage on all pins and across load
- ESD protected on all pins
- Thermal protection against temperatures exceeding 150 °C
- Load dump protection
- Overvoltage protection.

GENERAL DESCRIPTION

The IC incorporates the following functions:

1. 4×6 W SE amplifies without SE capacitor, because of the availability of 2 half supply voltage power buffers
2. 2×20 W BTL amplifiers
3. Automatic switching between 2 and 4 speaker operation. The mode of operation is determined during start-up.

This amplifier is protected for all general short-circuit conditions to battery or ground, overvoltage, 45 V load dump and short-circuits on the speaker outputs.

The IC is contained in a 20-pin power HSOP package, but is also available in a 17-pin SIL power package. When packaged in the 20-pin HSOP package additional functions are available:

1. DDD level selection between 2 and 10%
2. Overrule pin for changing mode of operation (from SE to BTL or from BTL to SE).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8586Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1
TDA8586TH	HSOP20	heatsink small outline package; 20 leads; low stand-off	SOT418-2

Power amplifier with load detection and auto BTL/SE selection

TDA8586

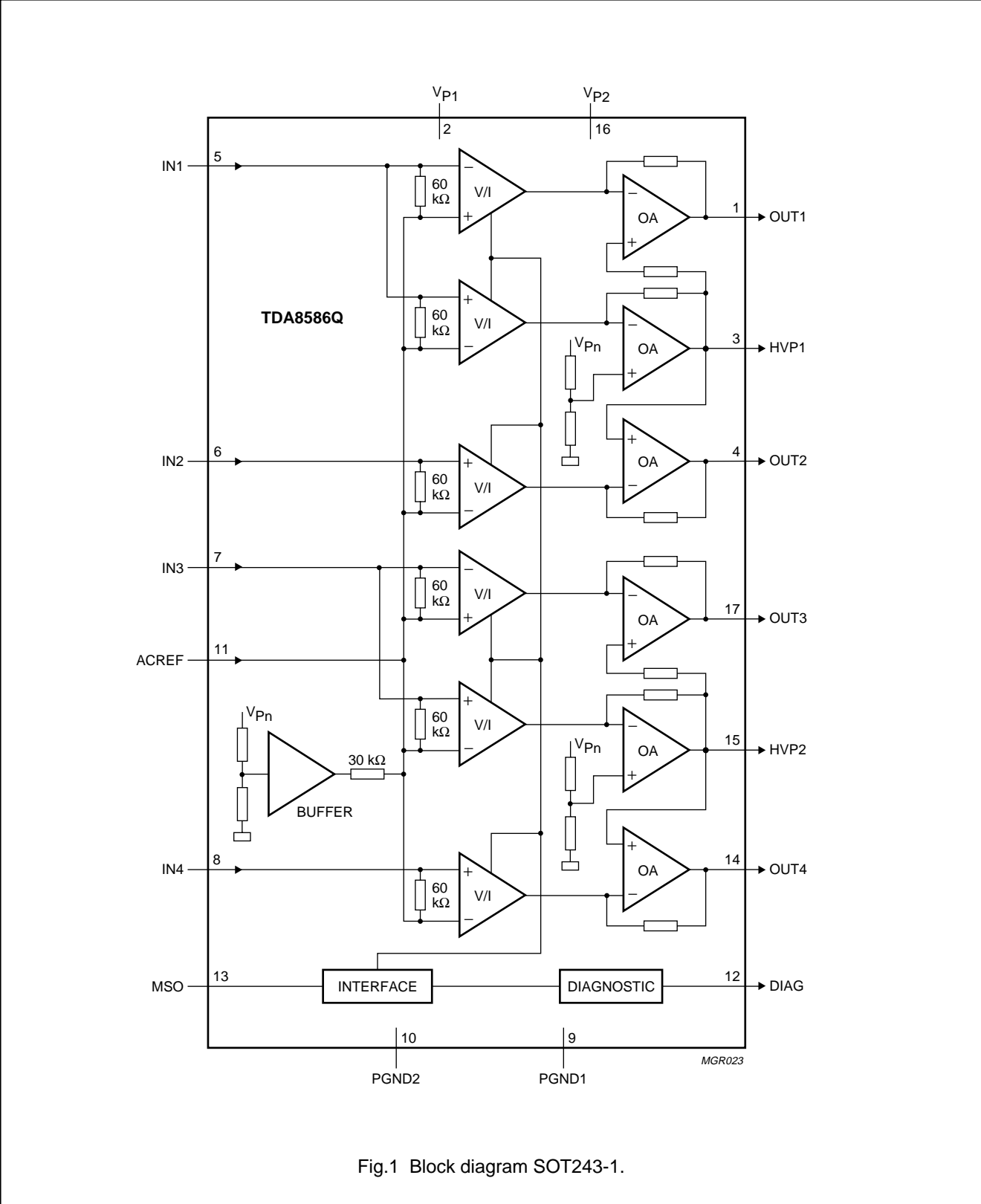
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _P	operating supply voltage		8.0	–	18	V
I _{q(tot)}	total quiescent current	V _P = 14.4 V, SE mode	–	140	170	mA
I _{stb}	standby supply current	V _P = 14.4 V	–	1	100	μA
G _V	voltage gain	SE mode	25	26	27	dB
		BTL mode	31	32	33	dB
Bridge-tied load application						
P _O	output power	V _P = 14.4 V; R _L = 4 Ω				
		THD = 0.5%	14	15	–	W
		THD = 10%	17	21	–	W
THD	total harmonic distortion	f _i = 1 kHz; P _O = 1 W; V _P = 14.4 V; R _L = 4 Ω	–	0.05	0.15	%
V _{OO}	DC output offset voltage	V _P = 14.4 V; R _L = 4 Ω; mute condition	–	10	20	mV
		V _P = 14.4 V; on condition	–	0	100	mV
V _{n(o)}	noise output voltage	R _S = 1 kΩ; V _P = 14.4 V	–	100	200	μV
Single-ended application						
P _O	output power	V _P = 14.4 V; R _L = 4 Ω				
		THD = 0.5%	4	4.5	–	W
		THD = 10%	5	6	–	W
THD	total harmonic distortion	f _i = 1 kHz; P _O = 1 W; V _P = 14.4 V; R _L = 4 Ω	–	0.08	0.15	%
V _{OO}	DC output offset voltage	V _P = 14.4 V; R _L = 4 Ω; mute condition	–	10	20	mV
		V _P = 14.4 V; on condition	–	0	100	mV
V _{n(o)}	noise output voltage	R _S = 1 kΩ; V _P = 14.4 V	–	80	150	μV

Power amplifier with load detection and
auto BTL/SE selection

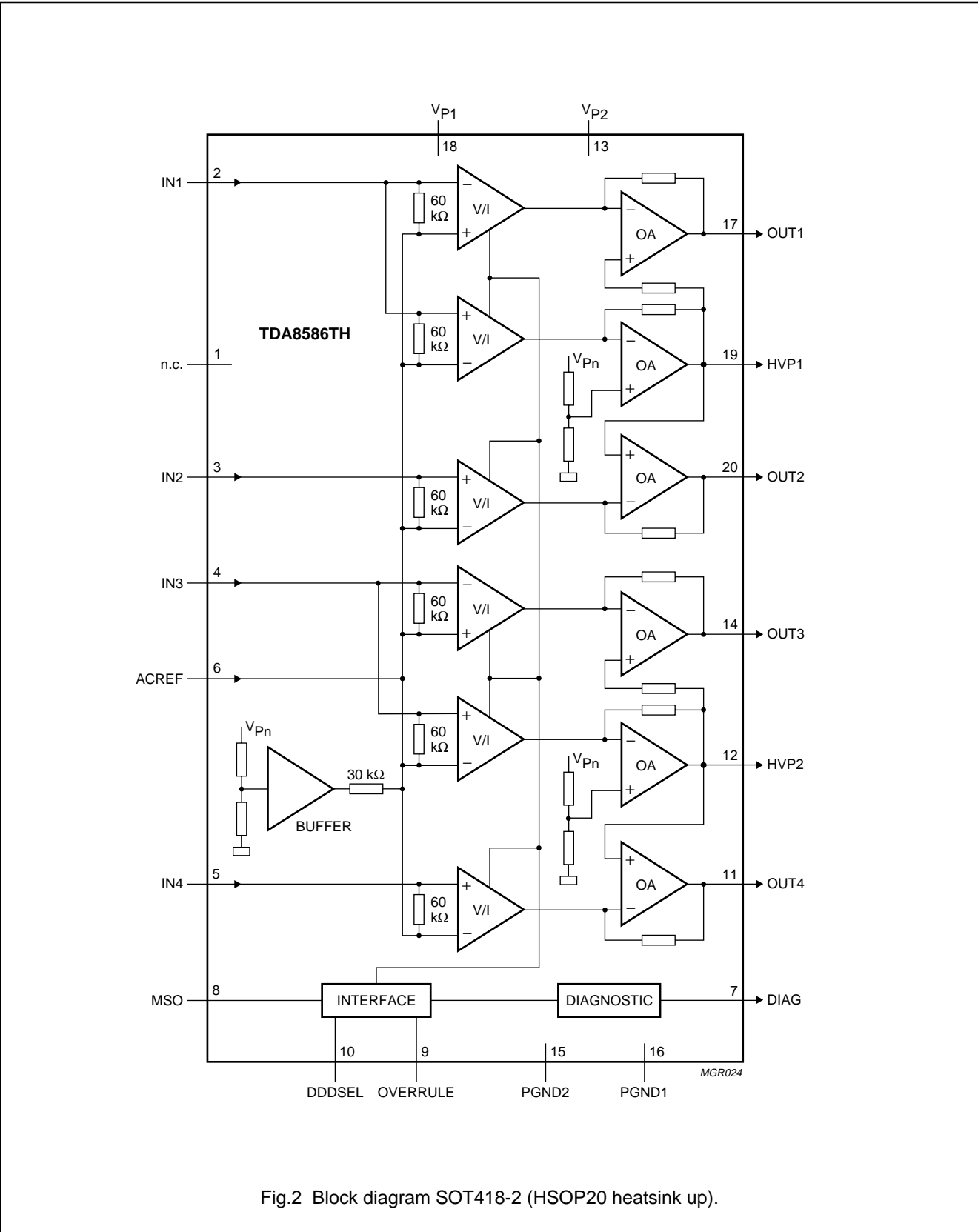
TDA8586

BLOCK DIAGRAM



Power amplifier with load detection and
auto BTL/SE selection

TDA8586



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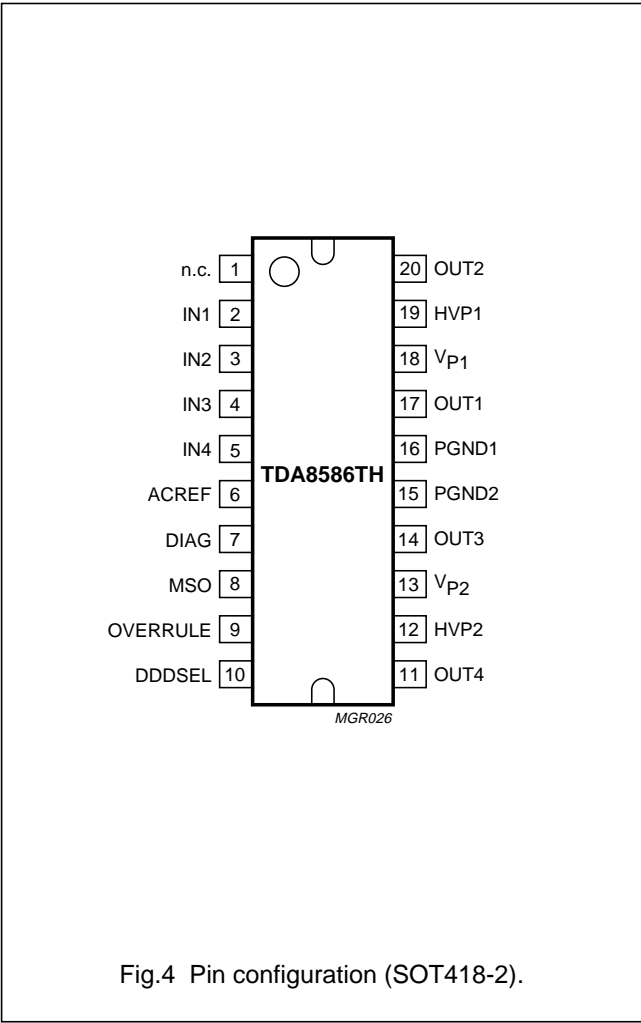
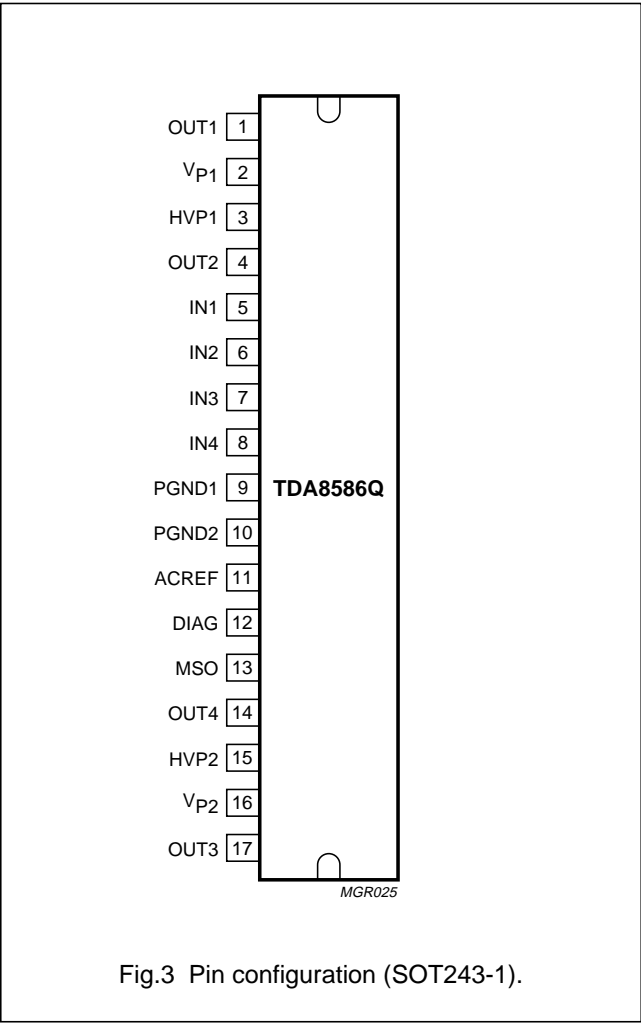
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PINNING

SYMBOL	PIN SOT243	PIN SOT418	DESCRIPTION
n.c.	–	1	not connected
IN1	5	2	non-inverting input 1
IN2	6	3	inverting input 2
IN3	7	4	non inverting input 3
IN4	8	5	inverting input 4
ACREF	11	6	common signal input
DIAG	12	7	diagnostic output/mode fix
MSO	13	8	mode select mute, standby or on
OVERRULE	–	9	mode selection overrule
DDDSEL	–	10	2 or 10% dynamic distortion detection
OUT4	14	11	SE output 4 (negative)
HVP2	15	12	buffer output/BTL output 2 (negative)
V _{P2}	16	13	supply voltage 2
OUT3	17	14	SE output 3/BTL output 2 (positive)
PGND2	10	15	power ground 2
PGND1	9	16	power ground 1
OUT1	1	17	SE output 1/BTL output 1 (positive)
V _{P1}	2	18	supply voltage 1
HVP1	3	19	buffer output/BTL output 1 (negative)
OUT2	4	20	SE output 2 (negative)

Power amplifier with load detection and
auto BTL/SE selection

TDA8586



Power amplifier with load detection and auto BTL/SE selection

TDA8586

FUNCTIONAL DESCRIPTION

The TDA8586 is a multi-purpose power amplifier with four amplifiers and 2 buffer stages, which can be connected in the following configurations with high output power and low distortion:

- Dual Bridge-Tied Load (BTL) amplifiers
- Quad Single-Ended (SE) amplifiers.

In the BTL mode of operation, the 2 buffer amplifiers act as inverting amplifiers to complete the bridge across the 'front' amplifiers (OUT1 and OUT3) and the 'rear' outputs (OUT2 and OUT4) enter a high-impedance state.

In the SE mode of operation, the buffers act as an AC ground path thereby eliminating the need for series capacitors on the speaker outputs.

Diagnostics:

- While the IC is in the mute mode, the diagnostic output will signal the mode of operation when the IC is not overruled
- In the on mode the diagnostic output will signal any fault in the IC or if the output of any amplifier is clipping with a distortion of 10% (or 2% depending on selected clip-mode).

Special attention is given to the dynamic behaviour as follows:

- Noise suppression during engine start
- No plops when switching from standby to on
- Slow offset change between mute and on (controlled by MSO pin)
- Low noise levels, which are independent of the supply voltage.

Protections are included to avoid the IC being damaged at:

- Over temperature: $T_j > 150\text{ }^{\circ}\text{C}$
- Short-circuit of the output pin(s) to ground or supply rail. When short-circuited, the power dissipation is limited
- ESD protection (Human Body Model 3000 V and Machine Model 300 V).

The presence of the load is measured after the transition between standby and mute. The IC will determine if there is an acceptable load on both outputs (OUT2 and OUT4). If both outputs are unloaded, the IC will switch to a 2 speaker mode of operation (BTL mode), unless it is overruled.

There are two options to overrule:

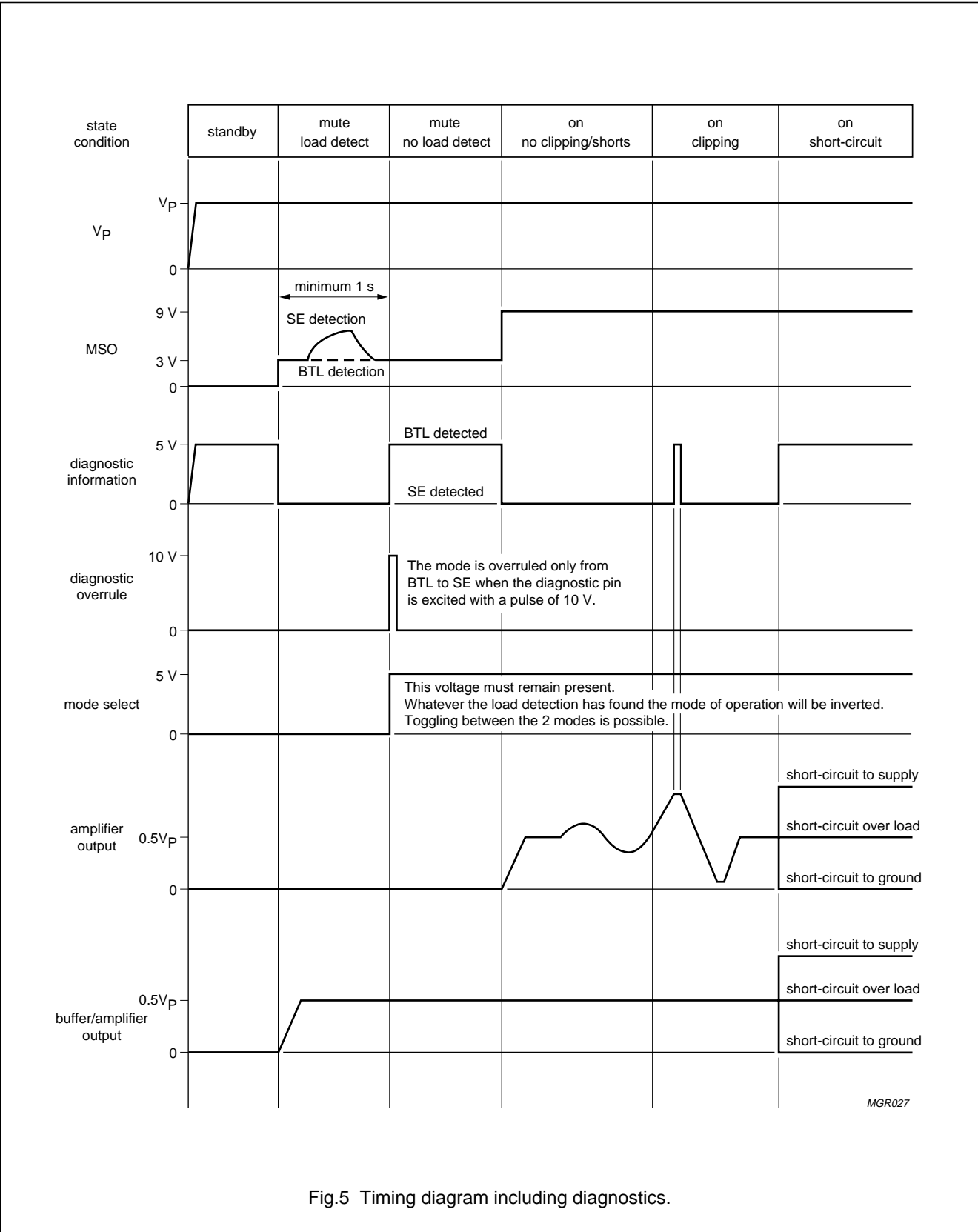
1. Before transition from mute to on, after a load detection, pulling the diagnostic output above 9.5 V will force the IC into 4 speaker mode
2. TDA8586TH: pulling the OVERRULE pin according pinning table.

Care should be taken with the OVERRULE function as it works during the on mode. If there is a 2 or 4 speaker mode change during the on mode a large 'plop' can be heard on the speakers.

The ACREF input (common signal input) acts with the four signal inputs (IN1 to IN4) to provide quasi differential inputs. A capacitor must be connected to this pin of which the ground pin should be connected to the ground at the signal source (usually the ground at the audio signal processor). This capacitor has a dual function. During the speaker detection, the signal ground capacitor is used to set the time constant of the measurement (and thus determines the minimum required switch-on time). The capacitor on the MSO pin allows the integrate function to provide immunity to outside noises during load detection.

Power amplifier with load detection and auto BTL/SE selection

TDA8586



Power amplifier with load detection and auto BTL/SE selection

TDA8586

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	8	18	V
		load dump protected; see Fig.6	–	45	V
V_{DIAG}	voltage on diagnostic pin		–	18	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
V_{rp}	reverse polarity voltage	note 1	–	6	V
V_{sc}	AC and DC short-circuit voltage of output pins across loads and to ground or supply pins		–	18	V
P_{tot}	total power dissipation		–	75	W
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+150	°C

Note

1. A large reverse current will flow, therefore external protection is needed (fuse and reverse diode).

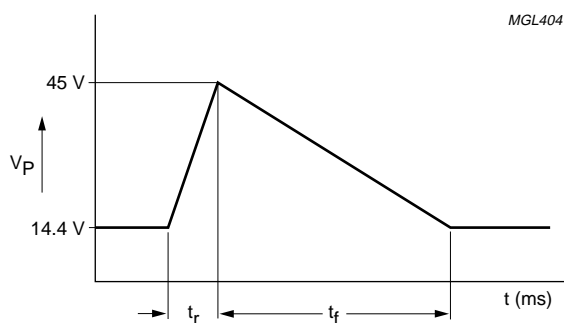


Fig.6 Load dump voltage waveform.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		2	K/W

Power amplifier with load detection and auto BTL/SE selection

TDA8586

CHARACTERISTICS

$V_P = 14.4\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; $f_i = 1\text{ kHz}$; $R_L = \infty$; measured in test circuit of Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	operating supply voltage		8.0	14.4	18	V
$I_{q(\text{tot})}$	total quiescent current	SE mode	–	140	170	mA
I_{stb}	standby current		–	1	100	μA
V_O	DC output voltage	$V_P = 14.4\text{ V}$	–	7.0	–	V
$V_{P(\text{mute})}$	low supply voltage mute		6.0	7.0	8.0	V
V_o	single-ended and bridge-tied load output voltage	$V_P = 14.4\text{ V}$; $R_L = 4\text{ }\Omega$ mute condition on condition	– –	– –	20 100	mV mV
V_I	DC input voltage	$V_P = 14.4\text{ V}$	–	4.0	–	V
PIN MSO						
V_{MSO}	voltage at pin MSO	standby condition	0	–	0.8	V
		mute condition; note 1	2.0	3.0	4	V
		on condition	8.0	–	10.5	V
I_{MSO}	input current	mute pin at standby condition; $V_{\text{MSO}} < 0.8\text{ V}$	–	5	40	μA
Diagnostic; output buffer (open-collector); see Figs 7 to 8						
$V_{\text{DIAG(L)}}$	diagnostic output voltage LOW	$I_{\text{sink}} = 1\text{ mA}$	–	0.3	0.8	V
I_{LI}	leakage current	$V_{\text{DIAG}} = 14.4\text{ V}$	–	–	1	μA
$V_{\text{DIAG(or)}}$	diagnostic override voltage	in mute mode after load detection	10.5	–	18	V
$V_{\text{DIAG(4ch)}}$	diagnostic 4 channel indication voltage	mute, after load detection with 4 speakers connected	–	0.3	0.8	V
CD2	clip detector LOW	THD mode; $V_{\text{DIAG}} > 3\text{ V}$; $R = 10\text{ k}\Omega$	0.5	2	3.5	%
CD10	clip detector HIGH	THD mode (default); $V_{\text{DIAG}} > 3\text{ V}$; $R = 10\text{ k}\Omega$	7	10	13	%
CLIP DETECT CONTROL PIN						
V_{DDSEL}	voltage at DDD select pin to obtain:	10% DDD	0	–	1	V
		2% DDD	3	–	6	V
I_{DDSEL}	Input current DDD select pin	$V_{\text{DDSEL}} = 5\text{ V}$	15	–	140	μA

Power amplifier with load detection and auto BTL/SE selection

TDA8586

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (see Fig.7)						
THD	total harmonic distortion	$f_i = 1 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega$	–	0.05	0.15	%
		$45 \text{ Hz} < f_i < 10 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega; \text{filter: } f < 30 \text{ kHz}$	–	0.3	–	%
P_o	output power	$V_P = 14.4 \text{ V}; R_L = 4 \Omega; \text{note 2}$				
		THD = 0.5%	14	15	–	W
		THD = 10%	17	21	–	W
G_v	voltage gain	$V_{i(\text{rms})} = 15 \text{ mV}$	31	32	33	dB
ΔG_v	channel unbalance	$V_{i(\text{rms})} = 15 \text{ mV}$	–0.7	0	+0.7	dB
α_{cs}	channel separation	$P_o = 2 \text{ W}; f_i = 1 \text{ kHz}; R_L = 4 \Omega$	45	55	–	dB
V_{OO}	DC output offset voltage	$V_P = 14.4 \text{ V}; \text{on condition}$	–	0	100	mV
		$V_P = 14.4 \text{ V}; R_L = 4 \Omega; \text{mute condition}$	–	10	20	mV
$V_{n(o)}$	noise output voltage on	$R_s = 1 \text{ k}\Omega; V_P = 14.4 \text{ V}; \text{note 3}$	–	100	150	μV
$V_{n(o)(\text{mute})}$	noise output voltage mute	note 3	–	0	20	μV
$V_{o(\text{mute})}$	output voltage mute	$V_{i(\text{rms})} = 1 \text{ V}$	–	3	500	μV
SVRR	supply voltage ripple rejection:	$R_s = 0 \Omega; f_i = 1 \text{ kHz}; V_{\text{ripple}} = 2 \text{ V (p-p)}$				
		on condition	45	55	–	dB
		mute condition	55	70	–	dB
Z_i	input impedance	input referenced to ground	40	60	90	$\text{k}\Omega$

Power amplifier with load detection and auto BTL/SE selection

TDA8586

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quad SE application (see Fig.8)						
THD	total harmonic distortion	$f_i = 1 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega$	–	0.05	0.15	%
		$45 \text{ Hz} < f_i < 10 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega; \text{filter: } f < 30 \text{ kHz}$	–	0.5	–	%
P_o	output power	$V_P = 14.4 \text{ V}; R_L = 4 \Omega; \text{note 2}$				
		THD = 0.5%	4	4.5	–	W
		THD = 10%	5	6	–	W
G_v	voltage gain	$V_{i(\text{rms})} = 15 \text{ mV}$	25	26	27	dB
ΔG_v	channel unbalance	$V_{i(\text{rms})} = 15 \text{ mV}$	–0.7	0	+0.7	dB
α_{CS}	channel separation	$P_o = 2 \text{ W}; f_i = 1 \text{ kHz}; R_L = 4 \Omega$	40	50	–	dB
V_{OO}	DC output offset voltage	$V_P = 14.4 \text{ V}; \text{on condition}$	–	0	100	mV
		$V_P = 14.4 \text{ V}; R_L = 4 \Omega; \text{mute condition}$	–	10	20	mV
$V_{n(o)}$	noise output voltage on	$R_s = 1 \text{ k}\Omega; V_P = 14.4 \text{ V}; \text{note 3}$	–	80	150	μV
$V_{n(o)(\text{mute})}$	noise output voltage mute	note 3	–	0	20	μV
$V_{o(\text{mute})}$	output voltage mute	$V_{i(\text{rms})} = 1 \text{ V}$	–	3	500	μV
SVRR	supply voltage ripple rejection	$R_s = 0 \Omega; f_i = 1 \text{ kHz}; V_{\text{ripple}} = 2 \text{ V (p-p)}$				
		on condition	43	47	–	dB
		mute condition	55	70	–	dB

Notes

1. Tolerances on the mute level is tight because of the usage of this pin for integration during load detection.
2. The output power is measured directly on the pins of the IC.
3. The noise output is measured in a bandwidth of 20 Hz to 20 kHz.

Power amplifier with load detection and auto BTL/SE selection

TDA8586

APPLICATION INFORMATION

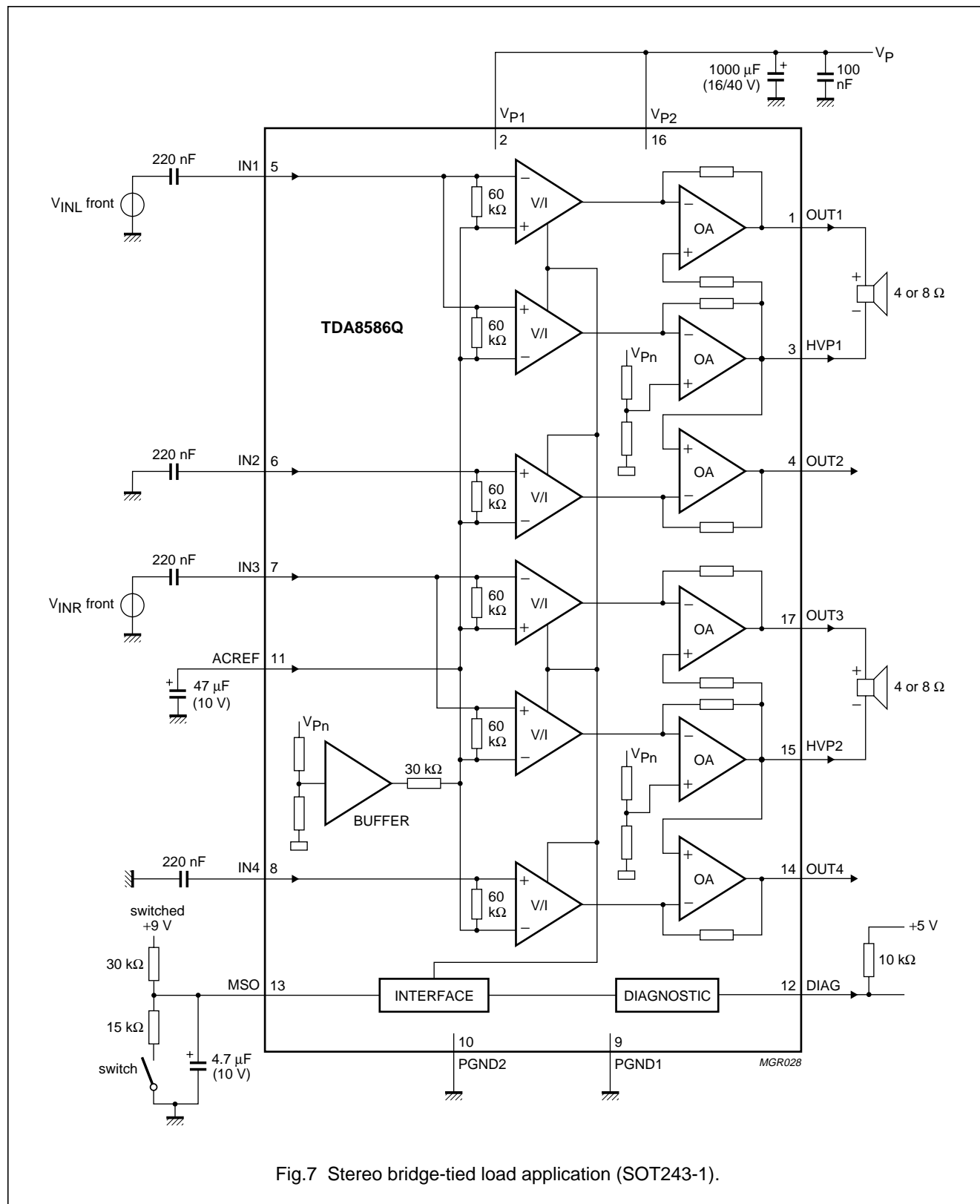


Fig.7 Stereo bridge-tied load application (SOT243-1).

Power amplifier with load detection and
auto BTL/SE selection

TDA8586

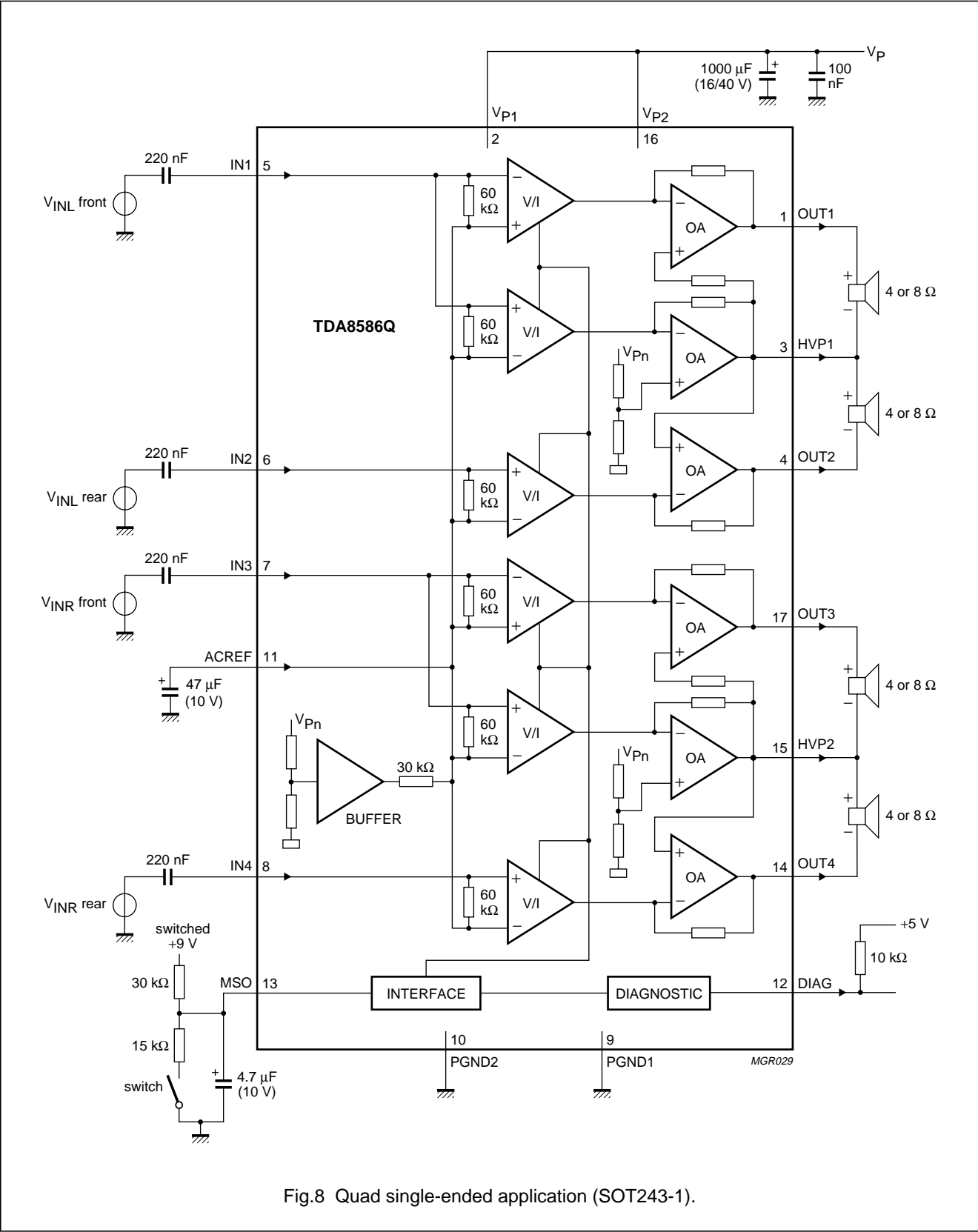


Fig.8 Quad single-ended application (SOT243-1).

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TDA8586

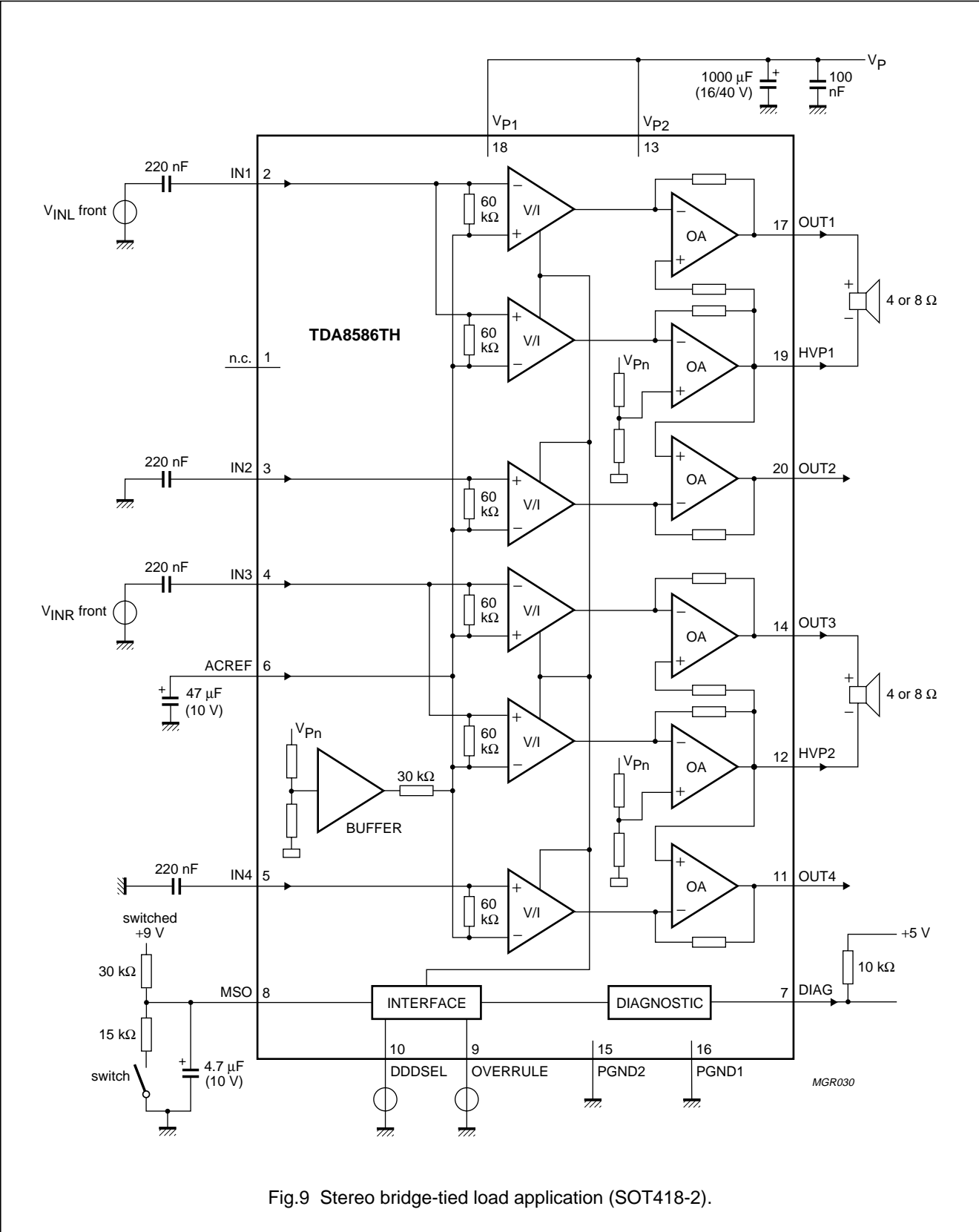


Fig.9 Stereo bridge-tied load application (SOT418-2).

Power amplifier with load detection and auto BTL/SE selection

TDA8586

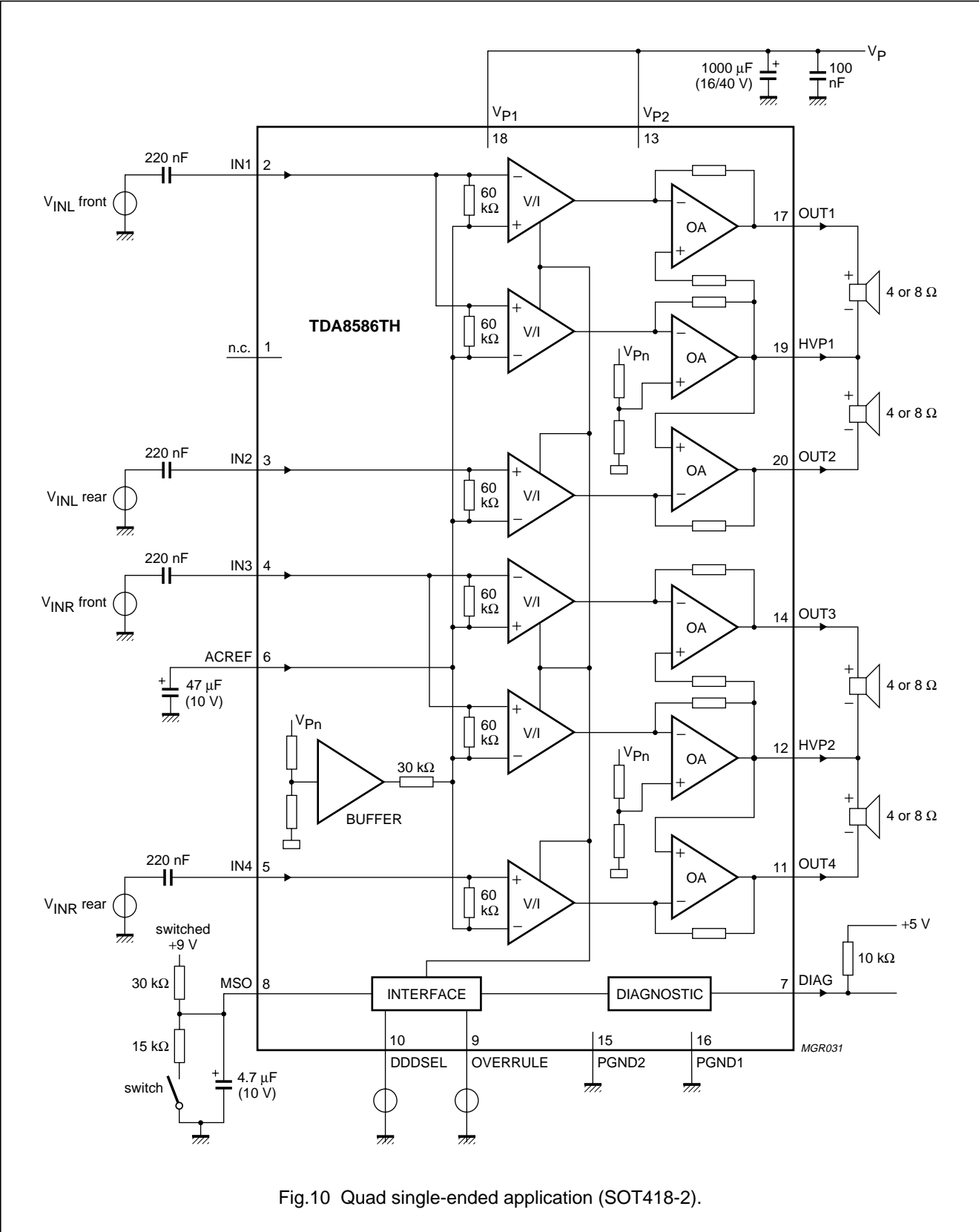
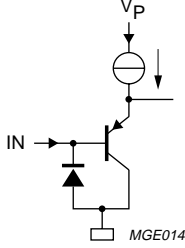
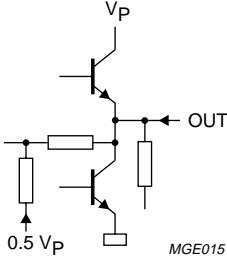
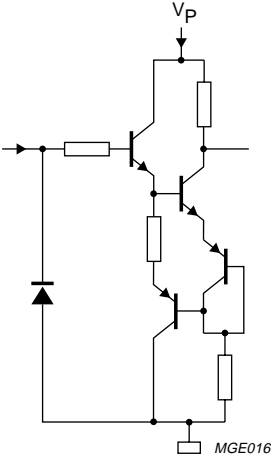


Fig.10 Quad single-ended application (SOT418-2).

Power amplifier with load detection and auto BTL/SE selection

TDA8586

INTERNAL PIN CONFIGURATION

PIN TDA8586TH	NAME	EQUIVALENT CIRCUIT
2, 3, 4, 5 and 6	inputs	
11, 12, 14, 17, 19 and 20	outputs	
8	mode select	

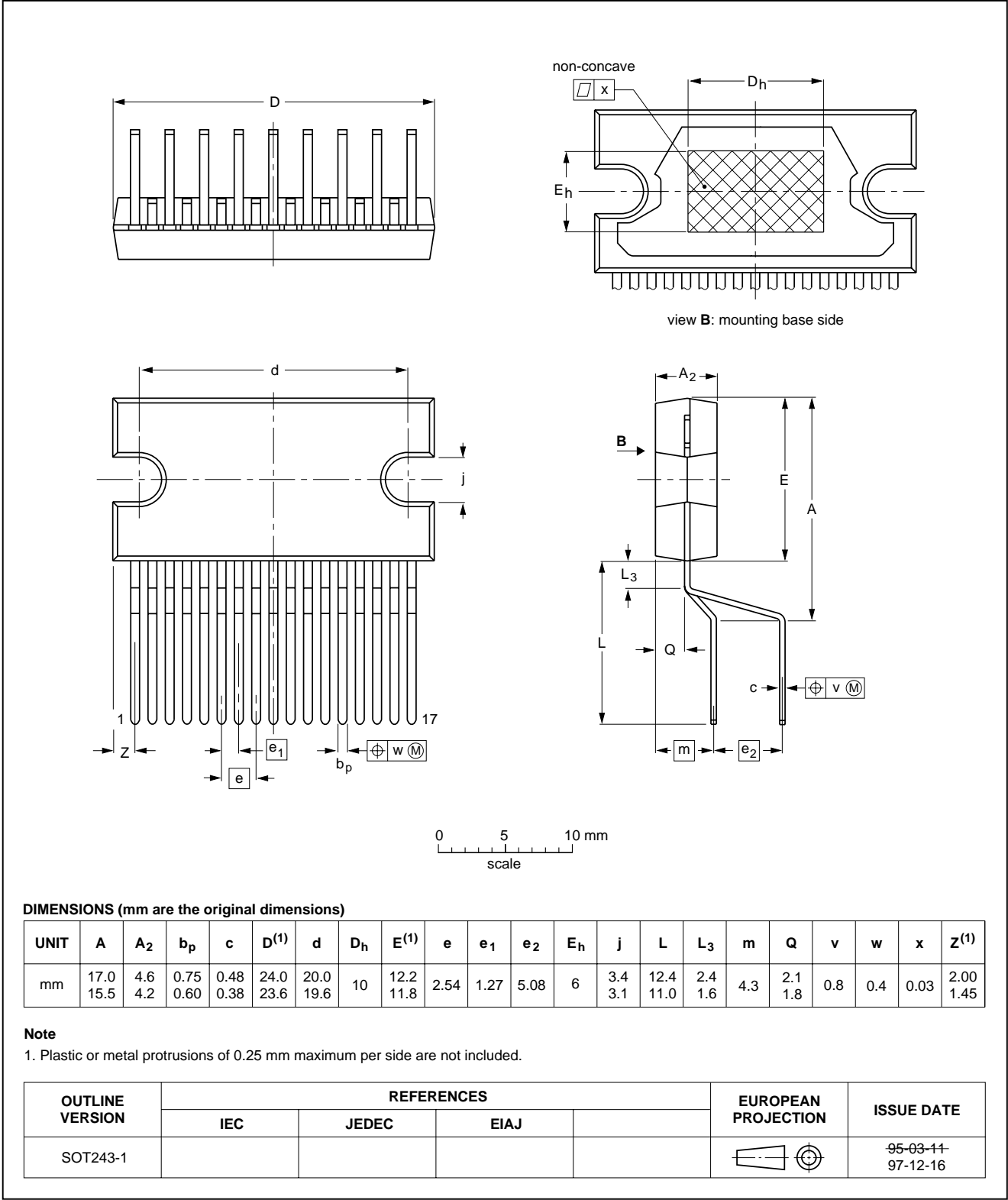
Power amplifier with load detection and
auto BTL/SE selection

TDA8586

PACKAGE OUTLINES

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1

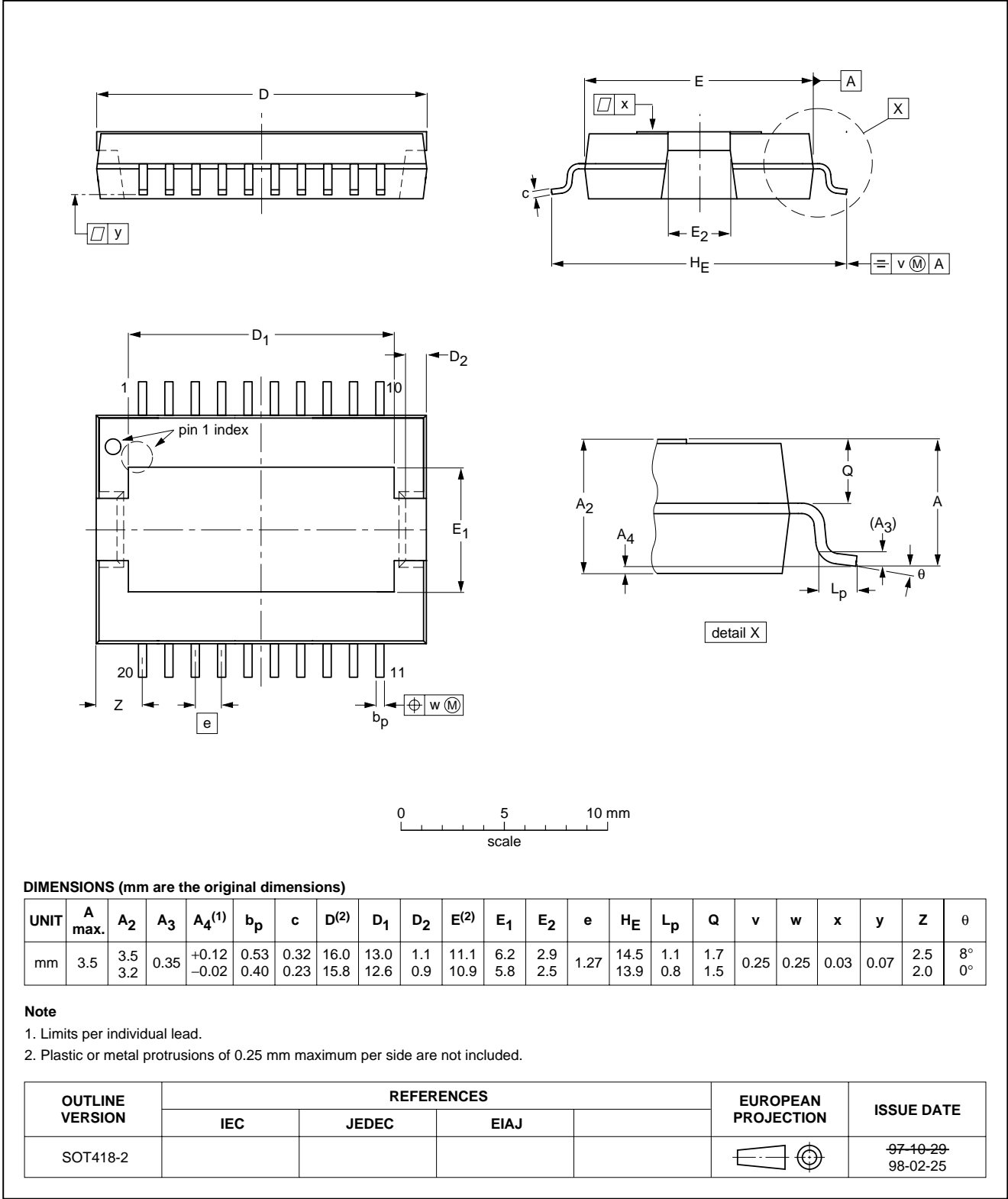


Power amplifier with load detection and
auto BTL/SE selection

TDA8586

HSOP20: heatsink small outline package; 20 leads; low stand-off

SOT418-2



Power amplifier with load detection and auto BTL/SE selection

TDA8586

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Power amplifier with load detection and auto BTL/SE selection

TDA8586

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW ⁽¹⁾	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable ⁽²⁾	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable ⁽³⁾	suitable	–
	PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable	–
	SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Power amplifier with load detection and
auto BTL/SE selection

TDA8586

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SCA63

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